

DISCRIPTION

2SC4524 is a silicon NPN epitaxial planar type transistor specifically designed for RF power amplifiers applications in 1.65GHz.

FEATURES

- High power gain: $G_{pb} \geq 5.4\text{dB}$, $P_O = 7\text{W}$
@ $V_{CC} = 28\text{V}$, $f = 1.65\text{GHz}$.
- High ruggedness: Ability to withstand 16:1 load VSWR when operated at $V_{CC} = 28\text{V}$, $f = 1.65\text{GHz}$, $P_O = 7\text{W}$.
- Emitter ballasted construction. Gold metalization die.

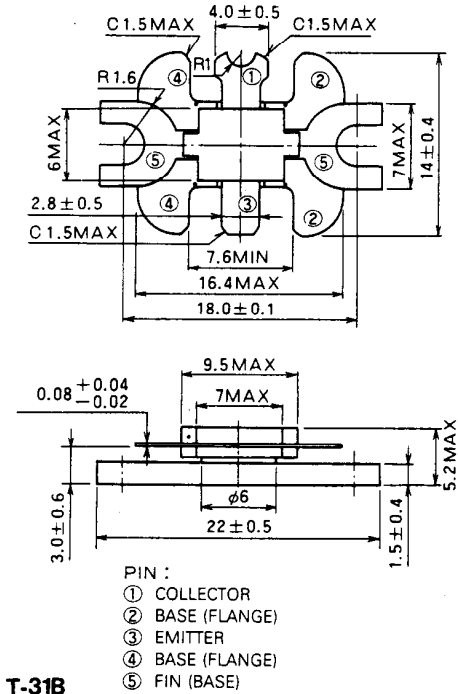
APPLICATION

For pre-amplifier stage of 50W, 1.6GHz - 1.65GHz, 28V, amamplifier.



OUTLINE DRAWING

Dimensions in mm



T-31B

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CBO}	Collector to base voltage		50	V
V_{EBO}	Emitter to base voltage		4	V
V_{CES}	Collector to emitter voltage	$R_{BE} = 0$	45	V
I_C	Collector current		2.5	A
P_C	Collector dissipation	$T_C = 25^\circ\text{C}$	30	W
T_J	Junction temperature		175	$^\circ\text{C}$
T_{Stg}	Storage temperature		-55 to 175	$^\circ\text{C}$
R_{th-c}	Thermal resistance	Junction to case	5.0	$^\circ\text{C}/\text{W}$

Note. Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{(BR)EBO}$	Emitter to base breakdown voltage	$I_E = 5\text{mA}$, $I_C = 0$	4.0			V
$V_{(BR)CBO}$	Collector to base breakdown voltage	$I_C = 10\text{mA}$, $I_E = 0$	50			V
$V_{(BR)CES}$	Collector to emitter breakdown voltage	$I_C = 10\text{mA}$, $R_{EB} = 0$	45			V
I_{CBO}	Collector cutoff current	$V_{CB} = 25\text{V}$, $I_E = 0$			1	mA
h_{FE}	DC forward current gain *	$V_{CE} = 5\text{V}$, $I_C = 1\text{A}$	10	50	180	—
P_O	Output power	$V_{CC} = 28\text{V}$, $f = 1.65\text{GHz}$, $P_{in} = 2\text{W}$	7	10		W
η_C	Collector efficiency		45	50		%

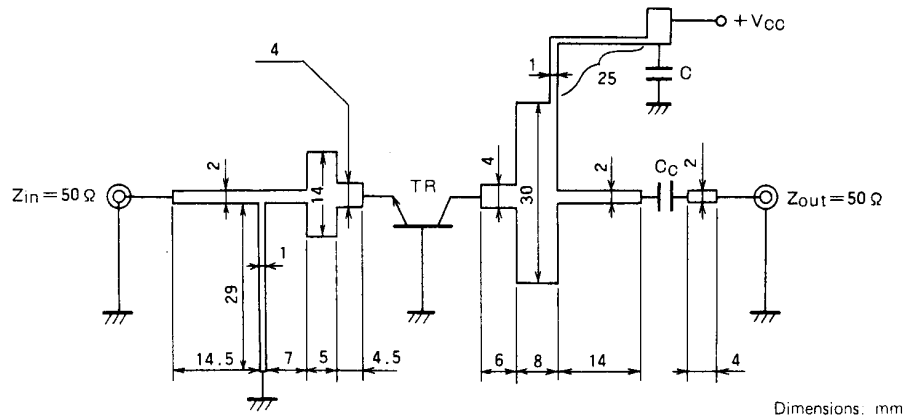
Note. * Pulse test, $P_W = 150\mu\text{s}$, duty = 5%.

Above parameters, ratings, limits and conditions are subject to change.

MITSUBISHI RF POWER TRANSISTOR 2SC4524

NPN EPITAXIAL PLANAR TYPE

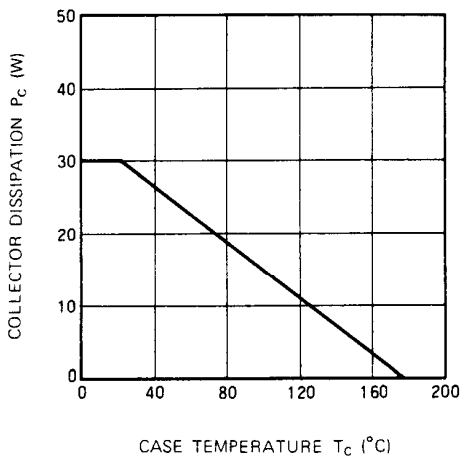
TEST CIRCUIT



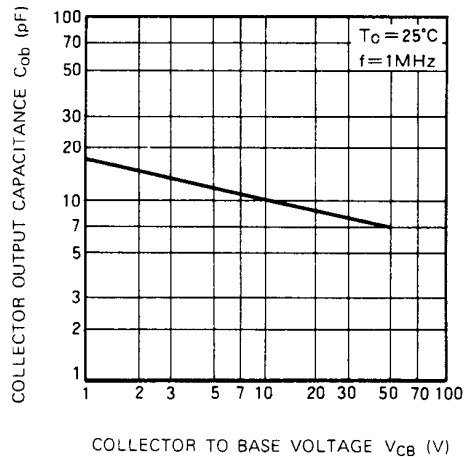
C_c : 50pF Chip capacita
 C : 50pF, 2200pF, 22000pF, 100 μ F in parallel
 Board Material: Teflon-Glass $t = 0.8$ mm

TYPICAL PERFORMANCE DATE

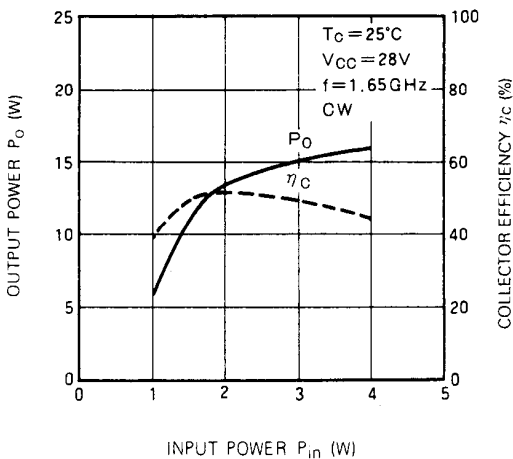
**COLLECTOR DISSIPATION VS.
CASE TEMPERATURE**



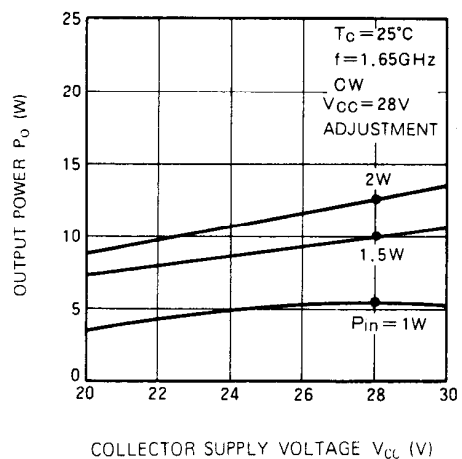
**COLLECTOR OUTPUT CAPACITANCE VS.
COLLECTOR TO BASE VOLTAGE**



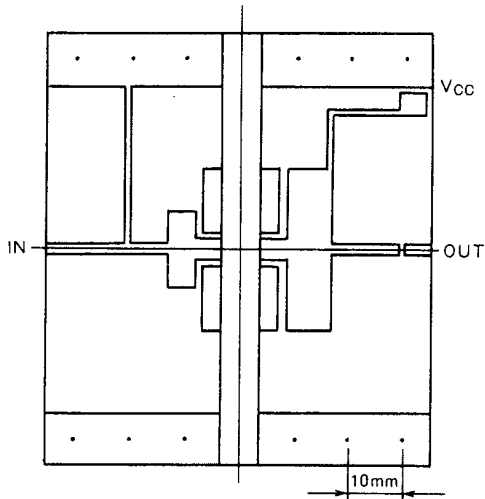
**OUTPUT POWER, COLLECTOR
EFFICIENCY VS. INPUT POWER**



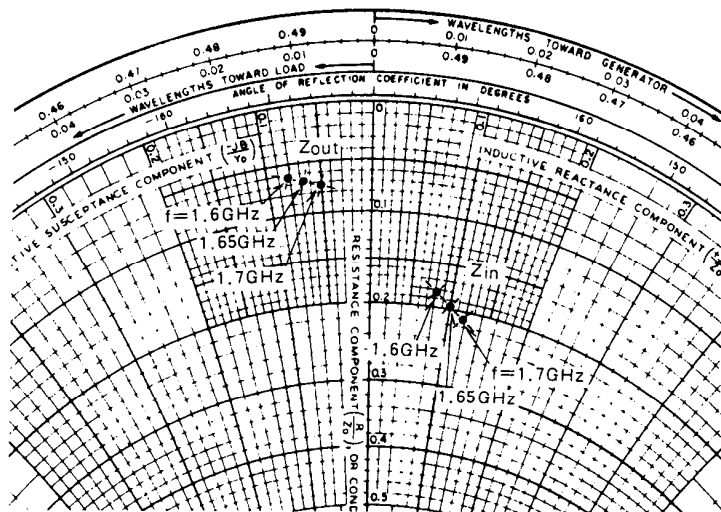
**OUTPUT POWER VS.
COLLECTOR SUPPLY VOLTAGE**



CIRCUIT PATTERN LAYOUT



INPUT AND OUTPUT SERIES IMPEDANCE



f	Z _{in} (Ω)	Z _{out} (Ω)
1.6GHz	9.2 + j4.0	3.2 - j3.0
1.65GHz	9.8 + j4.9	3.4 - j3.3
1.7GHz	10.3 + j6	3.7 - j2.5

CONDITIONS:
 V_{CC} = 28V, f = 1.6 - 1.7GHz,
 P₀ = 7W CW

NPN EPITAXIAL PLANAR TYPE

1. Special Instructions for Flange-Mounted Ceramic-Encapsulated High-Frequency High-Output Transistor Installation

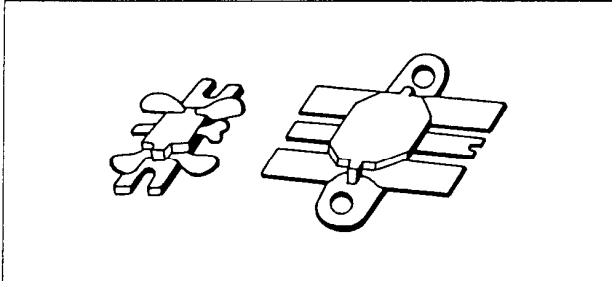


Fig. 1 Flange-Mounted Ceramic Encapsulated High-Frequency High-Output Transistor

When the flange-mounted ceramic-encapsulated transistor shown in Fig. 1 is mounted on a heat sink plate, be sure to follow the special instructions below, after referring to Fig. 2.

- (1) Be sure to use M3 x 0.5 screws for mounting the transistor.
- (2) Be sure that the fastening screws are tightened to a torque of 5 to 6kg.cm.
- (3) Application of lubricants (grease): Apply lubricant (grease) to all heat-conducting components, including the bottom of the flange, the fastening screws, inside the flange holes, and the holes of the heat sink fins. Particular care is required in applying the lubricant compound. Be the more careful the greater the higher the operating level of the device concerned is.
- (4) Be sure that the screw hole centers of the heat sink fins are spaced at a distance of $18.3 \pm 0.2\text{mm}$ and that the holes have a diameter of 3.5mm.
- (5) Take care to ensure that when the device is mounted on to the substrate, no tensile stress acting in the upward direction is applied to the leads. Mount so that the printed circuit board is positioned slightly lower than the bottom of the leads.
- (6) After the device has been mounted, solder the leads so that the soldering temperature is below 250°C and that the time used for soldering one lead is within 8 seconds.

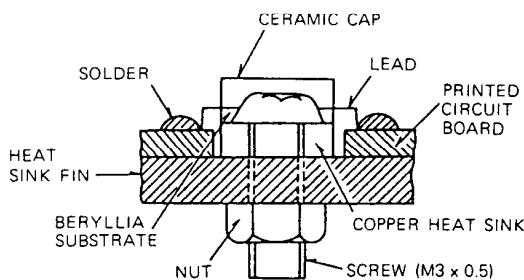


Fig. 2 Installation Procedure for Flange-Mounted Ceramic-Encapsulated Transistor with Printed Pattern on the Upper Surface

2. Precautions for Use of the Device

(1) Operating Junction Temperature (T_{jop})

Be sure to design the circuit so that the operating junction temperature T_{jop} will not exceed 130°C at ambient temperature conditions within 60°C .

(2) Base-Emitter Externally Connected Resistor

If a bias resistor is inserted between the base and emitter for AB class amplifiers, be sure to design the bias circuit so that the resistance remains below 5 ohm. If this resistance value is excessively high, the exciting input will be increased, accordingly and a reverse bias current will be applied between the base and the emitter, thereby giving rise to the problem of a reduction in h_{FE} and a drop in the output power.

(3) Guaranteed Characteristics

All graphic characteristics illustrated in this catalog are typical examples. The characteristics for the individual devices are guaranteed under the specified conditions laid down with respect to the absolute maximum ratings and electrical characteristics.

3. Disposal of Defective or Discarded Products

All types of resin-encapsulated and ceramic-encapsulated high-frequency high-output transistors as well as some metal-encapsulated high-frequency high-output transistors use beryllia porcelain. The inhalation of beryllia dust and/or vapors can be extremely dangerous to the human body. It is therefore essential not to attempt to break, crush, cut, or dispose of these devices at high temperatures (above 800°C) in a moisture-containing atmosphere.