CMOS single-chip 8-bit microcontrollers 83C576/87C576

FEATURES

- 80C51 based architecture
  - 8k × 8 ROM (83C576)
  - 8k × 8 EPROM (87C576)
  - 256 × 8 RAM
  - 10-bit, 6 channel A/D
  - Three 16-bit counter/timers
  - 2 PWM outputs
  - Programmable Counter Array
  - Universal Peripheral Interface
  - Enhanced UART
  - Oscillator fail detect
  - Low active reset
  - 4 analog comparators
  - Watchdog timer
  - Low V_{CC} detect
  - Power-on detect
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 6 to 16MHz
- Extended temperature ranges
- OTP package available
- EPROM/OTP versions can be programmed in circuit
- Software Reset
- 15 source, 2 level interrupt structure
- Lower EMI noise
- Programmable I/O pins
- Serial on-board programming
- Schmitt trigger inputs on Port 1

DESCRIPTION

The Philips 83C576/87C576 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC576 contains an 8k × 8 ROM (83C576) EPROM (87C576), a 256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a Programmable Counter Array (PCA), a 10-bit, 6 channel A/D, 2 PWM outputs, an 8-bit UPI interface, a fifteen-source, two-priority level nested interrupt structure, an enhanced UART, four analog comparators, power-fail detect and oscillator fail detect circuits, and on-chip oscillator and clock circuits.

In addition, the 8XC576 has a low active reset, and a software reset. There is also a fully configurable watchdog timer, and internal power on clear circuit. The part includes idle mode and power-down mode states for reduced power consumption.

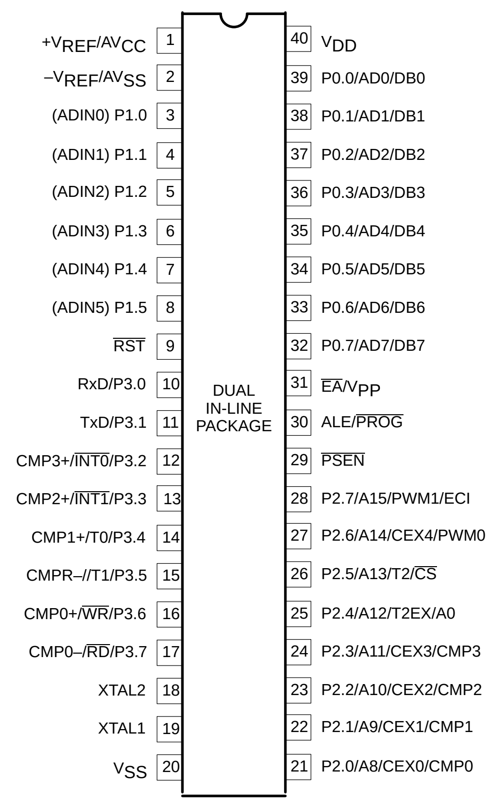
ORDERING INFORMATION

ROMless	ROM	EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQ (MHz)	DRAWING NUMBER
P80C576EBPN	P83C576EBPN	P87C576EBPN	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	16	SOT129-1
P80C576EBAA	P83C576EBAA	P87C576EBAA	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
		P87C576EBFFA	UV	0 to +70, 40-Pin Ceramic Dual In-line Package	16	0590B
		P87C576EBLKA	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier	16	1472A
P80C576EBBB	P83C576EBBB	P87C576EBBB	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	16	SOT307-2
P80C576EFPN	P83C576EFPN	P87C576EBPN	OTP	–40 to +85, 40-Pin Plastic Dual In-line Package	16	SOT129-1
P80C576EFAA	P83C576EFAA	P87C576EFAA	OTP	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
		P87C576EFFFA	UV	–40 to +85, 40-Pin Ceramic Dual In-line Package	16	0590B
		P87C576EFLKA	UV	–40 to +85, 44-Pin Ceramic Leaded Chip Carrier	16	1472A
P80C576EFBB	P83C576EFBB	P87C576EFBB	OTP	–40 to +85, 44-Pin Plastic Quad Flat Pack	16	SOT307-2
	P83C576EHPN	P87C576EHPN	OTP	–40 to +125, 40-Pin Plastic Dual In-line Package	16	SOT129-1
	P83C576EHAA	P87C576EHAA	OTP	–40 to +125, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
	P83C576EHBB	P87C576EHBB	OTP	–40 to +125, 44-Pin Plastic Quad Flat Pack	16	SOT307-2

NOTE:
1. OTP - One Time Programmable EPROM. UV - Erasable EPROM

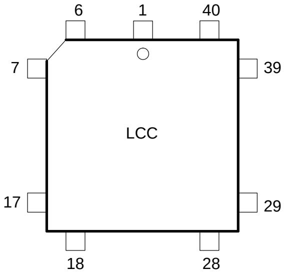
PIN CONFIGURATIONS

40-pin Dual In-line Package



SU00251A

44-pin Ceramic and Plastic Leaded Chip Carrier

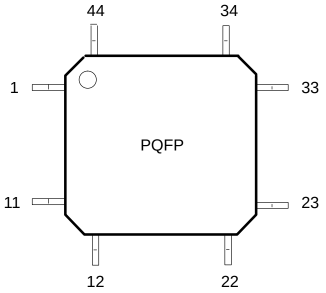


Pin	Function	Pin	Function	Pin	Function
1	NC*	16	T0/P3.4/CMP1+	31	P2.7/A15/PWM1/ECI
2	$+V_{REF}/AV_{CC}$	17	T1/P3.5/CMPR–	32	$\overline{\text{PSEN}}$
3	$-V_{REF}/AV_{SS}$	18	$\overline{\text{WR}}$/P3.6/CMP0+	33	ALE/$\overline{\text{PROG}}$
4	ADIN0/P1.0	19	$\overline{\text{RD}}$/P3.7/CMP0–	34	NC*
5	ADIN1/P1.1	20	XTAL2	35	$\overline{\text{EA}}/V_{PP}$
6	ADIN2/P1.2	21	XTAL1	36	P0.7/AD7/DB7
7	ADIN3/P1.3	22	V_{SS}	37	P0.6/AD6/DB6
8	ADIN4/P1.4	23	NC*	38	P0.5/AD5/DB5
9	ADIN5/P1.5	24	P2.0/A8/CEX0/CMP0	39	P0.4/AD4/DB4
10	$\overline{\text{RST}}$	25	P2.1/A9/CEX1/CMP1	40	P0.3/AD3/DB3
11	RxD/P3.0	26	P2.2/A10/CEX2/CMP2	41	P0.2/AD2/DB2
12	NC*	27	P2.3/A11/CEX3/CMP3	42	P0.1/AD1/DB1
13	TxD/P3.1	28	P2.4/A12/T2EX/A0	43	P0.0/AD0/DB0
14	$\overline{\text{INT}}$0/P3.2/CMP3+	29	P2.5/A13/T2/$\overline{\text{CS}}$	44	V_{CC}
15	$\overline{\text{INT}}$1/P3.3/CMP2+	30	P2.6/A14/CEX4/PWM0		

* DO NOT CONNECT

SU00252A

44-pin Plastic Quad Flat Pack

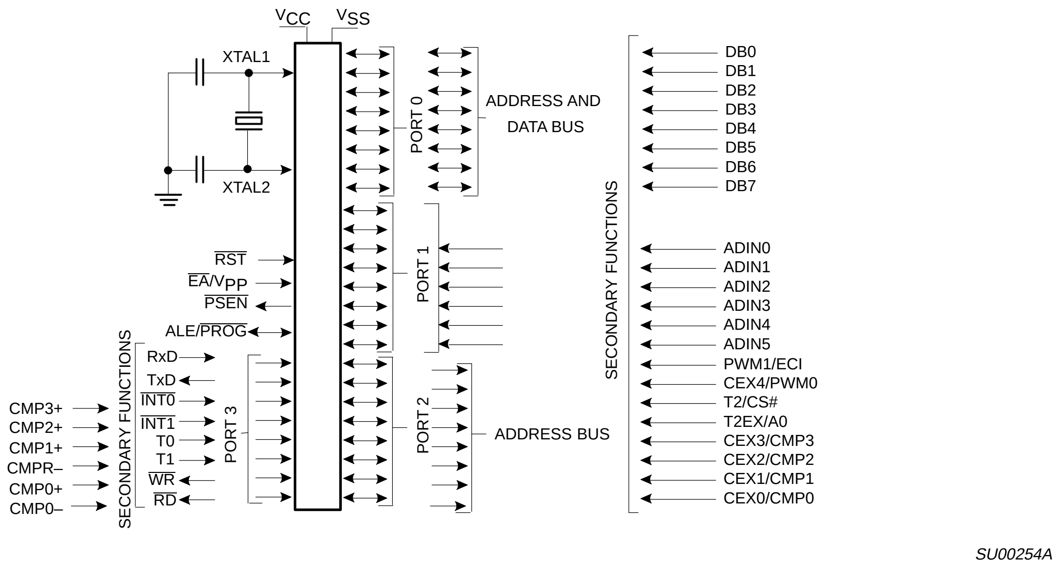


Pin	Function	Pin	Function	Pin	Function
1	ADIN3/P1.3	16	V_{SS}	31	P0.6/AD6/DB6
2	ADIN4/P1.4	17	NC*	32	P0.5/AD5/DB5
3	ADIN5/P1.5	18	P2.0/A8/CEX0/CMP0	33	P0.4/AD4/DB4
4	$\overline{\text{RST}}$	19	P2.1/A9/CEX1/CMP1	34	P0.3/AD3/DB3
5	RxD/P3.0	20	P2.2/A10/CEX2/CMP2	35	P0.2/AD2/DB2
6	NC*	21	P2.3/A11/CEX3/CMP3	36	P0.1/AD1/DB1
7	TXD/P3.1	22	P2.4/A12/T2EX/A0	37	P0.0/AD0/DB0
8	$\overline{\text{INT}}$0/P3.2/CMP3+	23	P2.5/A13/T2/$\overline{\text{CS}}$	38	V_{CC}
9	$\overline{\text{INT}}$1/P3.3/CMP2+	24	P2.6/A14/CEX4/PWM0	39	NC*
10	T0/P3.4/CMP1+	25	P2.7/A15/PWM1/ECI	40	$+V_{REF}/AV_{CC}$
11	T1/P3.5/CMPR–	26	$\overline{\text{PSEN}}$	41	$-V_{REF}/AV_{SS}$
12	$\overline{\text{WR}}$/P3.6/CMP0+	27	ALE/$\overline{\text{PROG}}$	42	ADIN0/P1.0
13	$\overline{\text{RD}}$/P3.7CMP0–	28	NC*	43	ADIN1/P1.1
14	XTAL2	29	$\overline{\text{EA}}/V_{PP}$	44	ADIN2/P1.2
15	XTAL1	30	P0.7/AD7/DB7		

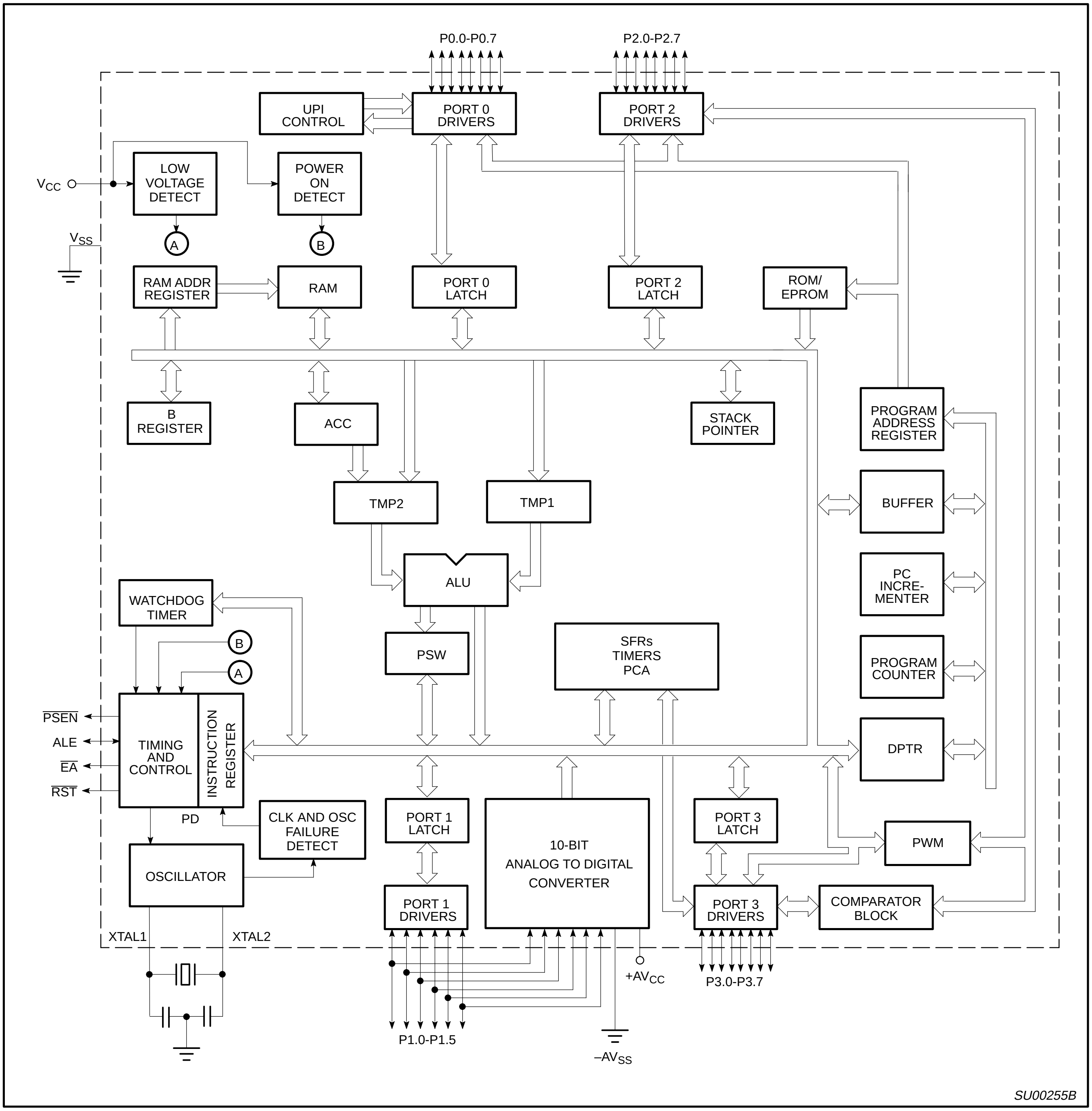
* DO NOT CONNECT

SU00253B

LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	 LCC	 QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0-0.7	39-32	43-36	37-30	I/O	**Port 0:** Port 0 is a bidirectional I/O port. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory (see Note 5). In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also receives code bytes during parallel EPROM programming and outputs code bytes during verification. External pull-ups are required during program verification. During reset, the port register is loaded with 1's. Port 0 has 4 output modes selected on a per bit basis by writing to the P0M1 and P0M2 Special Function Registers as follows: **P0M1.x** **P0M2.x** **Mode Description** 0 0 Open drain (default). See Note 1. 0 1 Weak pullup. See Note 2. 1 0 High impedance. See Note 3. 1 1 Push-pull. See Note 4. Port 0 is also the data I/O port for the Universal Peripheral Interface (UPI). When the UPI is enabled, port 0 must be configured as High-Z by the user. Input/Output through P0 is controlled by pin $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, and A0. Output is push-pull when enabled.
P1.0-P1.5	3-8	5-9	42-44 1-3	I/O	**Port 1:** Port 1 is a 6-bit bidirectional I/O port with Schmitt trigger inputs. Port 1 receives the control signals during program memory verification and parallel EPROM programming. During reset, port 1 is configured as a high impedance analog input port. Digital push-pull outputs are enabled by writing 1's to the P1M1 register. The programmer must take care to prevent digital outputs from switching while an A/D conversion is in progress. **P1M1.X** **P1M2.X** **Mode Description** 0 0 A/D only. (High impedance) 0 1 Digital input only. High impedance (default). 1 X Push-pull. Port 1 pins also serve alternate functions as follows:
	3	4	42	I/O	P1.0/ADIN0
	4	5	43	I/O	P1.1/ADIN1
	5	6	44	I/O	P1.2/ADIN2
	6	7	1	I/O	P1.3/ADIN3
	7	8	2	I/O	P1.4/ADIN4
	8	9	3	I/O	P1.5/ADIN5
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port. Port 2 emits the high-order address byte during accesses to external program and data memory that use 16-bit addresses (MOVX @DPTR) (see Note 5). In this application, it uses strong internal pull-ups when emitting 1s. Port 2 receives the high-order address byte during program verification and parallel EPROM programming. During reset, the port 2 pullups are turned on synchronously, and the port register is loaded with 1's. Port 2 has the following output modes which can be selected on a per bit basis by writing to P2M1 and P2M0: **P2M1.X** **P2M2.X** **Mode Description** 0 0 Open drain. See Note 1. 0 1 Weak pullup (default). See Note 2. 1 0 High impedance. See Note 3. 1 1 Push-pull. See Note 4. Port 2 pins serve alternate functions as follows:
	21	24	18		**P2.0** **CEX0** PCA module 0 external I/O **CMP0** comparator 0 output
	22	25	19		**P2.1** **CEX1** PCA module 1 external I/O **CMP1** comparator 1 output
	23	26	20		**P2.2** **CEX2** PCA module 2 external I/O **CMP2** comparator 2 output
	24	27	21		**P2.3** **CEX3** PCA module 3 external I/O **CMP3** comparator 3 output
	25	28	22		**P2.4** **T2EX** timer 2 capture input **A0** UPI address input
	26	29	23		**P2.5** **T2** timer 2 external I/O — clock-out (programmable) $\overline{\textbf{CS}}$ UPI chip select input
	27	30	24		**P2.6** **CEX4** PCA module 4 external I/O **PWM0** Pulse width modulator 0 output
	28	31	25		**P2.7** **ECI** PCA count input **PWM1** Pulse width modulator 1 output

PIN DESCRIPTIONS (Continued)

	PIN NUMBER				
MNEMONIC	**DIP**	**LCC**	**QFP**	**TYPE**	**NAME AND FUNCTION**
$+V_{REF}/AV_{CC}$	1	2	40	I	**A/D positive power supply**
$–V_{REF}/AV_{SS}$	2	3	41	I	**A/D 0V reference**
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port. Port 3 pins that have 1s written to them can be used as inputs but will source current when externally pulled low (see DC Electrical Characteristics: I_{IL}). During reset all pins will be synchronously driven high and will remain high until written to by software. Port 3 has the following output modes which can be selected on a per bit basis by writing to P3M1 and P3M2: **P3M1.X** **P3M2.X** **Mode Description** 0 0 Open drain. See Note 1. 0 1 Weak pullup (default). See Note 2. 1 0 High impedance. See Note 3. 1 1 Push-pull. See Note 4. Port 3 pins serve alternate functions as follows:
	10	11	5	I	**P3.0** **RxD** Serial receive port
	11	13	7	O	**P3.1** **TxD** Serial transmit port (enabled only when transmitting serial data)
	12	14	8	I	**P3.2** **$\overline{\text{INT0}}$** External interrupt 0 **CMP3+** Comparator 3 positive input
	13	15	9	I	**P3.3** **$\overline{\text{INT1}}$** External interrupt 1 **CMP2+** Comparator 2 positive input
	14	16	10	I	**P3.4** **T0** Timer/counter 0 input **CMP1+** Comparator 1 positive input
	15	17	11	I	**P3.5** **T1** Timer/counter 1 input **CMPR–** Common reference to comparators 1, 2, 3
	16	18	12	O	**P3.6** **$\overline{\text{WR}}$** External data memory write strobe **CMP0+** Comparator 0 positive input
	17	19	13	O	**P3.7** **$\overline{\text{RD}}$** External data memory read strobe **CMP0–** Comparator 0 negative input
$\overline{\text{RST}}$	9	10	4	I	**Reset:** A low on this pin synchronously resets all port pins to a high state. The pin must be held low with the oscillator running for 24 oscillator cycles to initialize the internal registers. An internal diffused resistor to V_{CC} permits a power on reset using only an external capacitor to V_{SS}. RST has a Schmitt trigger input stage to provide additional noise immunity with a slow rising input voltage.
ALE/$\overline{\text{PROG}}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE is switched off if the bit 0 in the AUXR register (8EH) is set. This pin is also the program pulse input ($\overline{\text{PROG}}$) during parallel EPROM programming. (See also Internal Reset on page 3-779.)
$\overline{\text{PSEN}}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{PP}$	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If this pin is at V_{PP} voltage during reset the device enters the in-circuit programming mode.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTES:
1. When Open Drain mode is selected, ports 0 and 2 have weak pulldowns to guarantee positive leakage current (see DC electrical characteristic I_{IH}).
2. When Weak Pullup mode is selected, ports bits that have 1's written to them can be used as inputs but will source current when externally pulled low (see DC electrical characteristic I_{IL}).
3. When High Impedance mode is selected, all pullups and pulldowns are turned off. The only current sourced or sunk by the pin is the parasitic leakage current (see DC electrical characteristic I_{L2} or I_{LC}, as applicable.
4. When Push-Pull mode is selected, strong pullups are on continuously when emitting 1's (see DC electrical characteristic V_{OH}).
5. When Open-Drain, Weak Pull-up, or Push-pull mode is selected.

Table 1. 87C576 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
ADC0H#	A/D Channel 0 MSB	AAH									00H
ADC1H#	A/D Channel 1 MSB	ABH									00H
ADC2H#	A/D Channel 2 MSB	ACH									00H
ADC3H#	A/D Channel 3 MSB	ADH									00H
ADC4H#	A/D Channel 4 MSB	AEH									00H
ADC5H#	A/D Channel 5 MSB	AFH									00H
ADC0L#	A/D Channel 0 2-LSBits	9AH									00H
ADC1L#	A/D Channel 1 2-LSBits	9BH									00H
ADC2L#	A/D Channel 2 2-LSBits	9CH									00H
ADC3L#	A/D Channel 3 2-LSBits	9DH									00H
ADC4L#	A/D Channel 4 2-LSBits	9EH									00H
ADC5L#	A/D Channel 5 2-LSBits	9FH									00H
ADCON#	A/D Control	B1H	ADF	ADCE	AD8M	AMOD1	AMOD0	ASCA2	ASCA1	ASCA0	00H
ADCS#	A/D Channel Select	B2H									00H
AUXR#	Auxiliary	8EH	–	–	–	–	SRST	TXI	LO	AO	xxxx0000B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxxB
CCAPM0#	Module 0 Mode	DAH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM1#	Module 1 Mode	DBH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM2#	Module 2 Mode	DCH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM3#	Module 3 Mode	DDH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM4#	Module 4 Mode	DEH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
			DF	DE	DD	DC	DB	DA	D9	D8	
CCON*#	PCA Counter Control	D8H	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000B
CH#	PCA Counter High	F9H									00H
CL#	PCA Counter Low	E9H									00H
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF	00xxx000B
			C7	C6	C5	C4	C3	C2	C1	C0	
CMP*#	Comparator	C0H	EC3DP	EC2DP	EC1DP	EC0DP	C3RO	C2RO	C1RO	C0RO	00H
CMPE#	Comparator Enable	92H	EC3TDC	EC2TDC	EC1TDC	EC0TDC	EC3O	EC2O	EC1O	EC0O	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE0*#	Interrupt Enable 0	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IE1*#	Interrupt Enable 1	E8H	EOB	EIB	EAD	EC4	EC3	EC2	EC1	EC0	00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

Table 1. 87C576 Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*	Interrupt Priority 0	B8H	–	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
IP1*#	Interrupt Priority 1	F8H	POB	PIB	PAD	PC4	PC3	PC2	PC1	PC0	00H
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	ADIN5	ADIN4	ADIN3	ADIN2	ADIN1	ADIN0	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	ECI	CEX4	T2	T2EX	CEX3	CEX2	CEX1	CEX0	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
P0M1#	Port 0 Output Mode 1	84H									00H
P0M2#	Port 0 Output Mode 2	85H									00H
P1M1#	Port 1 Output Mode 1	94H									00H
P1M2#	Port 1 Output Mode 2	95H									3FH
P2M1#	Port 2 Output Mode 1	A4H									00H
P2M2#	Port 2 Output Mode 2	A5H									FFH
P3M1#	Port 3 Output Mode 1	B4H									00H
P3M2#	Port 3 Output Mode 2	B5H									FFH
PCON	Power Control	87H	SMOD1	SMOD0	OSF^1	POF^1	LVF^1	WDT0F^1	PD	IDL	00xxxx00B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
PWCON#	PWM Control	BCH	–	–	–	–	PWMF	EN/$\overline{CLR}$	PWE1	PWE0	00H
PWMP#	PWM Prescaler	BDH									00H
PWM0#	PWM Register 0	BEH									00H
PWM1#	PWM Register 1	BFH									00H
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE^2	DCEN	xxxxxxx0B

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
1. Reset value depends on reset source.
2. Programmable clock-out

Table 1. 87C576 Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
UCS#	UPI Control/Status	86H	ST7	ST6	ST5	ST4	UE	AF	IBF	OBE/OBF	00H
			C7	C6	C5	C4	C3	C2	C1	C0	
WDCON#	Watchdog Timer Control	C4H	PRE2	PRE1	PRE0	LVRE	OFRE	DPD	WDRUN	WDMOD	11111111B
WDL#	Watchdog Timer Reload	C1H									00H
WFEED1#	Watchdog Feed 1	C2H									xxH
WFEED2#	Watchdog Feed 2	C3H									xxH

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
1. Reset value depends on reset source.

The 8XC576 has a number of failure detect circuits to prevent abnormal operating conditions. these failure detect circuits generate resets as shown in Figure 1.

POWER ON CLEAR / POWER ON FLAG

An on-chip Power On Detect Circuit resets the 8XC576 and sets the Power Off Flag (PCON.4) on power up or if V_{CC} drops to zero momentarily. The POF can only be cleared by software. The RST pin is not driven by the power on detect circuit. The POF can be read by software to determine that a power failure has occurred and can also be set by software.

LOW VOLTAGE DETECT

An on-chip Low Voltage Detect circuit sets the Low Voltage Flag (PCON.3) if V_{CC} drops below V_{LOW} (see DC Electrical Characteristics) and resets the 8XC576 if the Low Voltage Reset Enable bit (WDCON.4) is set. If the LVRE is cleared, the reset is disabled but LVF will still be set if V_{CC} is low. The $\overline{\text{RST}}$ pin is not driven by the low voltage detect circuit. The LVF can be read by software to determine that V_{CC} was low. The LVF can be set or cleared by software.

OSCILLATOR FAIL DETECT

An on-chip Oscillator Fail Detect circuit sets the Oscillator Fail Flag (PCON.5) if the oscillator frequency drops below OSCF for one or more cycles (see AC Electrical Characteristics: OSCF) and resets the 8XC576 if the Oscillator Fail Reset Enable bit (WDCON.3) is set. If OFRE is cleared, the reset is disabled but OSF will still be set if the oscillator fails. The RST pin is not driven by the oscillator fail detect circuit. The OSF can be read by software to determine that an oscillator failure has occurred. The OSF can be set or cleared by software.

LOW ACTIVE RESET

One of the most notable features on this part is the low active reset. The low active reset operates exactly the same as high active reset with the exception that the part is put into the reset mode by applying a low level to the reset pin. For power-on reset it is also necessary to invert the power-on reset circuit; connecting the 8.2K resistor from the reset pin to V_{CC} and the 10µf capacitor from the reset pin to ground. Figure 1 shows the reset related circuitry.

When reset the port pins on the 8XC576 are driven high synchronously.

The 8XC576 also has Low voltage detection circuitry that will, if enabled, force the part to reset when V_{CC} (on the part) fails below a set level. Low Voltage Reset is enabled by a normal reset. Low Voltage Reset can be disabled by clearing LVRE (bit 4 in the WDCON SFR) then executing a watchdog feed sequence (A5H to WFEED1 followed immediately by 5AH to WFEED2). In addition there is a flag (LVF) that is set if a low voltage condition is detected. The LVF flag is set even if the Low Voltage detection circuitry is disabled. Notice that the Low voltage detection circuitry does not drive the RST# pin so the LVF flag is the only way that the microcontroller can determine if it has been reset due to a low voltage condition.

The 8XC576 has an on-chip power-on detection circuit that sets the POF (PCON.4) flag on power up or if the V_{CC} level momentarily drops to 0V. This flag can be used to determine if the part is being started from a power-on (cold start) or if a reset has occurred due to another condition (warm start).

The 8XC576 can be reset in software by setting the RST bit of the AUXR register (AUXR.3). See Figure 1 for reset diagram.

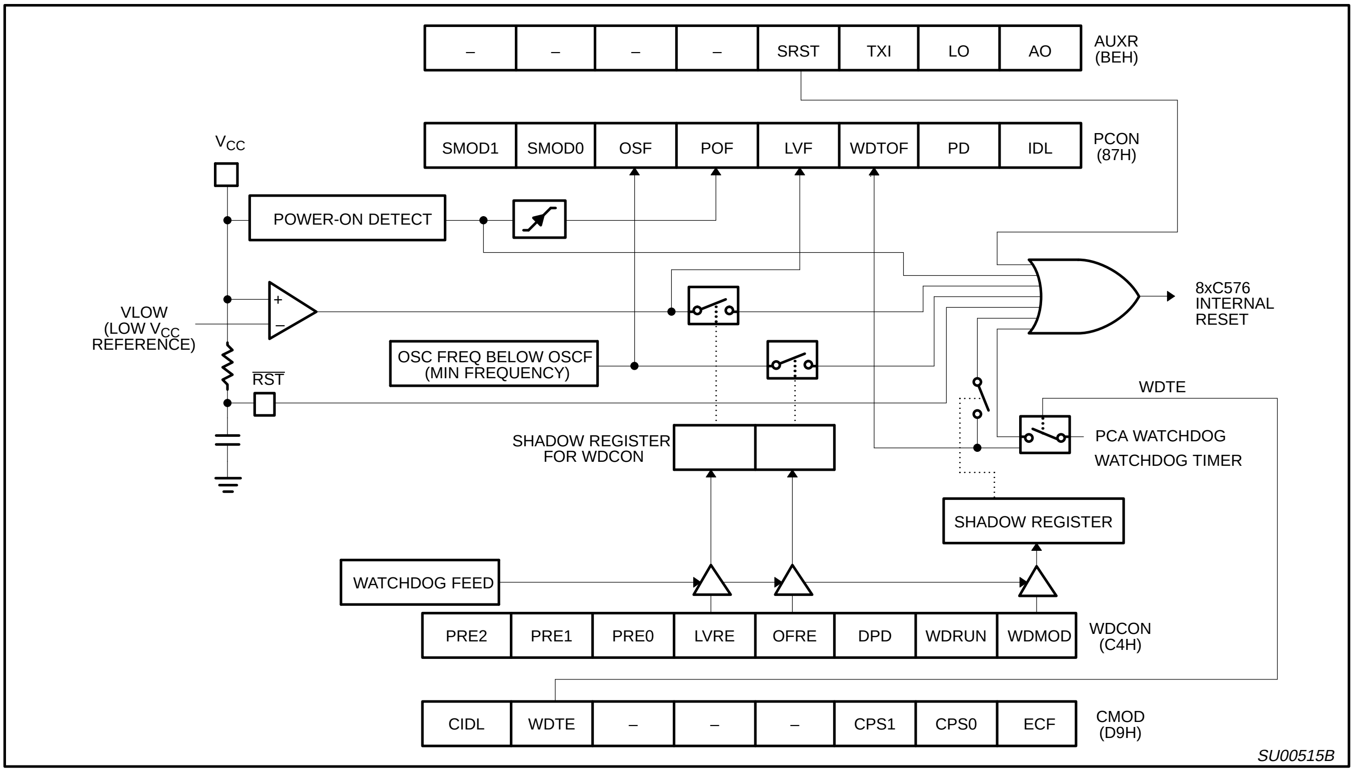


Figure 1. Reset Circuitry

TIMERS

The 8XC576 has four on-chip timers.

Timers 0 and 1 are identical in every way to Timers 0 and 1 on the 80C51.

Timer 2 on the 8XC576 is identical to the 80C52 Timer 2 (described in detail in the 80C52 overview) with the exception that it is an up or down counter. To configure the Timer to count down the DCEN bit in the T2MOD special function register must be set and a low level must be present on the T2EX pin (P1.1).

The Pulse Width Modulator (PWM) system can be used as a timer by disabling its outputs and monitoring its counter overflow flag, the PWMF bit in the PWCON register (see the PWM section for details).

The Watchdog timer operation and implementation is similar to the 8XC550 (for additional information see the 8XC550 datasheet) with the exception that the reset values of the WDCON and WDL special function registers have been changed. The changes in these registers cause the watchdog timer to be enabled with a timeout of 16384 × T_{OSC} when the part is reset. The watchdog can be disabled by executing a valid feed sequence and then clearing WDRUN (bit 2 in the WDCON SFR). In timer mode, the timer is controlled by toggling the WDRUN bit. The timeout flag, WDTOF, is set when the timer overflows and must be cleared in software.

PROGRAMMABLE COUNTER ARRAY (PCA)

The Programmable Counter Array is a special Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 2. Module 0 is connected to P2.0(CEX0), module 1 to P2.1(CEX1), etc. The basic PCA configuration is shown in Figure 2.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P2.7). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 3):

CPS1	CPS0	PCA Timer Count Source
0	0	1/12 oscillator frequency
0	1	1/4 oscillator frequency
1	0	Timer 0 overflow
1	1	External Input at ECI pin (P2.7)

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 3.

The watchdog timer function is implemented in module 4 as implemented in other parts that have a PCA that are available on the market. However, if a watchdog timer is required in the target application, it is recommended to use the hardware watchdog timer that is implemented on the 87C576 separately from the PCA (see Figure 15).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 6). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 4.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 7). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 8 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 2) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated. Refer to Figure 9.

16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 10).

High Speed Output Mode

In this mode the CEX output (on port 2) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 11).

Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. the allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

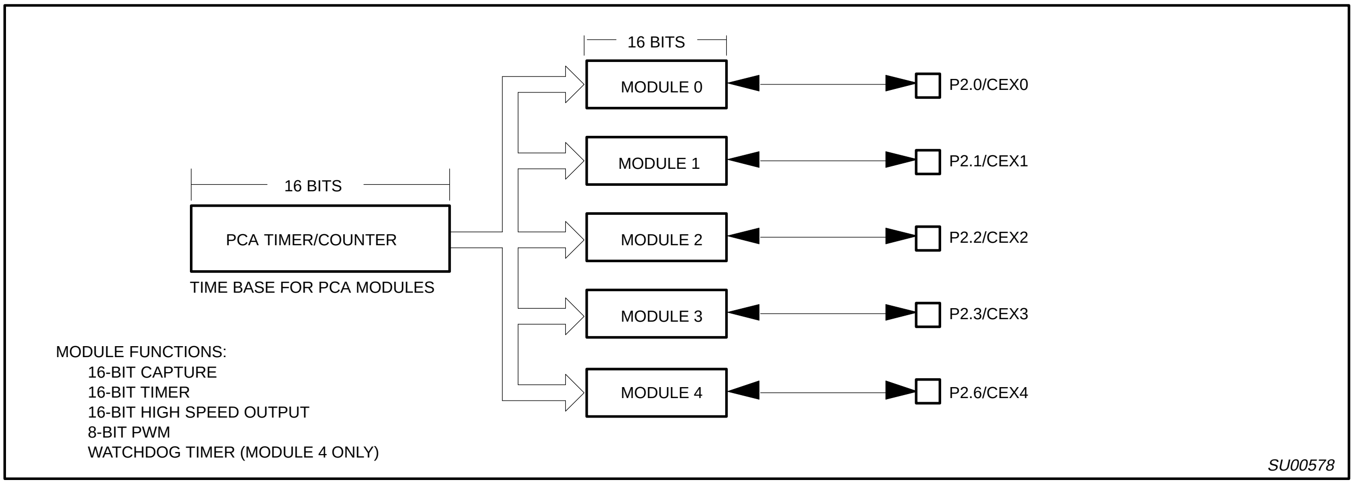


Figure 2. Programmable Counter Array (PCA)

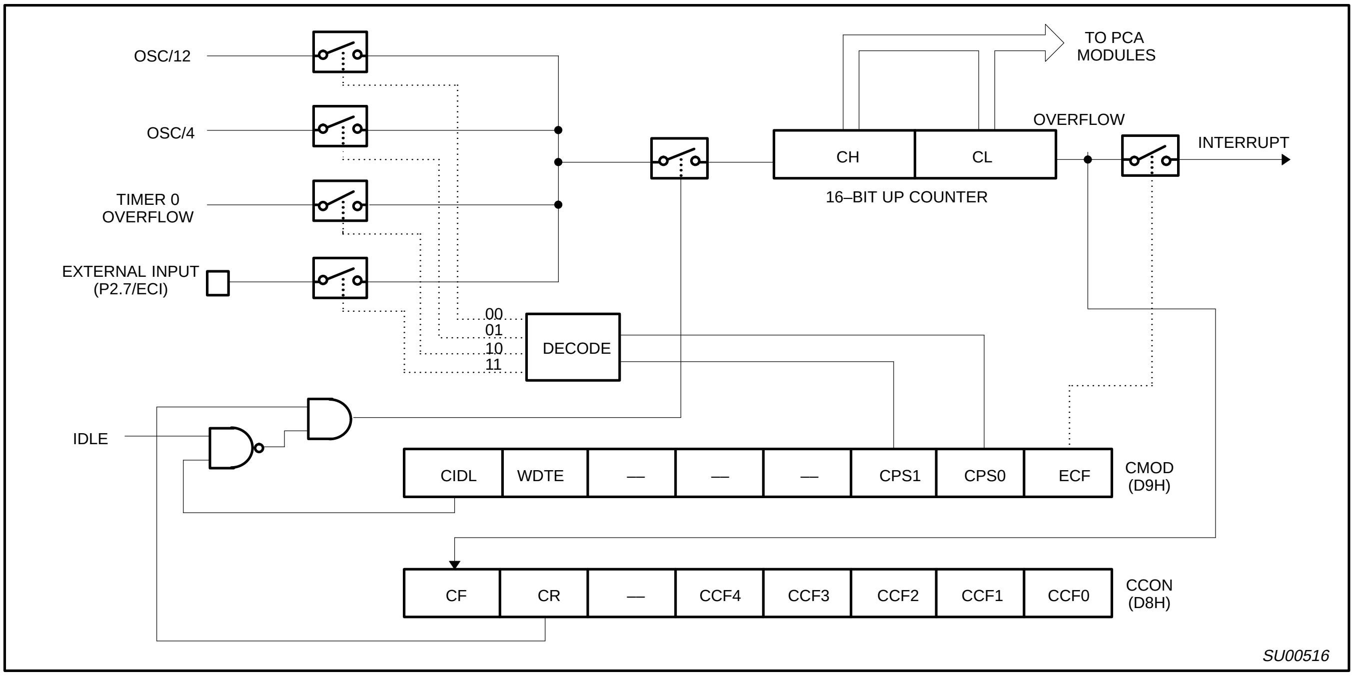


Figure 3. PCA Timer/Counter

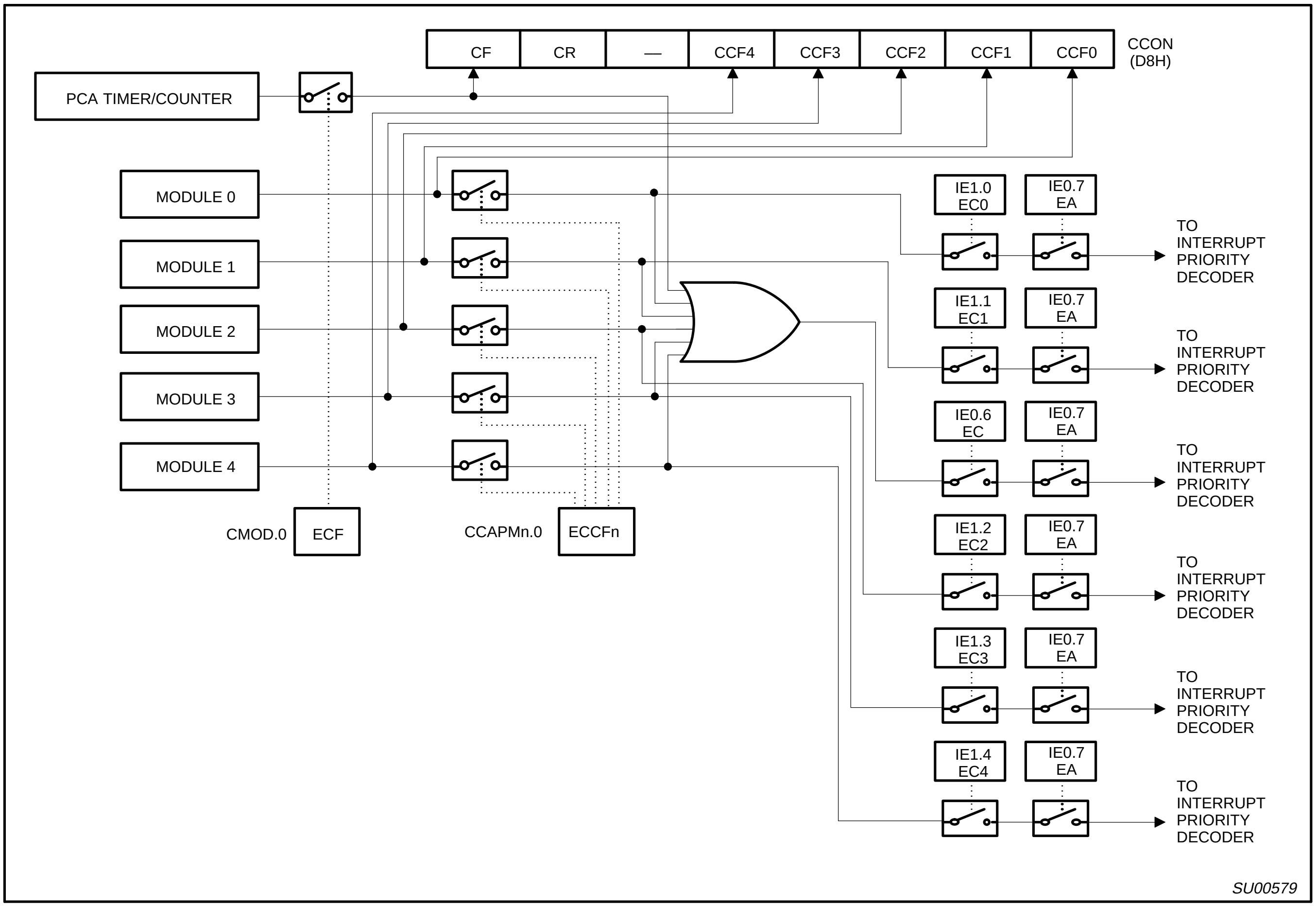


Figure 4. PCA Interrupt System

CMOD Address = OD9H

Reset Value = 00XX X000B

	CIDL	**WDTE**	**–**	**–**	**–**	**CPS1**	**CPS0**	**ECF**
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
–	Not implemented, reserved for future use.*
CPS1	PCA Count Pulse Select bit 1.
CPS0	PCA Count Pulse Select bit 0.

CPS1	**CPS0**	**Selected PCA Input****	
0	0	0	Internal clock, $f_{OSC} \div 12$
0	1	1	Internal clock, $f_{OSC} \div 4$
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P2.7 pin (max. rate = $f_{OSC} \div 8$)

Symbol	Function
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

NOTE:

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

** –f_{OSC} = oscillator frequency

SU00686A

Figure 5. CMOD: PCA Counter Mode Register

CCON Address = OD8H

Reset Value = 00X0 0000B

Bit Addressable

	CF	**CR**	**–**	**CCF4**	**CCF3**	**CCF2**	**CCF1**	**CCF0**
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
–	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

NOTE:

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU00036

Figure 6. CCON: PCA Counter Control Register

CCAPMn Address

CCAPM0	0DAH
CCAPM1	0DBH
CCAPM2	0DCH
CCAPM3	0DDH
CCAPM4	0DEH

Reset Value = X000 0000B

Not Bit Addressable

	–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use*.
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU00037

Figure 7. CCAPMn: PCA Modules Compare/Capture Registers

–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 8. PCA Module Modes (CCAPMn Register)

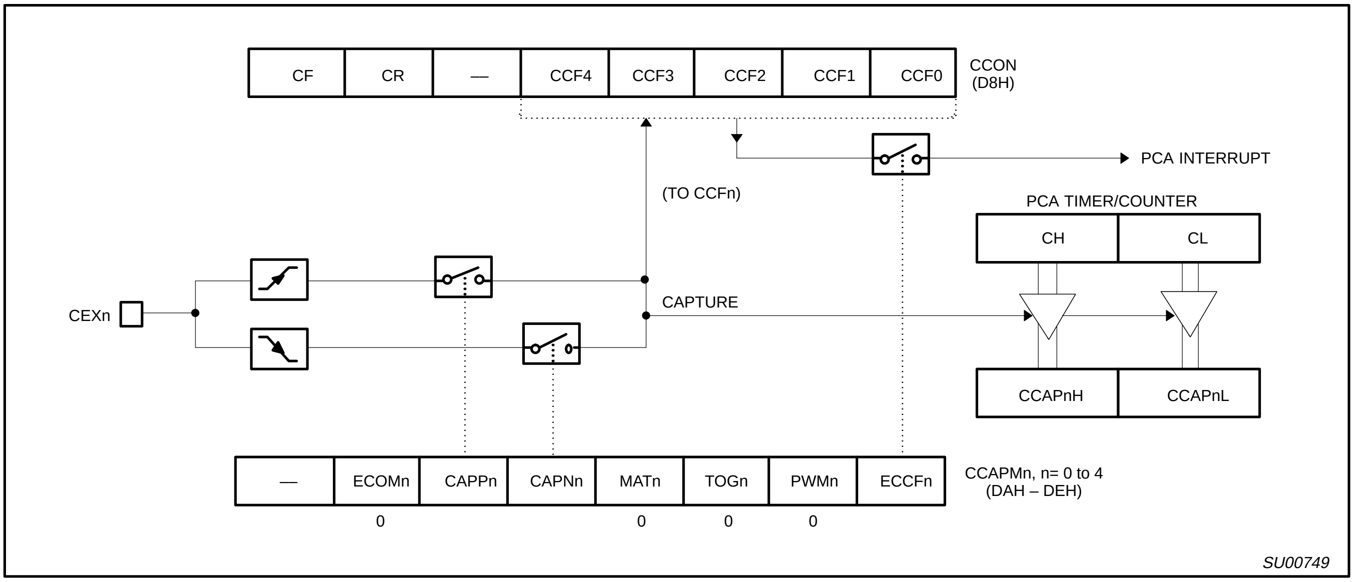


Figure 9. PCA Capture Mode

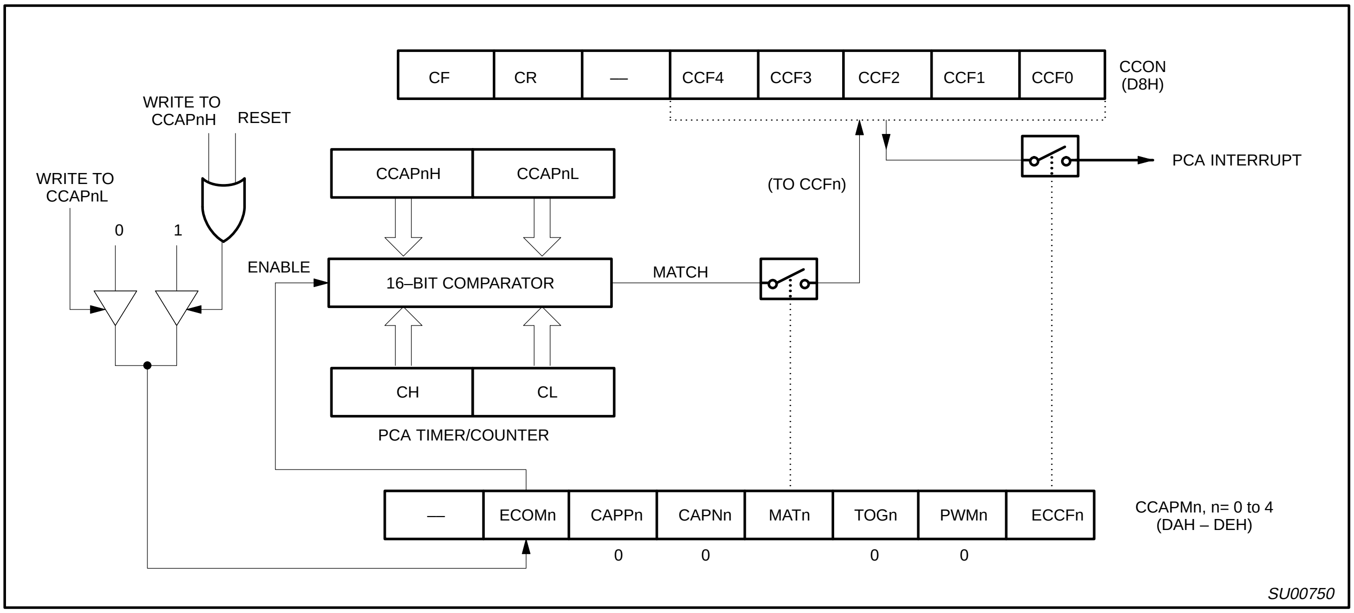


Figure 10. PCA Compare Mode

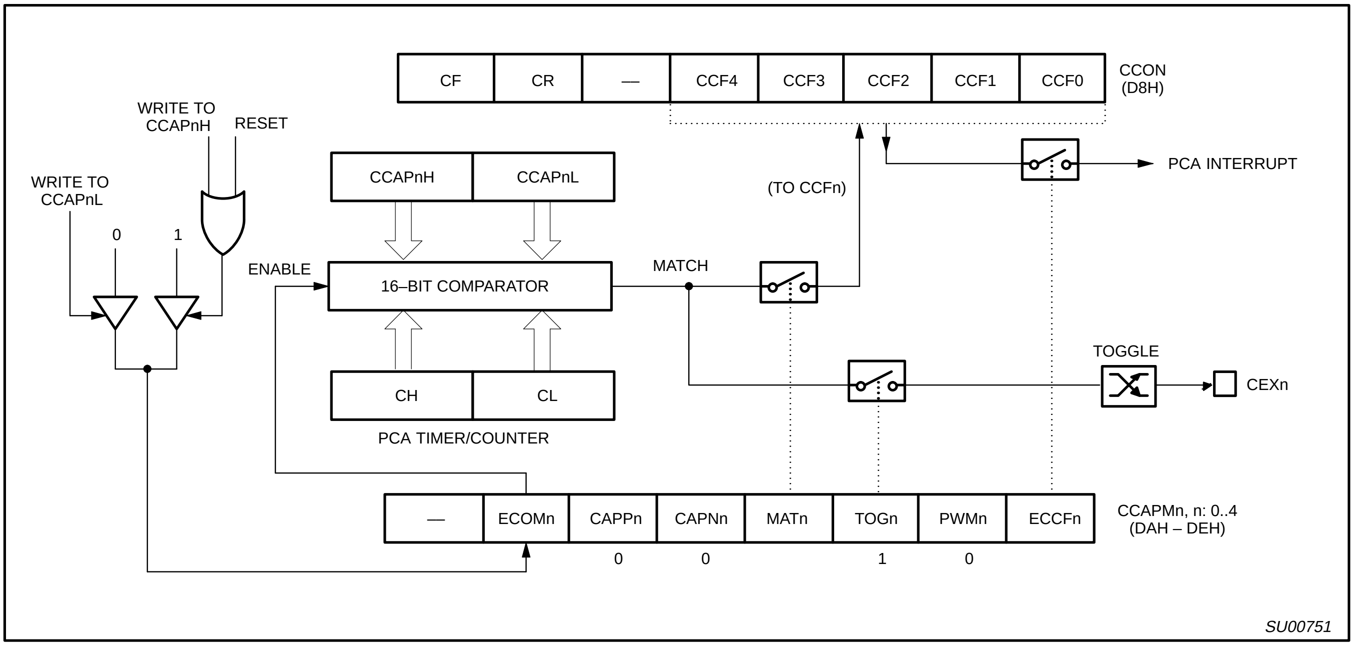


Figure 11. PCA High Speed Output Mode

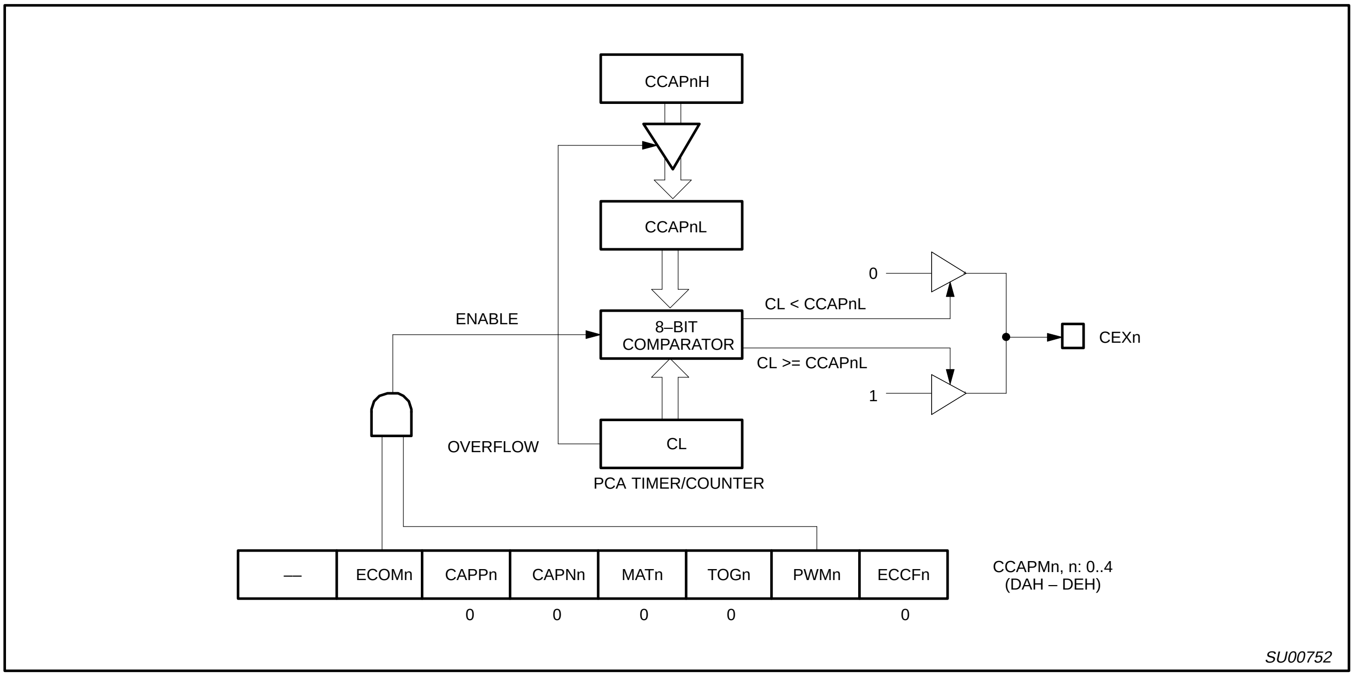


Figure 12. PCA PWM Mode

WATCHDOG TIMER

The watchdog timer is not directly loadable by the user. Instead, the value to be loaded into the main timer is held in an autoload register or is part of the mask ROM programming. In order to cause the main timer to be loaded with the appropriate value, a special sequence of software action must take place. This operation is referred to as feeding the watchdog timer.

To feed the watchdog, two instructions must be sequentially executed successfully. No intervening instruction fetches are allowed, so interrupts should be disabled before feeding the watchdog. The instructions should move A5H to the WFEED1 register and then 5AH to the WFEED2 register. If WFEED1 is correctly loaded and WFEED2 is not correctly loaded, then an immediate underflow will occur.

The watchdog timer subsystem has two modes of operation. Its principal function is a watchdog timer. In this mode it protects the system from incorrect code execution by causing a system reset when the watchdog timer underflows as a result of a failure of software to feed the timer prior to the timer reaching its terminal count. If the user does not employ the watchdog function, the watchdog subsystem can be used as a timer. In this mode, reaching the terminal count sets a flag. In most other respects, the timer mode possesses the characteristics of the watchdog mode. This is done to protect the integrity of the watchdog function.

The watchdog timer subsystem consists of a prescaler and a main counter. The prescaler has 8 selectable taps off the final stages and the output of a selected tap provides the clock to the main counter. The main counter is the section that is loaded as a result of the software feeding the watchdog and it is the section that causes the system reset (watchdog mode) or time-out flag to be set (timer mode) if allowed to reach its terminal count.

Programming the Watchdog Timer

Both the EPROM and ROM devices have a set of SFRs for holding the watchdog autoload values and the control bits. The watchdog time-out flag is present in the PCON register and operates the same in all versions. In the EPROM device, the watchdog parameters (autoload value and control) are always taken from the SFRs. In the ROM device, the watchdog parameters can be mask programmed or taken from the SFRs. The selection to take the watchdog parameters from the SFRs or from the mask programmed values is controlled by EA (external access). When EA is high (internal ROM access), the watchdog parameters are taken from the mask programmed values. If the watchdog is mask programmed to the timer mode, then the autoload values and the pre-scaler taps are taken from the SFRs. When EA is low (external access), the watchdog parameters are taken from the SFRs. The user should be able to leave code in his program which initializes the watchdog SFRs even though he has migrated to the mask ROM part. This allows no code changes from EPROM prototyping to ROM coded production parts. The run control bit only functions in timer mode and does not require a feed sequence to modify.

Watchdog Detailed Operation

EPROM Device (and ROMless Operation: EA = 0)

In the ROMless operation (ROM part, EA = 0) and in the EPROM device, the watchdog operates in the following manner (see Figure 15).

Whether the watchdog is in the watchdog or timer mode, when external RESET is applied, the following takes place:

- Watchdog mode bit set to watchdog mode.
- Watchdog is running.
- Autoload register set to 00 (min. count).
- Watchdog time-out flag is unchanged.
- Prescaler is cleared.
- Prescaler tap set to the highest divide.
- Autoload takes place.

The watchdog can be fed even though it is in the timer mode.

Note that the operational concept is for the watchdog mode of operation, when coming out of a hardware reset, the software should load the autoload registers, set the mode to watchdog, clear the watchdog timeout flag, and then feed the watchdog (cause an autoload). The watchdog will now be starting at a known point.

If the watchdog is in the watchdog mode and running and happens to underflow at the time the external RESET is applied, the watchdog time-out flag will be set.

When the watchdog is in the watchdog mode and the watchdog underflows, the following action takes place (see Figure 17):

- Autoload takes place.
- Watchdog time-out flag is set
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.
- All other device action same as external reset.

Note that if the watchdog underflows, the program counter will start from 00H as in the case of an external reset. The watchdog time-out flag can be examined to determine if the watchdog has caused the reset condition. The watchdog time-out flag bit must be cleared by software.

When the watchdog is in the timer mode and the timer software underflows, the following action takes place:

- Autoload takes place.
- Watchdog time-out flag is set
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.

Mask ROM Device (EA = 1)

In the mask ROM device, the watchdog mode bit (WDMOD) is mask programmed and the bit in the watchdog command register is read only and reflects the mask programmed selection. If the mask programmed mode bit selects the timer mode, then the watchdog run bit (WDRUN) operates as described under EPROM Device. If the mask programmed bit selects the watchdog mode, then the watchdog run bit has no effect on the timer operation (see Figure 16).

Watchdog Function

The watchdog consists of a programmable prescaler and the main timer. The prescaler derives its clock from the on-chip oscillator. The prescaler consists of a divide by 2 followed by a 13 stage upcounter with taps from stage 6 through stage 13. This is shown in Figure 18.

The tap selection is programmable. The watchdog main counter is a down counter clocked (decremented) each time the programmable prescaler overflows. The watchdog generates an underflow signal (and is autoloaded) when the watchdog is at count 0 and the prescaler clock decrements the watchdog. The watchdog is 8 bits long and the autoload value can range from 0 to FFH. (The autoload value of 0 is permissible since the prescaler is cleared upon autoload).

This leads to the following user design equations. Definitions :t_{OSC} is the oscillator period, N is the selected prescaler tap value, W is the main counter autoload value, t_{MIN} is the minimum watchdog time-out value (when the autoload value is 0), t_{MAX} is the maximum time-out value (when the autoload value is FFH), t_D is the design time-out value.

$t_{MIN} = t_{OSC} \times 2 \times 64$

$t_{MAX} = t_{MIN} \times 128 \times 256$

$t_D = t_{MIN} \times 2^{PRESCALER} \times (W + 1)$
(where prescaler = 0, 1, 2, 3, 4, 5, 6, or 7)

Note that the design procedure is anticipated to be as follows. A t_{MAX} will be chosen either from equipment or operation considerations and will most likely be the next convenient value higher than t_D. (If the watchdog were inadvertently to start from 00H, an underflow would be guaranteed, barring other anomalies, to occur within t_{MAX}).

The software must be written so that a feed operation takes place every t_D seconds from the last feed operation. Some tradeoffs may need to be made. It is not advisable to include feed operations in minor loops or in subroutines unless the feed operation is a specific subroutine.

Watchdog Control Register (WDCON)
Address C4H
The following bits of this register are read only in the ROM part when $\overline{EA}$ is high: WDMOD, DPD, OFRE, LVRE, PRE0, PRE1, and PRE2. That is, the register will reflect the mask programmed values. In the ROM part with $\overline{EA}$ high, these bits are taken from mask coded bits and are not readable by the program. WDRUN is read only in the ROM part when $\overline{EA}$ is high and WDMOD is in the watchdog mode. When WDMOD is in the timer mode, WDRUN functions normally.

The parameters written into WDMOD, DPD, OFRE, LVRE, PRE0, PRE1, and PRE2 by the program are not applied directly to the watchdog timer subsystem. The watchdog timer subsystem is directly controlled by a second register which stores these bits. The transfer of these bits from the user register to the second control register takes place when the watchdog is fed. This prevents random code execution from directly foiling the watchdog function. This does not affect the operation where these bits are taken from mask coded values.

The reset values of the WDCON and WDL registers will be such that the timer resets to the watchdog mode with a timeout period of $2 \times 64 \times 128 \times t_{OSC}$. The watchdog timer does not generate an interrupt.

Additional bits in WDCON are used to disable reset generation by the oscillator fail and low voltage detect circuits. WDCON can be written by software only by executing a valid watchdog feed sequence.

WDCON Register Bit Definitions

WDCON.7	PRE2	Prescaler Select 2, reset to 1
WDCON.6	PRE1	Prescaler Select 1, reset to 1
WDCON.5	PRE0	Prescaler Select 0, reset to 1
WDCON.4	LVRE	Low Voltage Reset Enable, reset to 1 (enabled)
WDCON.3	OFRE	Oscillator Fail Reset Enable, reset to 1 (enabled)
WDCON.2	DPD	Disable Power Down
WDCON.1	WDRUN	Watchdog Run, reset to 1 (enabled)
WDCON.0	WDMOD	Watchdog Mode, reset to 1 (watchdog mode)

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of this book for the 80C51. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 8XC576 UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 20). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 19.

The serial port transmitter data can be inverted by setting the TXI (AUXR.2) bit. For normal operation, the TXI bit should be cleared.

Automatic Address Recognition
Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 21.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

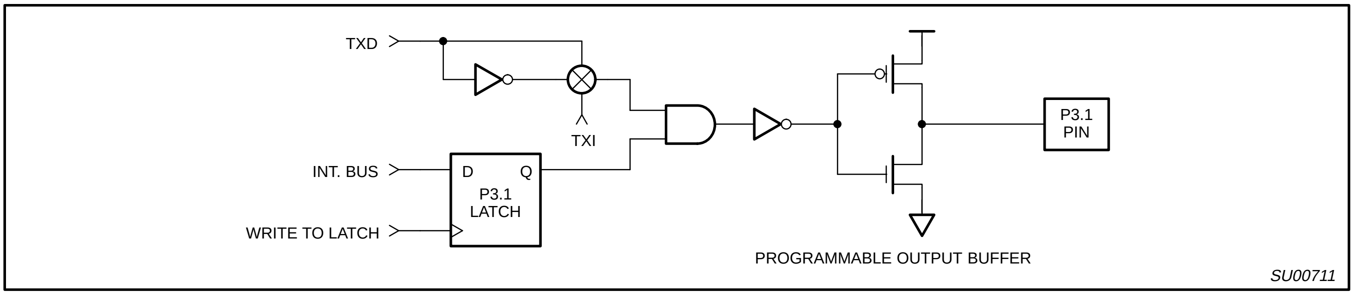


Figure 13. TXI (AUXR.2) Bit Inverts the TxD Pin (P3.1) When Set

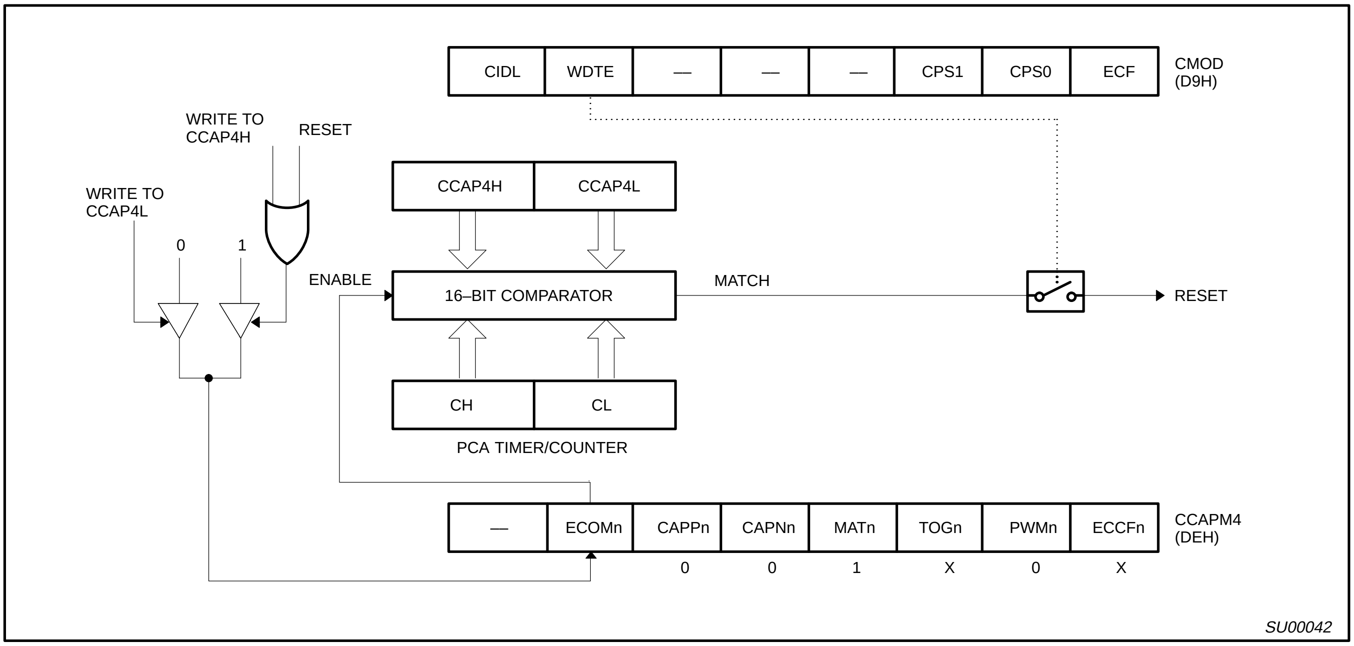


Figure 14. PCA Watchdog Timer

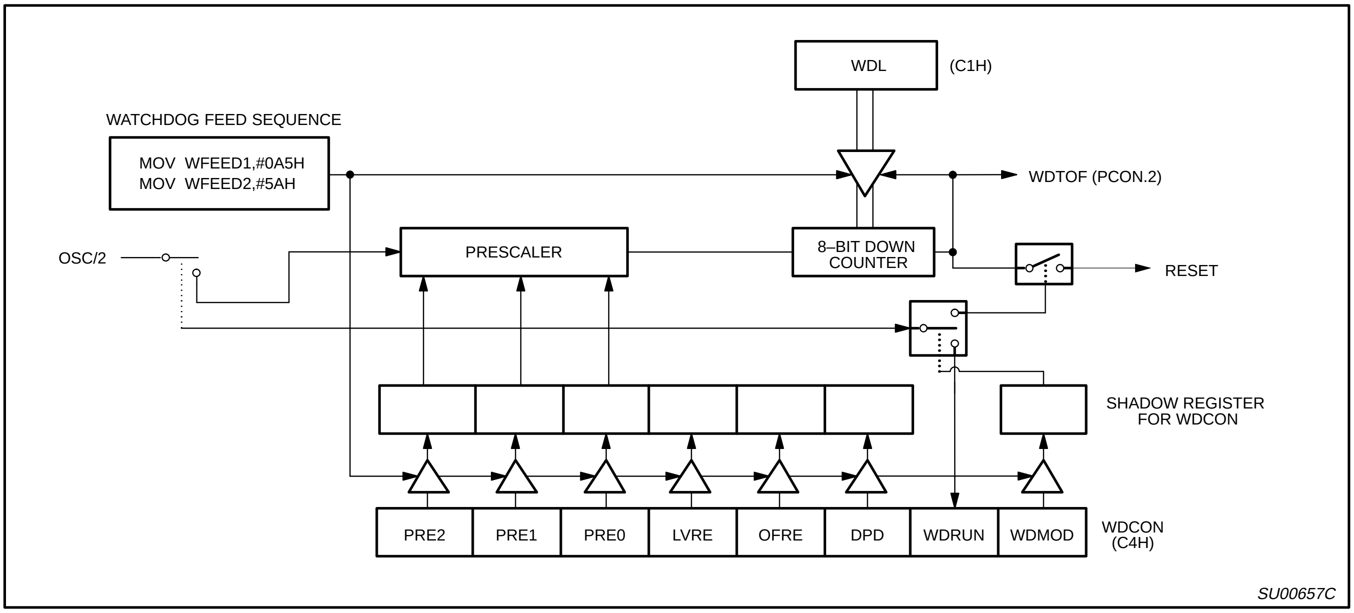


Figure 15. Watchdog Timer in 87C576 and 80C576 / 83C576 ($\overline{EA}$ = 0)

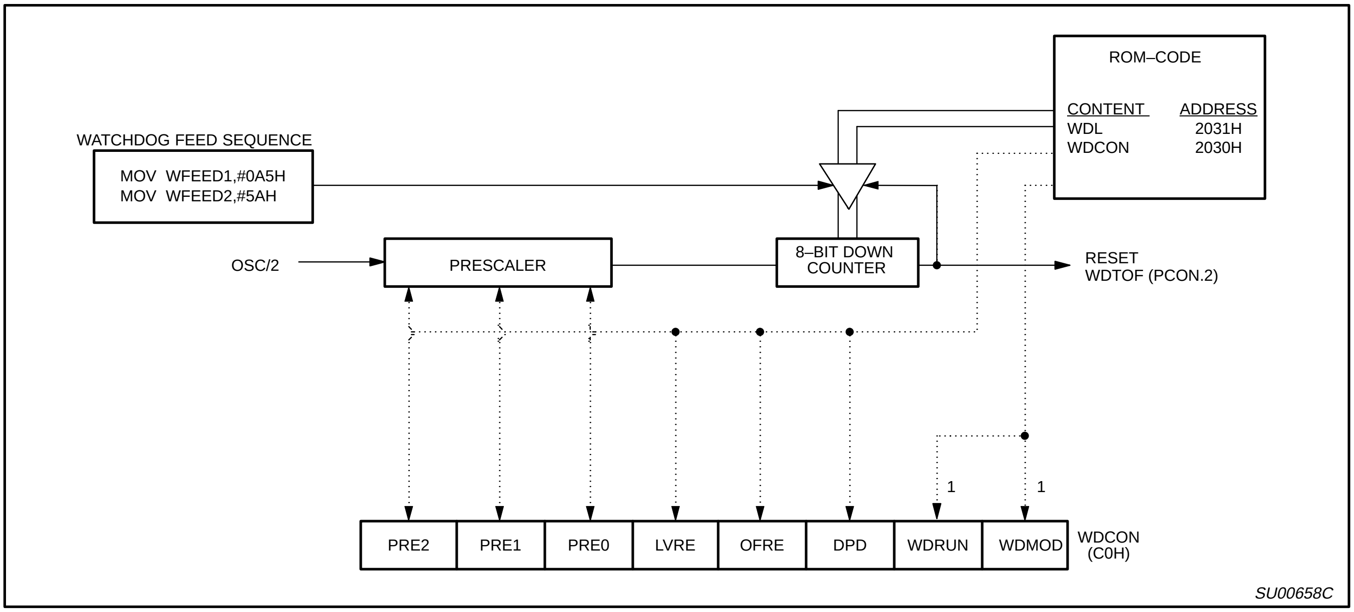


Figure 16. Watchdog Timer of 83C576 in Watchdog Mode ($\overline{EA}$ = 1, WDMOD = 1)

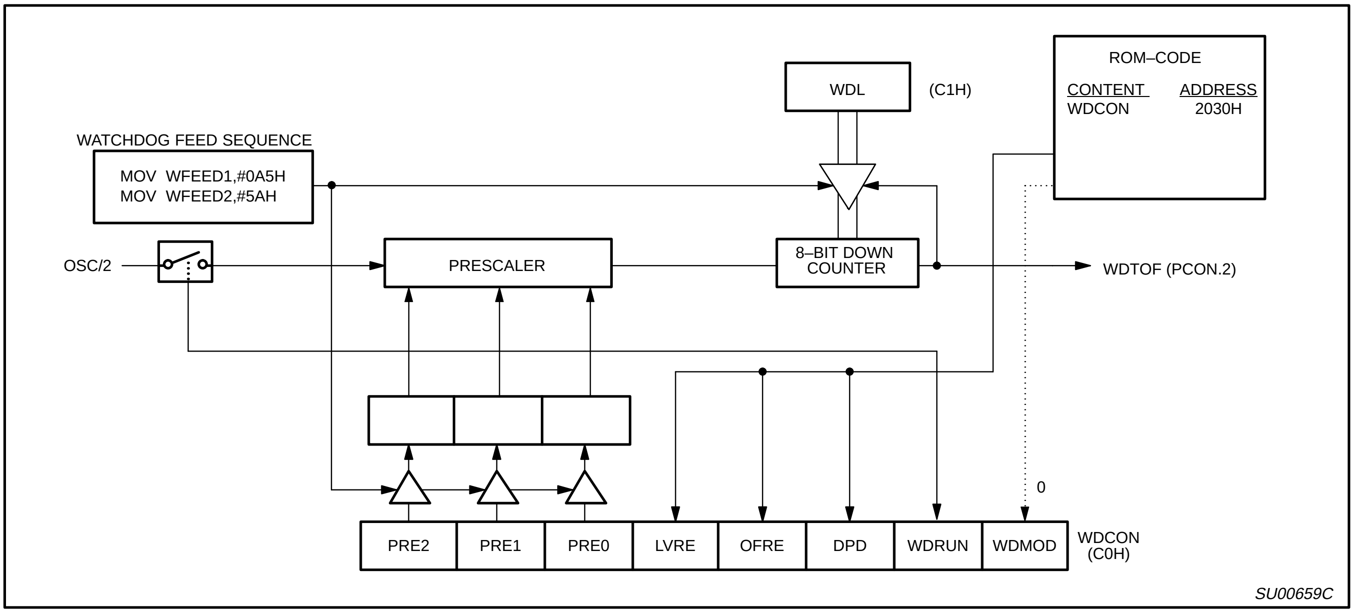


Figure 17. Watchdog Timer of 83C576 in Timer Mode ($\overline{EA}$ = 1, WDMOD = 0)

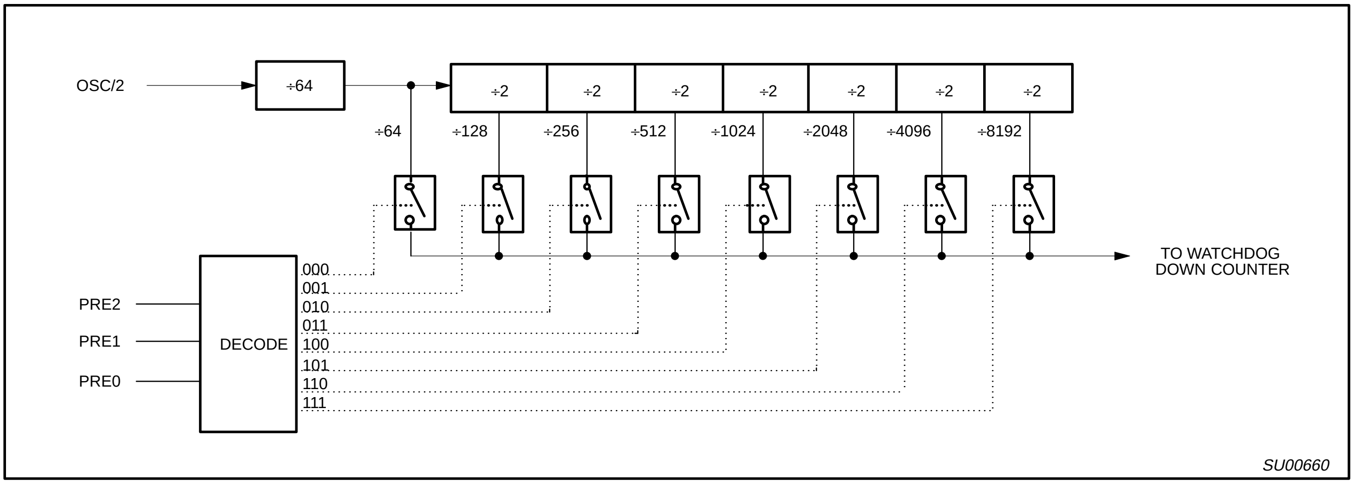


Figure 18. **Watchdog Prescaler**

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**
Bit:	7	6	5	4	3	2	1	0
	(SMOD0/1)*							

Symbol	Function
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	$f_{OSC}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$
1	1	3	9-bit UART	variable

Symbol	Function
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
*SMOD0/1 is located at PCON.6, PCON.7
**f_{OSC} = oscillator frequency

SU00766

Figure 19. **SCON: Serial Port Control Register**

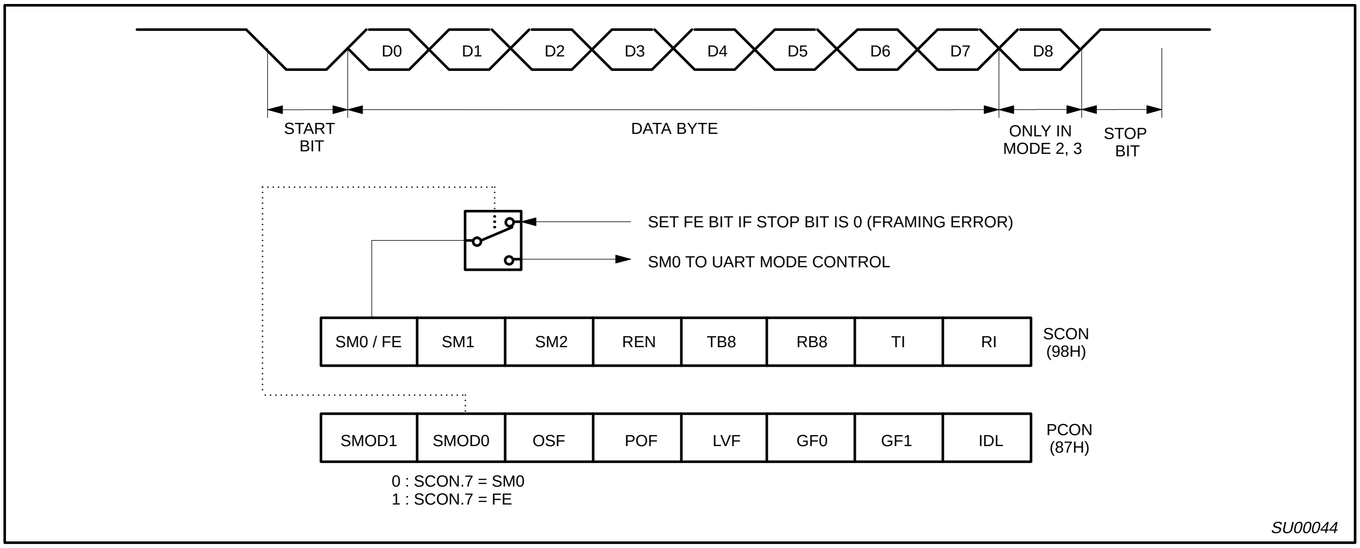


Figure 20. UART Framing Error Detection

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0 SADDR = 1100 0000
SADEN = 1111 1101
Given = 1100 00X0

Slave 1 SADDR = 1100 0000
SADEN = 1111 1110
Given = 1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0

Slave 1 SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X

Slave 2 SADDR = 1110 0000
SADEN = 1111 1100
Given = 1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary t make bit 2 = 1 to exclude slave 2.

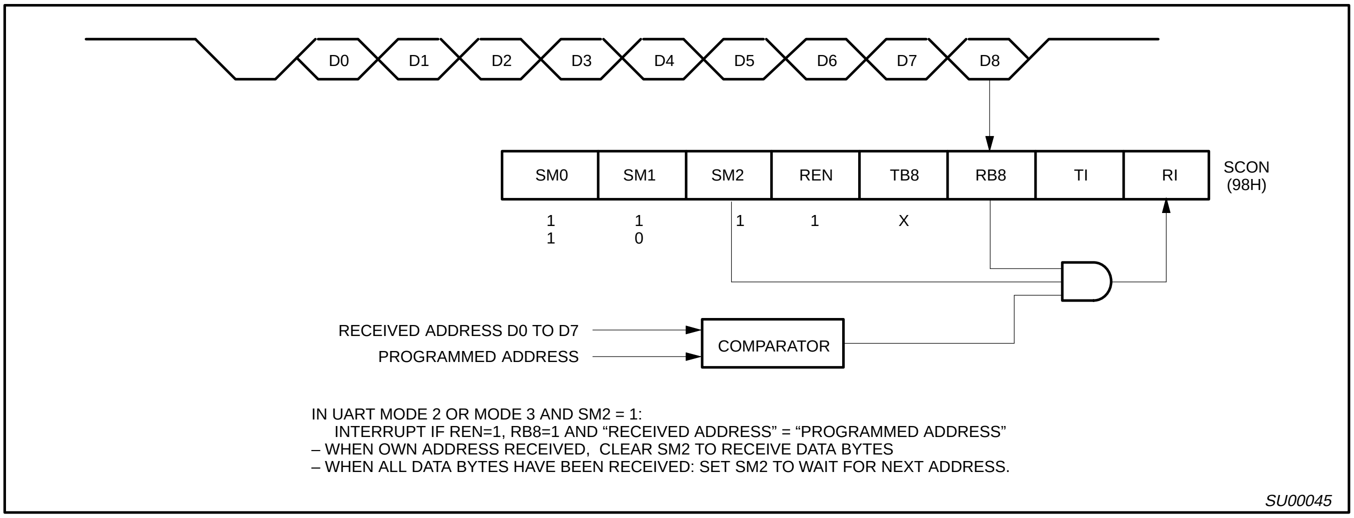
The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". this effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

Analog Comparators

Four analog comparators are provided on chip. Three comparators have a common negative reference CMPR- and independent positive inputs CMP1+, CMP2+, CMP3+ on port 3. The fourth comparator has independent positive and negative inputs CMP0+ and CMP0- on port 2. The CMP register contains an output and enable bit for each comparator. Figure 22 shows the connection of the comparators.

When the comparator is enabled, the port should be configured by the user as high impedance.



IN UART MODE 2 OR MODE 3 AND SM2 = 1:
INTERRUPT IF REN=1, RB8=1 AND “RECEIVED ADDRESS” = “PROGRAMMED ADDRESS”
– WHEN OWN ADDRESS RECEIVED, CLEAR SM2 TO RECEIVE DATA BYTES
– WHEN ALL DATA BYTES HAVE BEEN RECEIVED: SET SM2 TO WAIT FOR NEXT ADDRESS.

Figure 21. UART Multiprocessor Communication, Automatic Address Recognition

CMP Register Bit Definitions

CMP.7	enable comparator 3
CMP.6	enable comparator 2
CMP.5	enable comparator 1,
CMP.4	enable comparator 0
CMP.3	comparator 3 output (read only)
CMP.2	comparator 2 output (read only)
CMP.1	comparator 1 output (read only)
CMP.0	comparator 0 output (read only)

All comparators are disabled automatically in power down mode. In idle mode unused comparators should be disabled by software to save power. A comparator can generate an interrupt that will terminate idle mode when used to drive a PCA capture input.

The CMPE register contains bits to enable each comparator to drive external output pins or internal PCA capture inputs. When the comparator is configured for external output, the user must also configure the output port in one of its output modes. The comparator output is wire-ORed with the corresponding port SFR bit, so the SFR bit must also be set by software to enable the output.

CMPE Register Bit Definitions

CMPE.7	enables comparator 3 to drive CEX3
CMPE.6	enables comparator 2 to drive CEX2
CMPE.5	enables comparator 1 to drive CEX1
CMPE.4	enables comparator 0 to drive CEX0
CMPE.3	enables comparator 3 output on P2.3
CMPE.2	enables comparator 2 output on P2.2
CMPE.1	enables comparator 1 output on P2.1
CMPE.0	enables comparator 0 output on P2.0

When 1s are written to CMPE bits 7-4, the comparator outputs will drive the corresponding capture input. When 1s are written to CMPE bits 3-0 the comparator output will also drive the corresponding port 2 pin. If the comparator’s enabled to drive the capture input but not the port pin, then the port pin can be used for general purpose I/O. When a comparator output is enabled, the user will need to configure the port for one of its output modes.

There are two special function registers associated with the comparators. They are CMP which contains the comparator enables and a bit that can be read by software to determine the state of each comparator’s output, and CMPE which controls whether the output from each comparator drives the associated output pin or a capture input associated with one of the PCA modules.

The CMP registers bits 0–3 can be read by software to determine the state of the output of each comparator. To do this the associated comparator must be enabled but the output in port 2 can be disabled. This allows easy polling of the comparator output value without the need to use up a port pin.

The CMPE register allows the comparator to drive the associated PCA module capture input, so that on compare a capture can be generated in the PCA. Bits 0–3 of this register enable the comparator output to drive the associated port 2 output circuitry. Used as a comparator output, the output mode for this port must be configured for output by the user and the port output SFR bit latch must be set. If the comparator is not enabled to drive the port 2 circuitry, the associated port 2 pin can be used for other I/O. This includes when a comparator is enabled to drive the capture input to a PCA module.

Reduced EMI Mode

There are two bits in the AUXR register that can be set to reduce the internal clock drive and disable the ALE output. AO (AUXR.0) when set turns off the ALE output. LO (AUXR.1) when set reduces the drive of the internal clock circuitry. Both bits are cleared on Reset. With LO set the 8XC576 will still operate at 12MHz, and will have reduced EMI in the range above 100MHz.

8XC576 Reduced EMI Mode

AUXR (0X8E)

—	—	—	—	RST	TXI	LO	AO

AO: Turns off ALE output.

LO: Reduces drive of internal clock circuitry. 8XC576 spec’d to 12MHz when LO set.

TXI: Inverts TxD when set.

RST: Software reset.

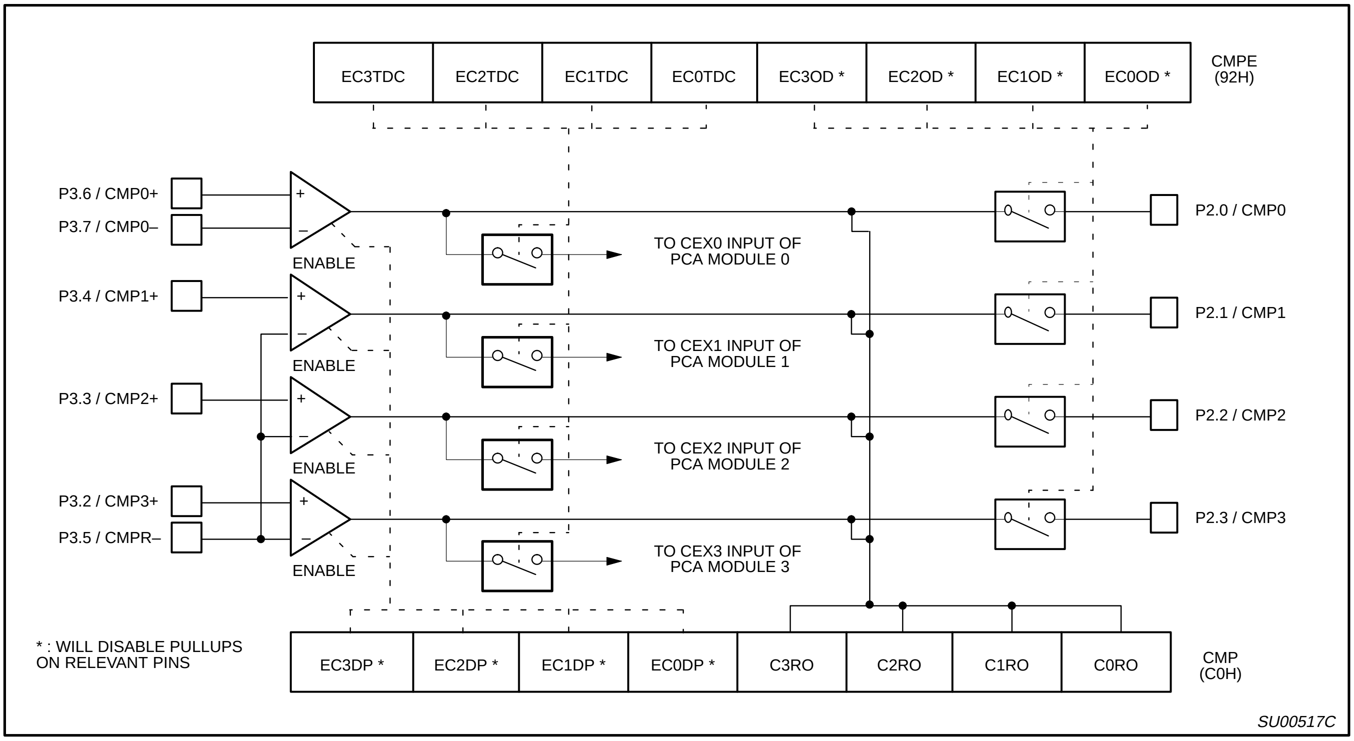


Figure 22. Analog Comparators

INTERNAL RESET

Internal resets (see Figure 1) generated by the power on, low voltage, software (SRST), watchdog and oscillator fail detect circuits are self timed to guarantee proper initialization of the 8XC576. Reset will be held approximately 24 oscillator periods after normal conditions are detected by all enabled detect circuits. Internal resets do not drive $\overline{\text{RST}}$ but will cause missing pulses on ALE.

Analog to Digital Converter

The 8XC576 has a 6 channel10 bit successive approximation A/D converter with separate result registers for each channel. Operating modes are provided for single or multiple channel conversions and multiple conversions of a single channel without software intervention. The ADC can also be operated in 8 bit mode with faster conversion times. Registers ADC0H–ADC5H contain the MSBs and ADC0L–ADC5L bits 6 and 7 contain the 2 LSBs of the conversion result for each channel. The ADCS register determines which channels are converted in multiple channel modes. If the ADCS bit corresponding to a channel is set, that channel is converted, else if the bit is clear the channel is skipped.

A/D Channel Select (ADCS) Register (Reset Value = 00H)

ADCS5	ADCS.5 – A/D channel 5 select bit
ADCS4	ADCS.4 – A/D channel 4 select bit
ADCS3	ADCS.3 – A/D channel 3 select bit
ADCS2	ADCS.2 – A/D channel 2 select bit
ADCS1	ADCS.1 – A/D channel 1 select bit
ADCS0	ADCS.0 – A/D channel 0 select bit

A/D Control (ADCON) Register (Reset Value = 00H)

ADF	ADCON.7 – A/D conversion complete flag
ADCE	ADCON.6 – A/D conversion enable
AD8M	ADCON.5 – A/D 8-bit mode
AMOD1	ADCON.4 – A/D mode select bit 1
AMOD0	ADCON.3 – A/D mode select bit 0
ASCA2	ADCON.2 – A/D channel address bit 2
ASCA1	ADCON.1 – A/D channel address bit 1
ASCA0	ADCON.0 – A/D channel address bit 0

AMOD1	**AMOD0**	
0	0	Single Conversion Mode – channel selected by bits ASCA2..0 in ADCON is converted, the result placed in the associated result registers; ADF is set on completion.
0	1	Mulitple Channel Scan Mode – all channels selected in the ADCS register are converted starting with the channel addressed by bits ASCA2..0 in ADON, conversion results are placed in the corresponding result registers for each channel. ADF is set when the last conversion is completed.
1	0	Single Channel Multiple Conversion – channel selected by bits ASCA2..0 in ADCON is converted 6 times and all 6 results are saved in ADC0H–ADC5H and ADC0L–ADC5L, ADF is set when all conversions are complete.
1	1	Multiple Channel Continuous – same as Multiple Channel Scan mode but repeats as long as ADCE=1, ADF is set when all channels have been converted once. Hardware will prevent the ADC from wiriting to the result registers while they are being read.

Flag ADF is set upon completion of a conversion, if the ADC interrupt enable bit EAD is set, the program will vector to the ADC interrupt location when ADF is set.

PWMs

The pulse width modulator system of the 8XC576 contains two PWM output channels. These channels generate pulses of programmable length and interval. The prescaler and counter are common to both PWM channels.

The prescaler is loaded with the complement of the PWMP register during counter overflow, internal reset, and when EN/CLR# = 0. The repetition frequency is defined by the 8-bit prescaler which clocks the counter. The prescaler division factor = PWMP+1. Reading the PWMP gives the current reload value. The actual count of the prescaler cannot be read.

The 8-bit counter counts from 0–254 inclusive. The value of the counter is compared to the contents of the compare registers PWM0 and PWM1. When the counter compares to the compare register, that register's output goes LOW. When the counter reaches zero the output is set HIGH unless PWMn = 00H. The duty cycle of each channel is defined by the contents of its compare register and is in the range of 0 to 1, programmed in increments of 1/255.

The outputs can be set continuously low by loading PWMn with 00H and continuously high by loading with FFH.

The PWM counter is enabled with bit EN/CLR# of the PWCON register. Output to the port pin is separately enabled by setting the PWEn bits in the PWCON register. The counter remains active if EN/CLR# is set even if both PWEn bits are reset. The PWM function is reset by a chip reset. In idle mode, the PWM will function as configured by PWCON. In power-down the state of the PWM will freeze when the internal clock stops. If the chip is awakened with an external interrupt, the PWM will continue to function from its state when power-down was entered. The EN/CLR# bit of PWCON will clear the counter and load the contents of the PWMP into the prescaler when set LOW. If PWEn is set at this time the output will go HIGH unless PWMn is 00H.

The repetition frequency is given by:

$$f_{PWM} = \frac{f_{OSC}}{(510 \times (1 + PWMP))}$$

An oscillator frequency of 12MHz results in a repetition range of 92Hz to 23.5KHz.

The high/low ratio of PWMn is PWMn/(255–PWMn) for PWMn values except 255. A PWMn value of 255 results in a high PWMn output.

In order for the PWMn output to be used as a standard I/O pin, PWMn must be reset. The PWM counter can still be used as an internal timer by setting EN/CLR#.

Pulse Width Modulator Control Register Bit Definitions (PWCON = BCH)

PWMF	PWCON.3	Counter overflow flag, must be cleared by software
EN/$\overline{\text{CLR}}$	PWCON.2	Counter enable and counter/prescaler reset when Low
PWE1	PWCON.1	PWM1 output to P2.7 pin enable
PWE0	PWCON.0	PWM0 output to P2.6 pin enable

Auxiliary Register Bit Definitions (AUXR =8EH)

RST	AUXR.3	Software reset bit
TXI	AUXR.2	SIO TxD invert
LO	AUXR.1	Low Speed, reduces internal clock drive
AO	AUXR.0	ALE Off, when set turns off ALE

Interrupt Enable 0 (IE0) Register

EA	IE0.7	Enable all interrupts
EC	IE0.6	Enable PCA interrupt
ET2	IE0.5	Enable Timer 2 interrupt
ES	IE0.4	Enable Serial I/O interrupt
ET1	IE0.3	Enable Timer 1 interrupt
EX1	IE0.2	Enable External interrupt 1
ET0	IE0.1	Enable Timer 0 interrupt
EX0	IE0.0	Enable External interrupt 0

Interrupt Enable 1 (IE1) Register

EOB	IE1.7	Enable OBE interrupt
EIB	IE1.6	Enable IBF interrupt
EAD	IE1.5	Enable ADC interrupt
EC4	IE1.4	Enable PCA module 4 interrupt
EC3	IE1.3	Enable PCA module 3 interrupt
EC2	IE1.2	Enable PCA module 2 interrupt
EC1	IE1.1	Enable PCA module 1 interrupt
EC0	IE1.0	Enable PCA module 0 interrupt

Interrupt Priority 0 (IP0) Register

	IP0.7	(reserved)
PPC	IP0.6	PCA interrupt priority
PT2	IP0.5	Timer 2 interrupt priority
PS	IP0.4	Serial I/O interrupt priority
PT1	IP0.3	Timer 1 interrupt priority
PX1	IP0.2	External interrupt 1 priority
PT0	IP0.1	Timer 0 interrupt priority
PX0	IP0.0	External interrupt 0 priority

Interrupt Priority 1 (IP1) Register

POB	IP1.7	OBE interrupt priority
PIB	IP1.6	IBF interrupt priority
PAD	IP1.5	ADC interrupt priority
PC4	IP1.4	PCA module 4 interrupt priority
PC3	IP1.3	PCA module 3 interrupt priority
PC2	IP1.2	PCA module 2 interrupt priority
PC1	IP1.1	PCA module 1 interrupt priority
PC0	IP1.0	PCA module 0 interrupt priority

Priority	Source	Flag	Vector	
1	INT0	IE0	03H	highest priority
2	ADC	ADF	3BH	
3	TIMER 0	TF0	0BH	
4	INT1	IE1	13H	
5	TIMER 1	TF1	1BH	
6	SERIAL	RI,TI	23H	
7	PCA0	CC0	43H	
8	PCA1	CC1	4BH	
9	PCA2	CC2	53H	
10	PCA3	CC3	5BH	
11	PCA4	CC4	63H	
12	PCA	ECF	33H	
13	TIMER 2	TF2/EXF2	2BH	
14	UPI	IBF	6BH	
15	UPI	OBE	73H	lowest priority

Power Control (PCON) Register

SMOD1	PCON.7	double baud rate bit
SMOD0	PCON.6	SCON.7 access control
OSF	PCON.5	oscillator fail flag
POF	PCON.4	power off flag
LVF	PCON.3	low voltage flag
WDTOF	PCON.2	watchdog timeout flag
PD	PCON.1	power down mode bit
IDL	PCON.0	idle mode bit

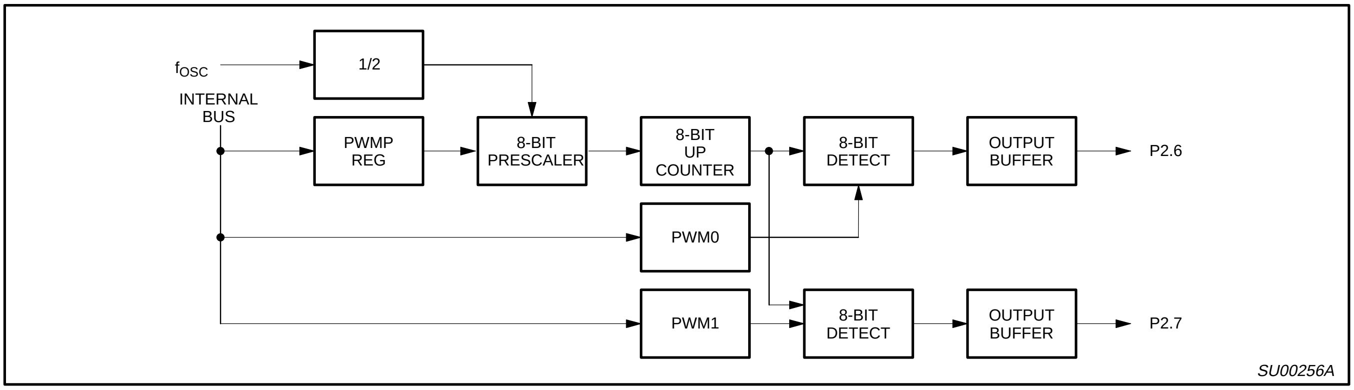


Figure 23. Block Diagram of PWMs

UNIVERSAL PERIPHERAL INTERFACE

UPI mode allows the 8XC576 to function as a slave processor connected to a host CPU bus via port 0. The interface consists of port 0 input and output buffer registers and the UPI control/status register (UCS). UPI mode is enabled by setting the UPI enable bit (UE) in the UCS. When operating in UPI mode, port 0 pins should be programmed to High-Z (P0M1=1 and P0M2=0) by user firmware. Access to port 0 is controlled by inputs $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{CS}}$, and A0. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are the external read and write strobes controlled by the host CPU. $\overline{\text{CS}}$ is the chip select input, normally a decoded address from the host CPU bus, which qualifies $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (these pins have no effect when $\overline{\text{CS}}$=1). The A0 pin is an address input from the host CPU which selects either the port 0 output buffer or the UCS register to be output during a read operation. During a write operation, the value of the A0 pin is latched in the AF flag in the UCS register. The following is a summary of the UPI data control inputs:

$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{A0}}$	
0	0	1	0	read port 0 output buffer, clear OBF/set OBE
0	0	1	1	read UPI control/ status register
0	1	0	0	write data to input buffer set IBF, clear AF
0	1	0	1	write command to input buffer set IBF, AF
1	x	x	x	disable input/output

UPI Control Status Register (UCS, Reset value = 00H)

UCS.7	ST7	User defined status bit
UCS.6	ST6	User defined status bit
UCS.5	ST5	User defined status bit
UCS.4	ST4	User defined status bit
UCS.3	UE	UPI Enable bit – if UE=1, UPI is enabled (read only AF, IBF, and OBE/OBF), if UE=0, UPI is disabled and port 0 functions normally.
UCS.2	AF	Address Flag – contains status of the A0 (address) pin during the last write. If A0=0, the input buffer should be interpreted as data by the 8XC576 software, if A0=1, the input buffer should be interpreted as a command.
USC.1	IBF	Input Buffer Full flag – set by hardware on trailing (rising) edge of $\overline{\text{WR}}$ when $\overline{\text{CS}}$=0, cleared by hardware when port 0 SFR is read (by the 8XC576 software).
USC.0	OBE/OBF	Output Buffer Full flag – set by hardware during writes (by 8XC576 software) to the port 0 SFR, set/cleared by hardware on the trailing (rising) edge of $\overline{\text{RD}}$ when $\overline{\text{CS}}$=0 and A0=0.

NOTE: This bit is defined as OBE (1=empty) when read by the MCU, and, as OBF (—full) when read by the external host.

The IBF and OBF flag bits reflect the status of the input/output buffers. The host CPU writes to the 8XC576 by driving data on the external bus connected to port 0 and strobing the $\overline{\text{WR}}$ pin while $\overline{\text{CS}}$=0. The $\overline{\text{WR}}$ strobe latches port 0 data in the input buffer and sets the IBF flag on the trailing (rising) edge. When the 8XC576 reads from port 0 in UPI mode, it reads from the input buffer and clears the IBF. When the 8XC576 writes to port 0 in UPI mode, it writes to the output buffer which sets the OBF and clears the OBE flag. The host CPU can read the output buffer or the UCS register enabling the port 0 drivers, the OBF flag is cleared and the OBE flag is set when the output buffer is read.

When the UPI is enabled, the AF, IBF, and OBE/OBF flags are read-only, and thus can only be modified by specific hardware events.

The UPI runs in idle mode. It can interrupt the part out of Idle mode for all UPI write and data read operations. It will not interrupt out of idle mode for a UCS register read operation.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol, page 3-758.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset. Also see UPI section.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. The control bits for the reduced power modes are in the special function register PCON. Power-down mode can be terminated with either a hardware reset or external interrupt. With an external interrupt $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ must be enabled and configured as level sensitive. Holding the pin low restarts to oscillator and bringing the pin back high completes the exit.

Power-down mode can be disabled by the DPD bit in the WDCON register. Reset and waking up from power-down will also enable the DPD bit, therefore, the DPD bit must be cleared again before the power-down mode.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} must come up with $\overline{\text{RST}}$ low for a proper start-up.

Table 2 shows the state of I/O ports during low current operating modes.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{\text{PSEN}}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ROM CODE SUBMISSION

When submitting ROM code for the 83C576, the following must be specified:

1. 8k byte user ROM data
2. 32 byte ROM encryption key
3. ROM security bits
4. The watchdog timer parameters. (See Watchdog Timer Specifications for definition of WDL and WDCON bits.)

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 1FFFH	DATA	7:0	User ROM Data
2000H to 201FH	KEY	7:0	ROM Encryption Key FFH = no encryption
2020H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
		1	ROM Security Bit 2 0 = enable security 1 = disable security
2030H	WDCON	7:5	PRE2:0
		4	LVRE
		3	OFRE
		2	DPD
		1	WDRUN = 0, not ROM coded
		0	WDMOD
2031H	WDL	7:0	Watchdog autoload value (see specification)

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. $\overline{EA}$ is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

If the ROM code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

Watchdog/Timer Modes: ☐ Watchdog Mode ☐ Timer Mode

Prescaler Value: ☐ (Value = 64, 128, 256, 512, 1024, 2048, 4096, 8192)
Value

Autoload Value (range 0–255): ☐

Low Voltage Reset (Value 0 or 1): ☐

Oscillator Fail Reset (Value 0 or 1): ☐

Power-Down (Value 0 or 1): ☐

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, –40°C to +85°C, and –40°C to +125°C; V_{CC} = 5V ±10%, V_{SS} = 0V

		TEST	**LIMITS**			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**[1]	**MAX**	**UNIT**
V_{IL}	Input low voltage (except Port 1, $\overline{EA}$)		–0.5		$0.2V_{CC}$–0.1	V
V_{IL1}	Input low voltage ($\overline{EA}$)		–0.5		$0.2V_{CC}$–0.45	V
V_{IL2}	Input low voltage (Port 1)		–0.5		$0.3V_{CC}$	V
V_{IH}	Input high voltage (except Port 1, XTAL1, RST)	I_{IH} < 2mA	$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage (XTAL1, RST, Port 1)	I_{IH} < 2mA	$0.7V_{CC}$		V_{CC}+0.5	V
HYS	Hysteresis voltage (Port 1)		200			mV
V_{OL}	Output voltage low (Ports 1, 2, 3)	I_{OL} = 1.6mA			0.45	V
V_{OL1}	Output voltage low (Ports 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2mA			0.45	V
V_{OH}	Output voltage high (Ports 1, 2, 3 in push-pull mode)	I_{OH} = –1.6mA	V_{CC}–1.0			V
V_{OH1}	Output voltage high (Port 0, ALE, $\overline{PSEN}$)	I_{OH} = –3.2mA	V_{CC}–0.7			V
V_{OH2}	Output voltage high in weak pullup mode (Port 0, 2, 3)	I_{OH} = –10µA	V_{CC}–1.0			V
V_{IO}	Offset voltage comparator inputs		–35		+35	mV
V_{CR}	Common mode range comparator inputs		0		V_{CC}	V
I_{IL}	Logical 0 input current (Ports 0, 2, 3) (weak pull-up)	V_{IN} = 0.45V			–250	µA
I_{IH}	Input pulldown current (Port 0, Port2 in open drain mode)	0.45 < V_{IN} < V_{CC}	2		40	µA
I_{L2}	Input leakage current ($\overline{EA}$, P0. 2. 3 High-Z)	0.45 < V_{IN} < V_{CC}	–10		+10	µA
I_{LA}	Input leakage current comparator/ADC inputs	0 < V_{IN} < V_{CC}	–1.0		+1.0	µA
I_{CC}	Power supply current:[7] Active mode @ 16MHz[5] Idle mode @ 16MHz Power-down mode	See note 6		 20 8 5	 30 12 75	 mA mA µA
R_{RST}	Internal reset pull-up resistor	V_{IN} = 0V	50		200	kΩ
V_{LOW}	Low V_{CC} detect voltage		3.75		4.25	V
C_{IO}	Pin capacitance[9]	f = 1MHz			15	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is between V_{IH} and V_{IL}.
5. I_{CC}MAX at other frequencies can be determined from Figure 33.
6. See Figures 34 through 37 for I_{CC} test conditions.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:	10mA
Maximum I_{OL} per 8-bit port:	26mA
Maximum total I_{OL} for all outputs:	71mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

9. 20pF MAX for CERDIP package; 15pF MAX for all other packages.

A/D CONVERTER DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, –40°C to +85°C, and –40°C to +125°C; V_{CC} = 5V ±10%, V_{SS} = 0V

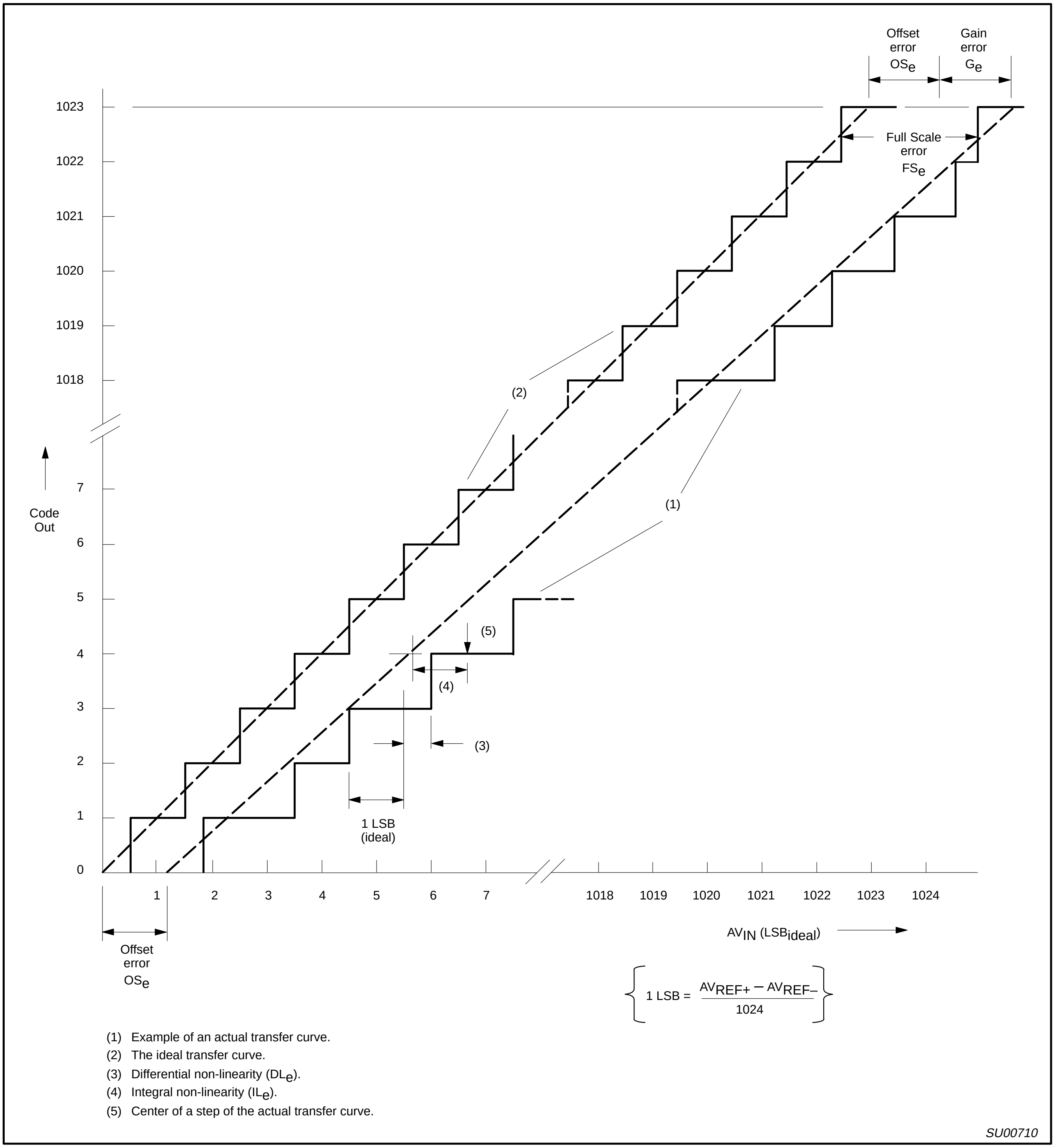
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Static Characteristics					
R	Resolution	Monotonic with no missing codes	10		Bits
IL_e	Integral non-linearity error [2, 5, 8]			±2	LSB
DL_e	Differential non-linearity error[2, 3, 4, 7, 8]			±1	LSB
FS_e	Full Scale error [2, 8]			±3	LSB
OS_e	Offset error [2, 6, 8]			±2	LSB
Dynamic Characteristics					
t_{ADC}	Conversion time (including sampling time)			$48t_{CY}$	µs
t_{ADS}	Sampling tme			$8t_{CY}$	µs
Analog Input Characteristics					
AV_{IN}	Analog input voltage		AV_{SS} – 0.2	AV_{DD} + 0.2	V
C_{IA}	Analog input capacitance			15	pF
M_{CTC}	Channel-to-channel matching[7]			±1	LSB
C_t	Crosstalk between inputs of port 1[7]	0–100kHz		–60	dB
Power Requirements					
AV_{CC}/V_{REF+}	Analog supply and reference voltage	$AV_{CC} = V_{CC} \pm 0.2$	4.0	6.0	V
AI_{CC}	Analog supply current: operating: (16MHz)	AV_{CC} = 6.0V		1.2	mA

NOTES:

1. The following condition must not be exceeded: $V_{DD} - 0.2V < AV_{DD} < V_{DD} + 0.2V$.
2. Conditions: AV_{SS} = 0V; AV_{CC} = 4.997V; V_{CC} = 5.0V.
3. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. (See Figure 24).
4. The ADC is monotonic; there are no missing codes.
5. The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 24).
6. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 24).
7. Guaranteed by design.
8. To meet Error Specification, analog input voltage must be less than 1V/ms.

$$\text{Slew Rate}_{MAX} = \frac{(AV_{CC}/1023) \times 1000}{4 \times (12/\text{Osc Freq (MHz)})} \quad (V/ms)$$

For 16MHz @ 5.0V slew rate = 1.6V/ms.



$$\left\{ 1\ \text{LSB} = \frac{AV_{REF+} - AV_{REF-}}{1024} \right\}$$

(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity (DL_e).
(4) Integral non-linearity (IL_e).
(5) Center of a step of the actual transfer curve.

Figure 24. ADC Conversion Characteristic

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, –40°C to +85°C, and –40°C to +125°C; V_{CC} = 5V ±10%, V_{SS} = 0V[1, 2]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK		UNIT
			MIN	MAX	
1/t_{CLCL}	25	Oscillator frequency: **Speed Version** 8XC576 E	6	16	MHz
OSCF		Oscillator fail detect frequency	0.6	5.5	MHz
TR		Comparator response time		10	µs
t_{LHLL}	25	ALE pulse width	2t_{CLCL}–40		ns
t_{AVLL}	25	Address valid to ALE low	t_{CLCL}–40		ns
t_{LLAX}	25	Address hold after ALE low	t_{CLCL}–30		ns
t_{LLIV}	25	ALE low to valid instruction in		4t_{CLCL}–100	ns
t_{LLPL}	25	ALE low to $\overline{\text{PSEN}}$ low	t_{CLCL}–30		ns
t_{PLPH}	25	$\overline{\text{PSEN}}$ pulse width	3t_{CLCL}–45		ns
t_{PLIV}	25	$\overline{\text{PSEN}}$ low to valid instruction in		3t_{CLCL}–105	ns
t_{PXIX}	25	Input instruction hold after $\overline{\text{PSEN}}$	0		ns
t_{PXIZ}	25	Input instruction float after $\overline{\text{PSEN}}$		t_{CLCL}–25	ns
t_{AVIV}	25	Address to valid instruction in		5t_{CLCL}–105	ns
t_{PLAZ}	25	$\overline{\text{PSEN}}$ low to address float		10	ns
Data Memory					
t_{RLRH}	26, 27	$\overline{\text{RD}}$ pulse width	6t_{CLCL}–100		ns
t_{WLWH}	26, 27	$\overline{\text{WR}}$ pulse width	6t_{CLCL}–100		ns
t_{RLDV}	26, 27	$\overline{\text{RD}}$ low to valid data in		5t_{CLCL}–165	ns
t_{RHDX}	26, 27	Data hold after $\overline{\text{RD}}$	0		ns
t_{RHDZ}	26, 27	Data float after $\overline{\text{RD}}$		2t_{CLCL}–60	ns
t_{LLDV}	26, 27	ALE low to valid data in		8t_{CLCL}–150	ns
t_{AVDV}	26, 27	Address to valid data in		9t_{CLCL}–165	ns
t_{LLWL}	26, 27	ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low	3t_{CLCL}–50	3t_{CLCL}+50	ns
t_{AVWL}	26, 27	Address valid to $\overline{\text{WR}}$ low or $\overline{\text{RD}}$ low	4t_{CLCL}–130		ns
t_{QVWX}	26, 27	Data valid to $\overline{\text{WR}}$ transition	t_{CLCL}–50		ns
t_{WHQX}	26, 27	Data hold after $\overline{\text{WR}}$	t_{CLCL}–50		ns
t_{RLAZ}	26, 27	$\overline{\text{RD}}$ low to address float		0	ns
t_{WHLH}	26, 27	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to ALE high	t_{CLCL}–40	t_{CLCL}+40	ns
External Clock					
t_{CHCX}	29	High time	20		ns
t_{CLCX}	29	Low time	20		ns
t_{CLCH}	29	Rise time		20	ns
t_{CHCL}	29	Fall time		20	ns
Shift Register					
t_{XLXL}	28	Serial port clock cycle time	12t_{CLCL}		ns
t_{QVXH}	28	Output data setup to clock rising edge	10t_{CLCL}–133		ns
t_{XHQX}	28	Output data hold after clock rising edge	2t_{CLCL}–60		ns
t_{XHDX}	28	Input data hold after clock rising edge	0		ns
t_{XHDV}	28	Clock rising edge to input data valid		10t_{CLCL}–133	ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{\text{PSEN}}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the 83C576/87C576 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

UPI AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, –40°C to +85°C, and –40°C to +125°C; V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AR}	$\overline{\text{CS}}$, A setup to $\overline{\text{RD}}$	0		ns
t_{RA}	$\overline{\text{CS}}$, A hold after $\overline{\text{RD}}$	35		ns
t_{RR}	$\overline{\text{RD}}$ pulse width	35		ns
t_{AD}	$\overline{\text{CS}}$, A to data out delay		45	ns
t_{RD}	$\overline{\text{RD}}$ to data out delay		35	ns
t_{DF}	$\overline{\text{RD}}$ to data float delay (guaranteed by design)		30	ns
t_{AW}	$\overline{\text{CS}}$, A setup to $\overline{\text{WR}}$	0		ns
t_{WA}	$\overline{\text{CS}}$, A hold after $\overline{\text{WR}}$	15		ns
t_{WW}	$\overline{\text{WR}}$ pulse width	45		ns
t_{DW}	Data setup to $\overline{\text{WR}}$	5		ns
t_{WD}	Data hold after $\overline{\text{WR}}$	25		ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

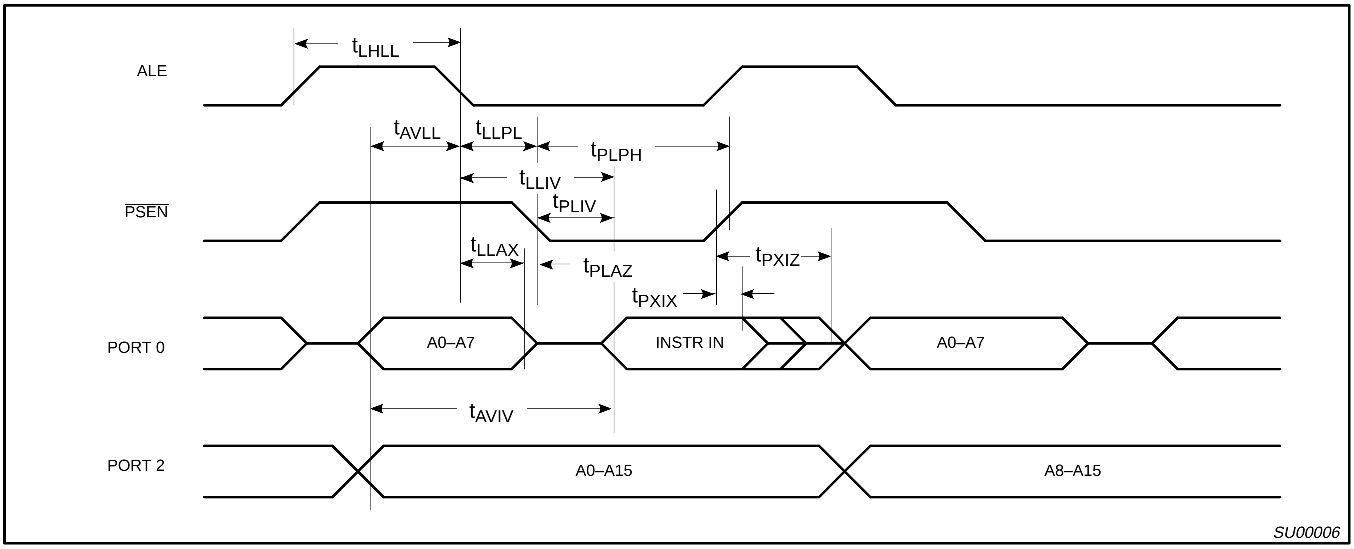


Figure 25. External Program Memory Read Cycle

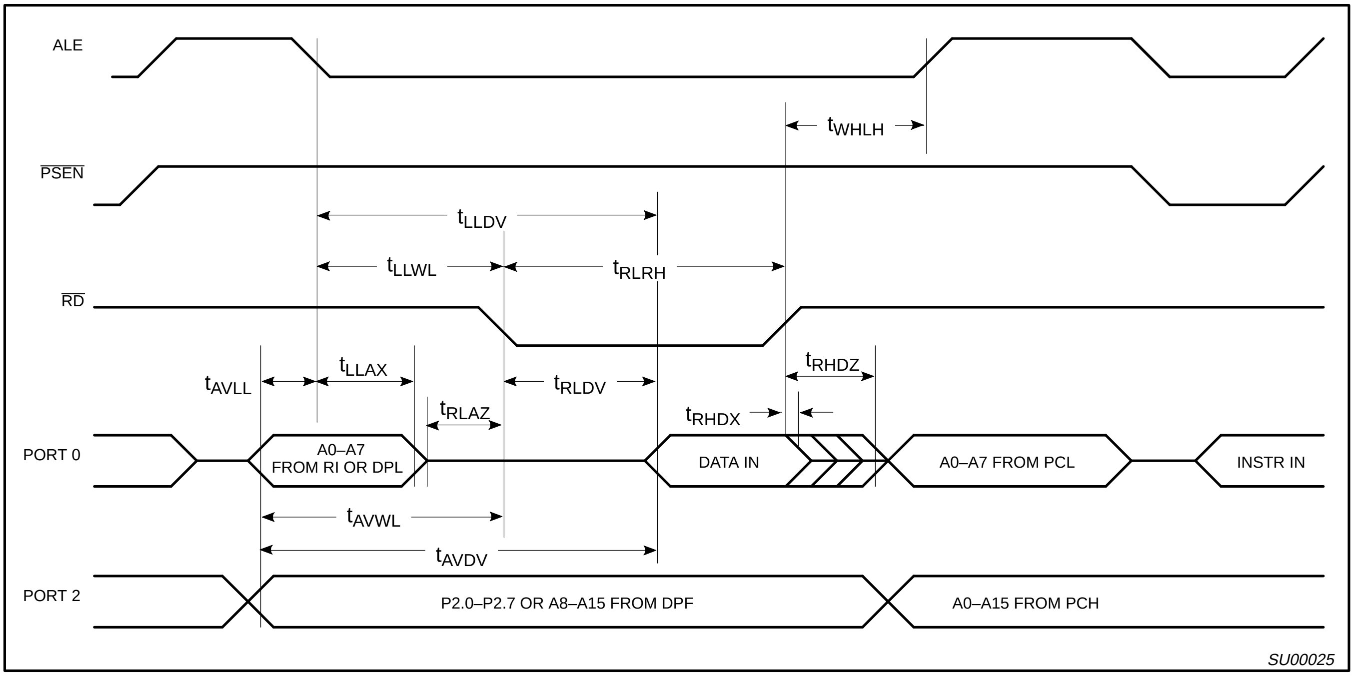


Figure 26. External Data Memory Read Cycle

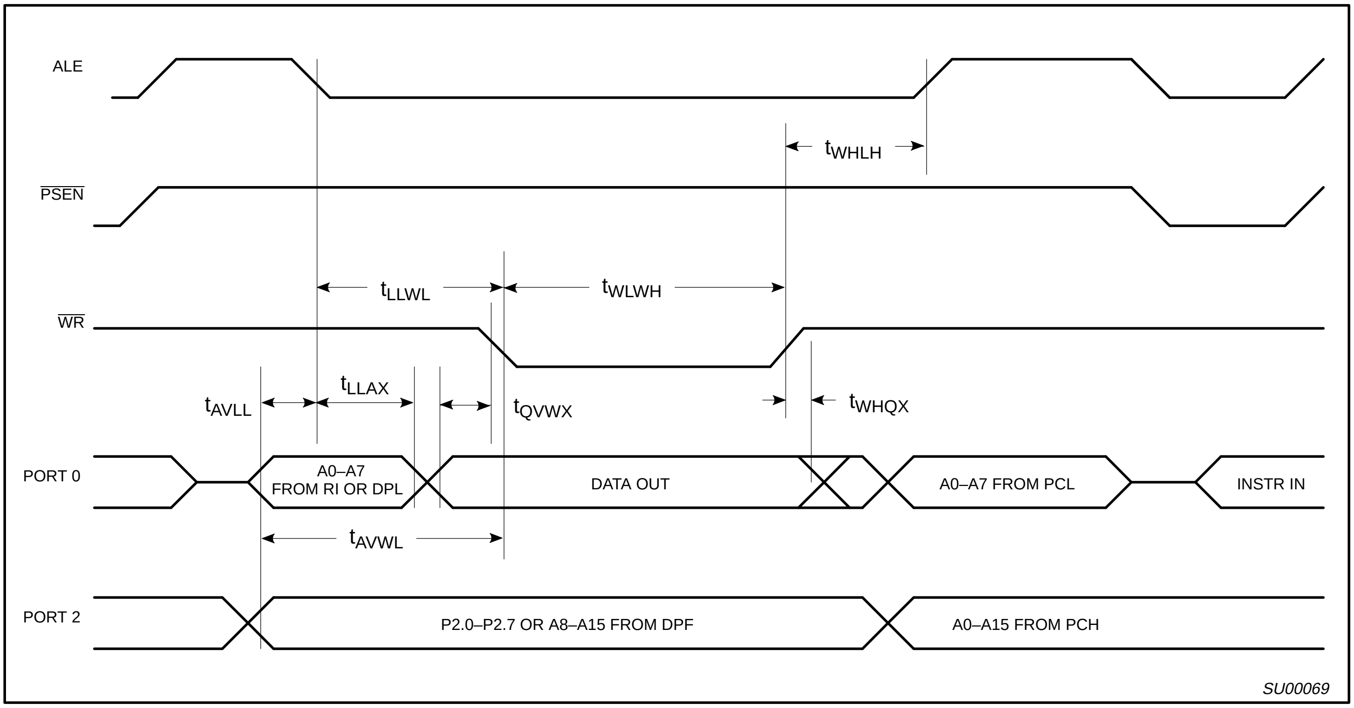


Figure 27. External Data Memory Write Cycle

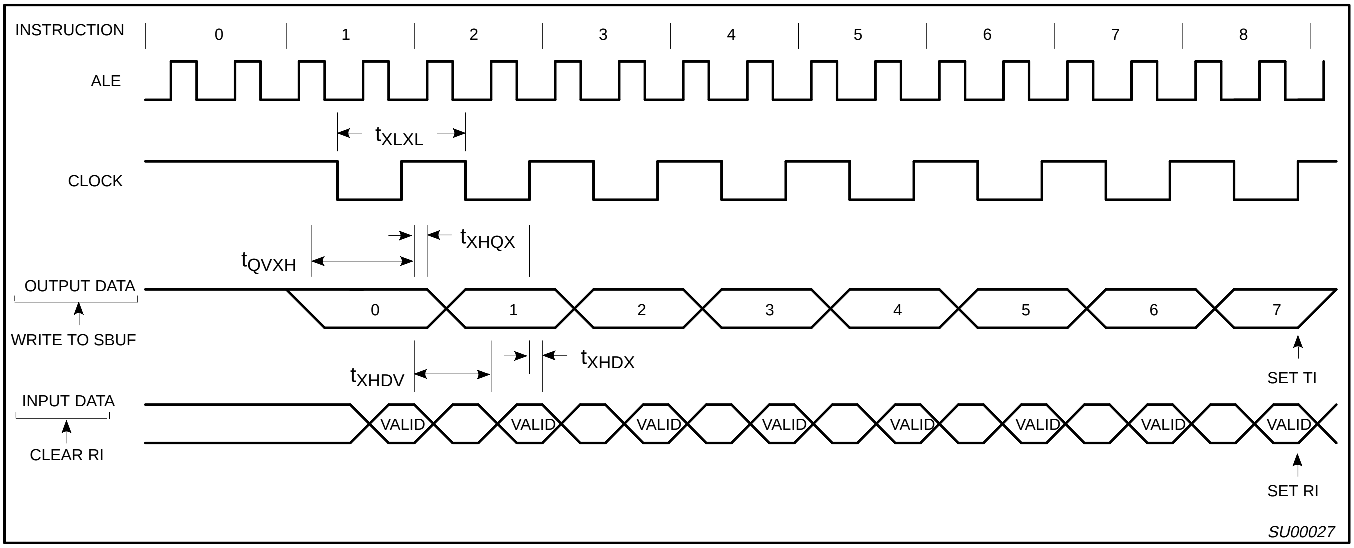


Figure 28. Shift Register Mode Timing

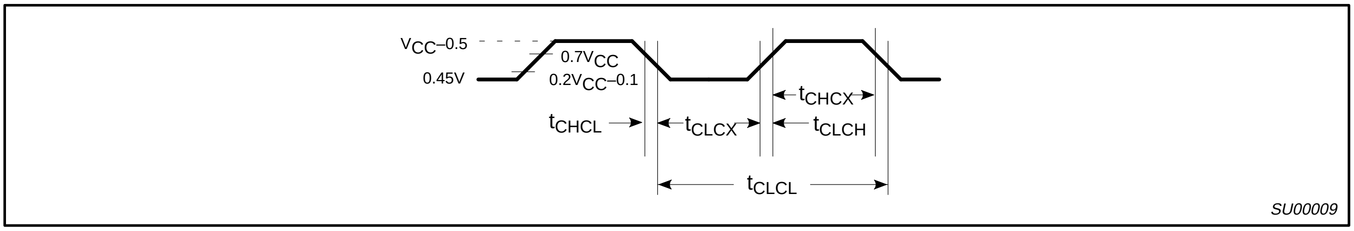
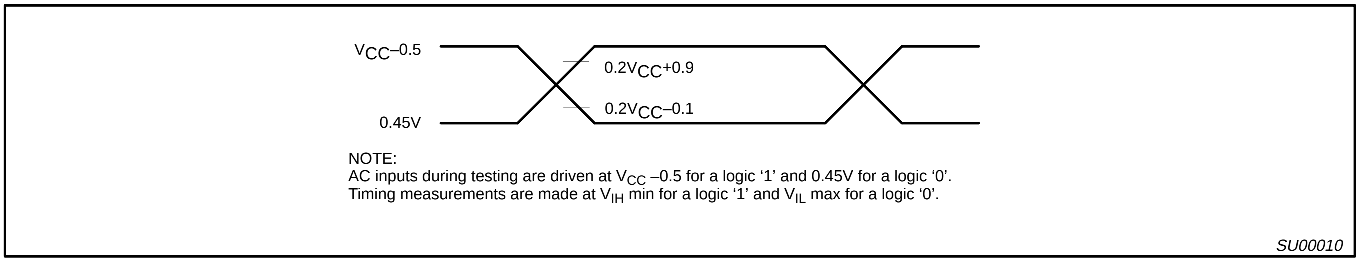
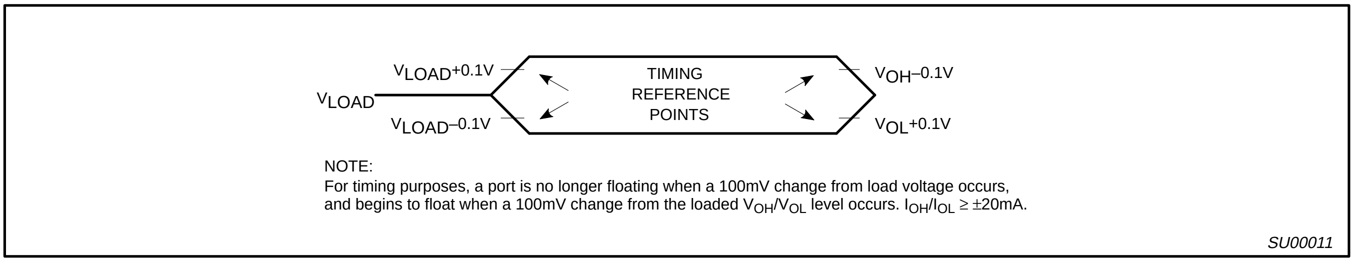


Figure 29. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 30. AC Testing Input/Output



NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20mA$.

Figure 31. Float Waveform

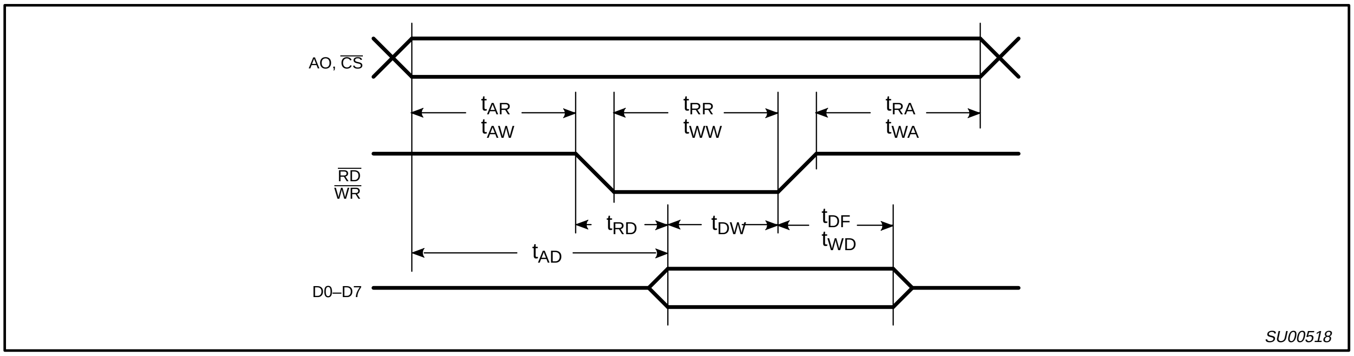


Figure 32. UPI Read/Write Cycles

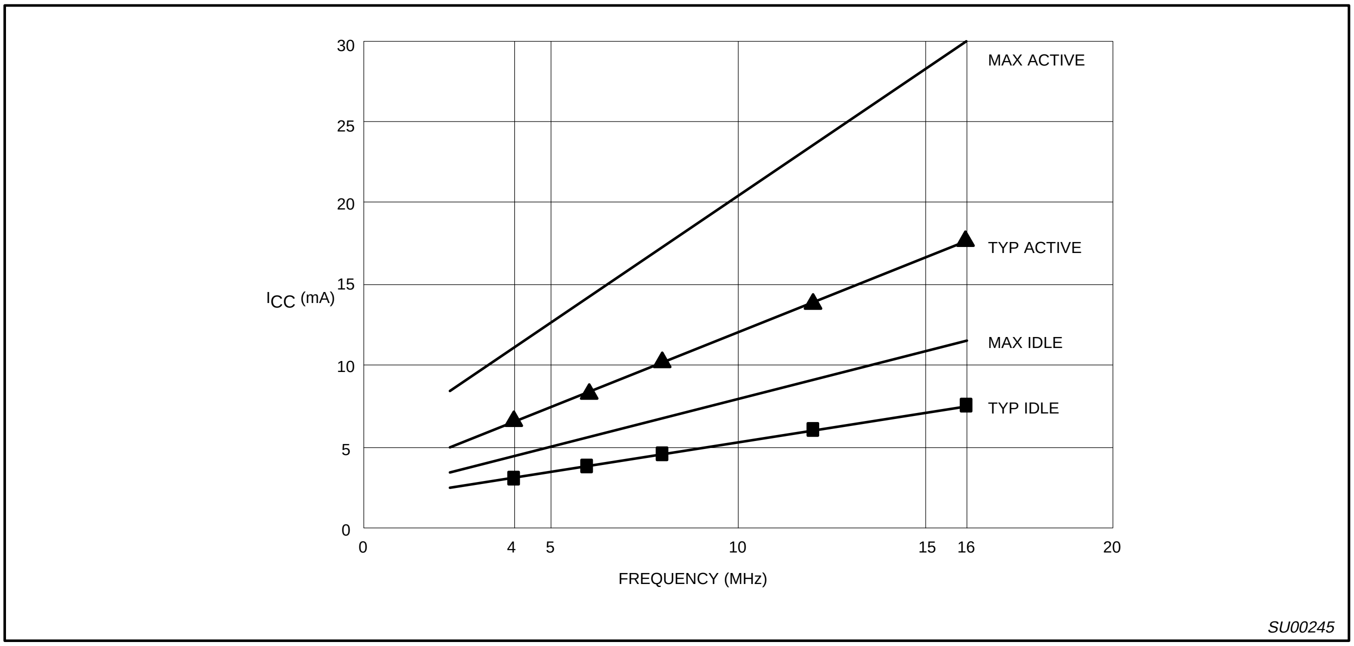


Figure 33. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

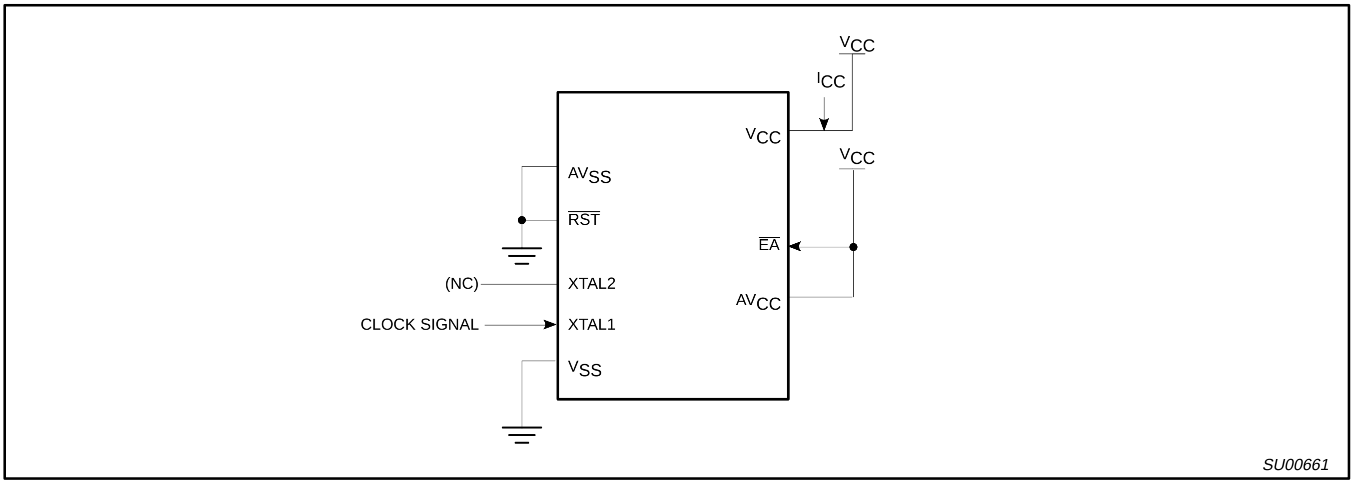


Figure 34. I_{CC} Test Condition, Active Mode
All other pins are disconnected

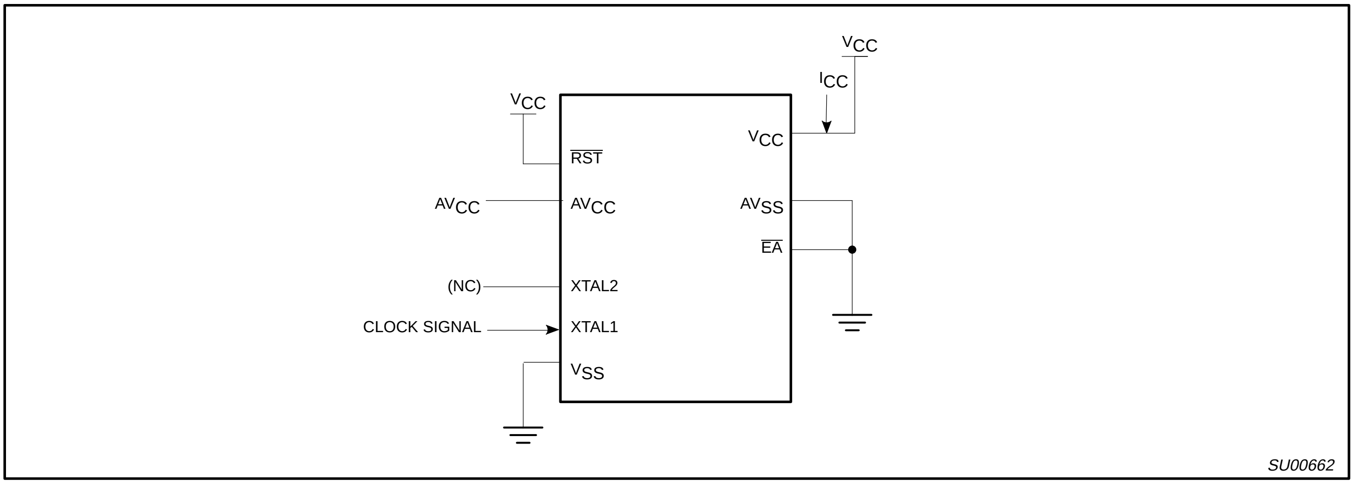


Figure 35. I_{CC} **Test Condition, Idle Mode**
All other pins are disconnected

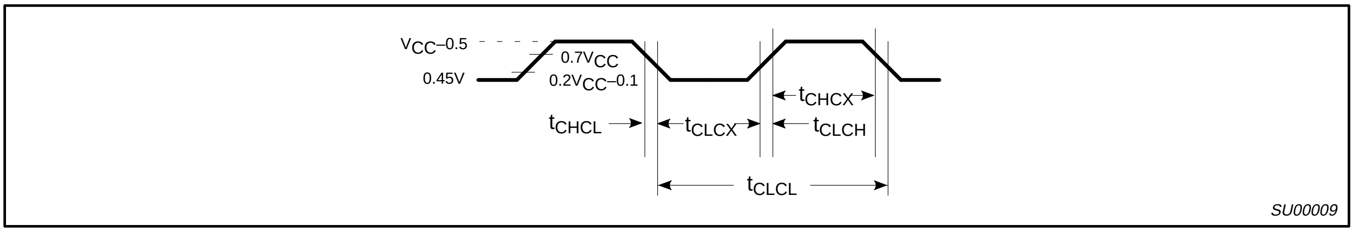


Figure 36. Clock Signal Waveform for I_{CC} **Tests in Active and Idle Modes**
$t_{CLCH} = t_{CHCL} = 5ns$

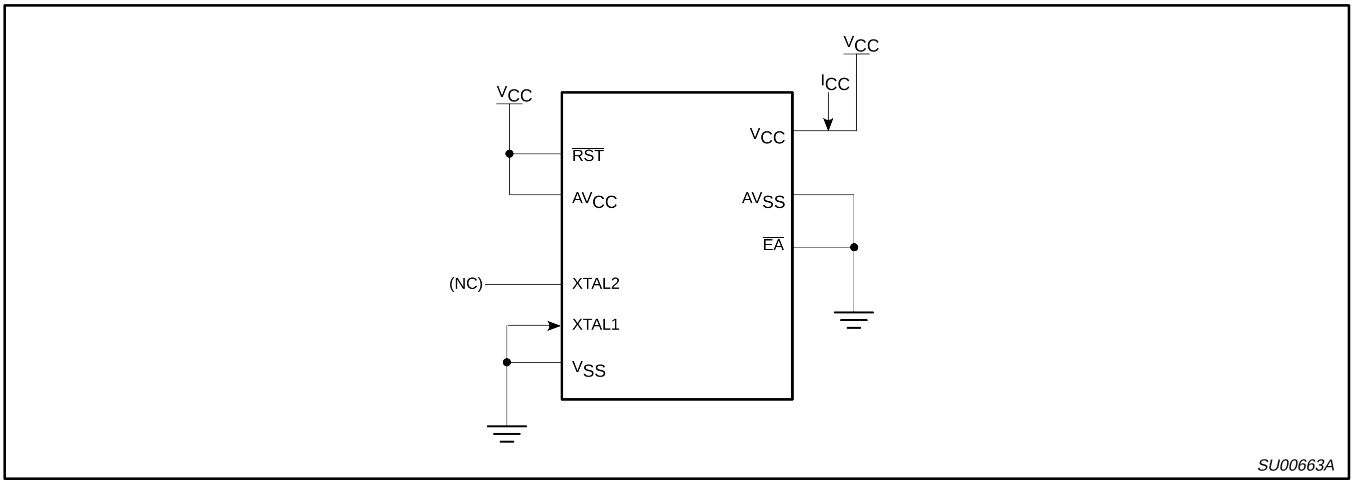


Figure 37. I_{CC} **Test Condition, Power Down Mode**
All other pins are disconnected. V_{CC} **= 2V to 5.5V**

EPROM CHARACTERISTICS

To put the 87C576 in the parallel EPROM programming mode, PSEN must be held high during power up, then driven low with reset active. The 87C576 is programmed by using a modified Quick-Pulse Programming™ algorithm.

The 87C576 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C576 manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 38 and 39. Figure 40 shows the circuit configuration for normal program memory verification.

On-Board Programming (OBP)

The On-Board Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the 87C576 through the serial port.

The OBP function is invoked by having the $\overline{EA}/V_{PP}$ pin at the V_{PP} voltage level at the time that the part exits reset. The OBP function only requires that the TxD, RxD, V_{SS}, V_{CC}, and V_{PP} pins be connected to an external circuit in order to use this feature.

The OBP feature provides for the use of a wide range of baud rates independent of the oscillator frequency used. It is also adaptable to a wide range of oscillator frequencies. The OBP facility provides for both auto-echo and no-echo of received characters. The OBP feature requires that an initial character, an uppercase U, be sent to the 87C576 to establish the baud rate to be used.

Once baud rate initialization has been performed, the OBP facility only accepts Intel Hex records. The record-type field of these hex records are used to indicate either commands or data for the OBP facility. The maximum number of data bytes in a record is limited to 16 (decimal). These commands/data are summarized below:

Record Type	Command/Data Function
00	Data record, programs the part with data indicated in record starting with load address in the record
01	EOF record, no operation
02	Specify timing parameters – rec length = 3 bytes – load address = 0000 – 1st byte = timer count for 50μs programming pulse – 2nd byte = timer count for 10μs delay between pulses – 3rd byte = 0AH
03	Program security bits – rec length = 1 byte – load address = 0000 – 1st byte = sec bit values (xxxx xxB2B1)
04	Display contents of USER EPROM array – rec length = 00 – load address = 0000
05	Verify security bit status – rec length = 00 – load address = 0000

Quick-Pulse Programming (Parallel)

The setup for microcontroller quick-pulse programming is shown in Figure 38. Note that the 87C576 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 3 and 2, as shown in Figure 38. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 1 specified in Table 3 are held at the ‘Program Code Data’ levels indicated in Table 3. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 39.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the ‘Pgm Encryption Table’ levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the ‘Pgm Security Bit’ levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 3 and 2 as shown in Figure 40. The other pins are held at the ‘Verify Code Data’ levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P1.0 and P1.1 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips
(B6H) = B6H indicates 87C576

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

™Trademark phrase of Intel Corporation.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P1.1	P1.0
Read signature	0	0	1	1	0	0	0	0
Program code data	0	0	0*	V_{PP}	1	0	1	1
Verify code data	0	0	1	1	0	0	1	1
Pgm encryption table	0	0	0*	V_{PP}	1	0	1	0
Pgm security bit 1	0	0	0*	V_{PP}	1	1	1	1
Pgm security bit 2	0	0	0*	V_{PP}	1	1	0	0

NOTES:

1. ‘0’ = Valid low for that pin, ‘1’ = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V±10% during programming and verification.

* ALE/$\overline{PROG}$ receives 5 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 50µs (±10µs) and high for a minimum of 10µs.

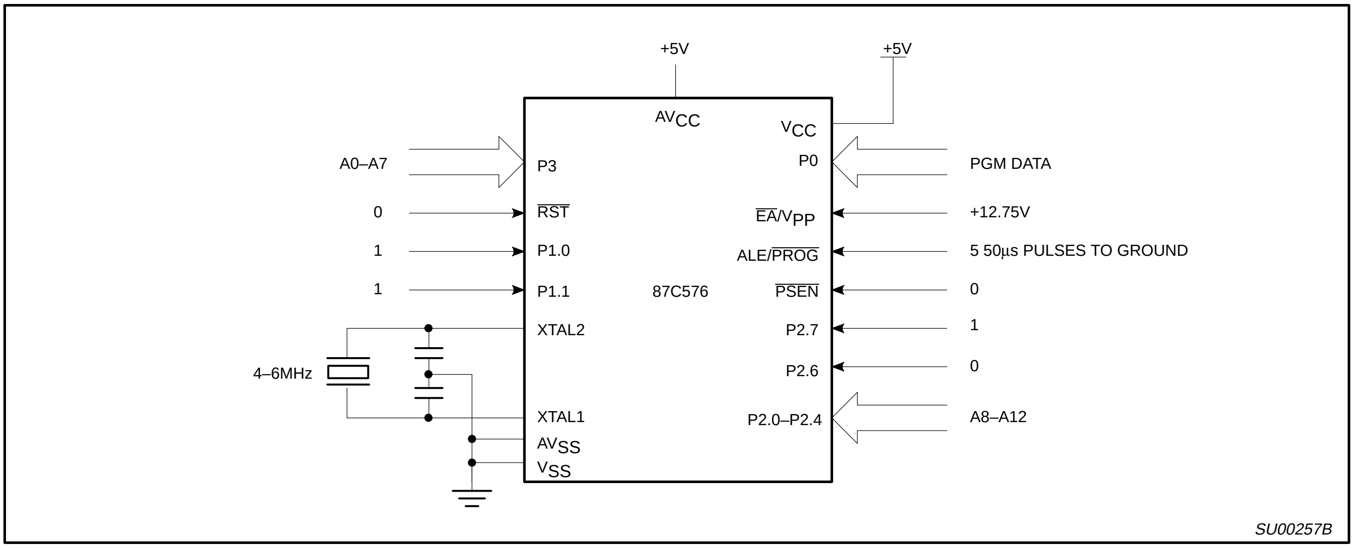


Figure 38. Programming Configuration

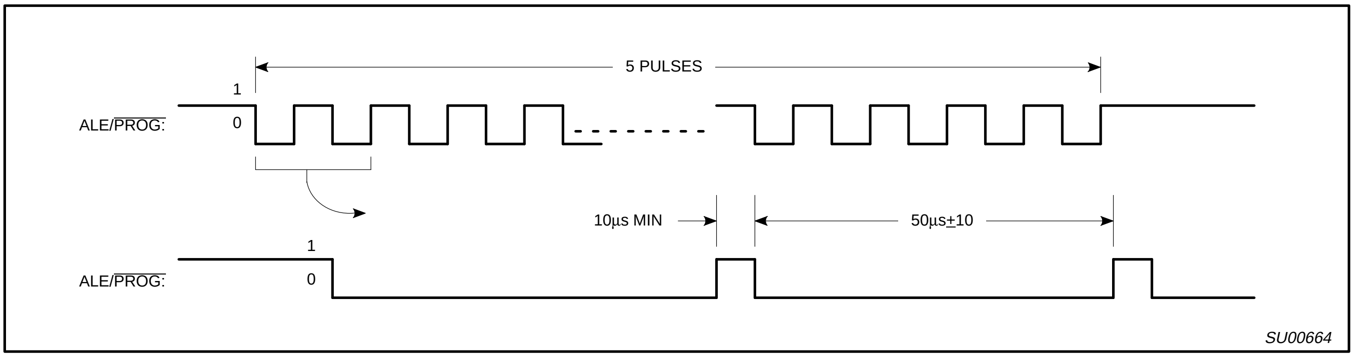


Figure 39. PROG Waveform

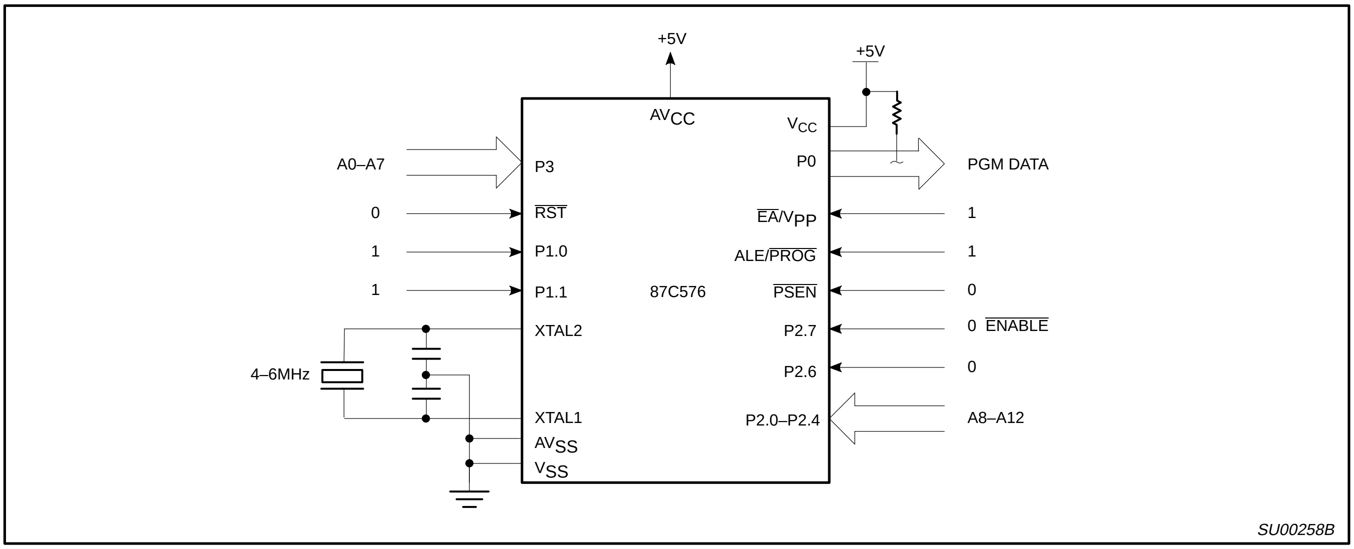
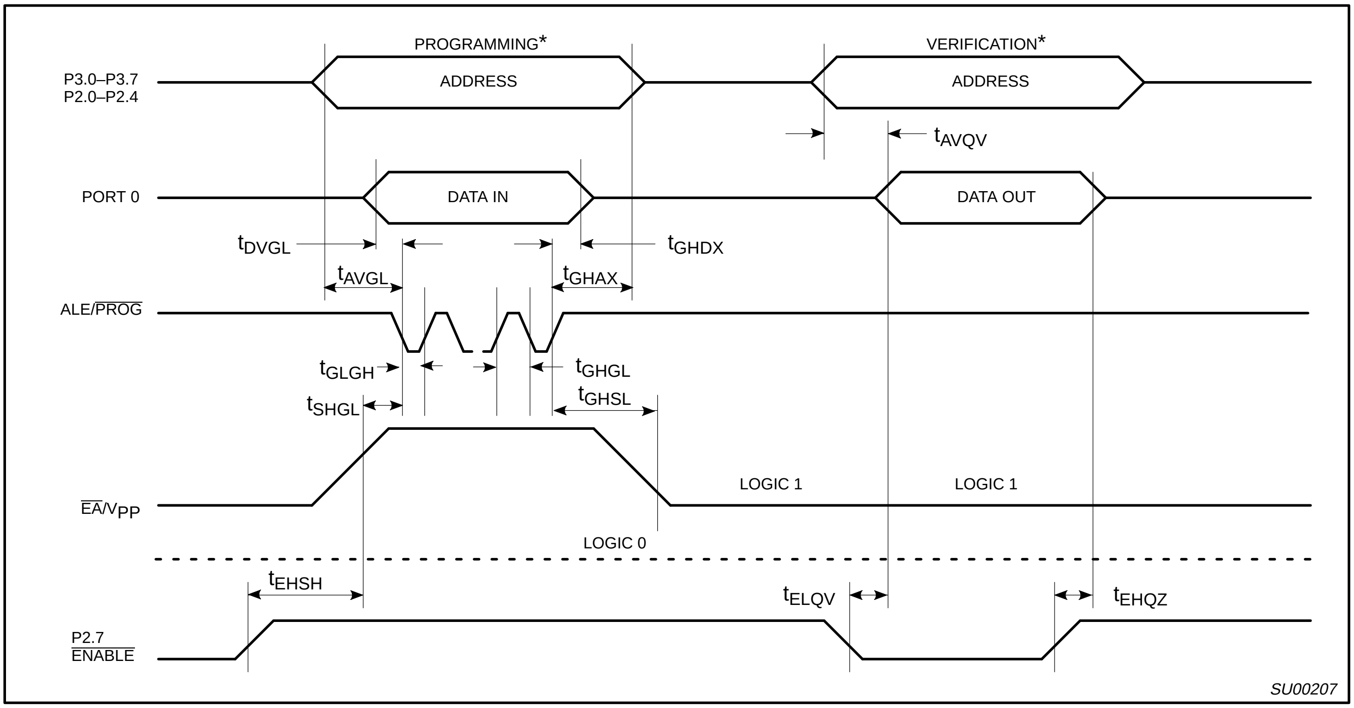


Figure 40. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 41)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	12	MHz
t_{AVGL}	Address setup to $\overline{\text{PROG}}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{\text{PROG}}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{\text{PROG}}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{\text{ENABLE}}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{\text{PROG}}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{\text{PROG}}$	10		µs
t_{GLGH}	$\overline{\text{PROG}}$ width	40	60	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{\text{ENABLE}}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low	10		µs



* FOR PROGRAMMING VERIFICATION SEE FIGURE 38.
FOR VERIFICATION CONDITIONS SEE FIGURE 40.

Figure 41. EPROM Programming and Verification