

## Single-chip 8-bit microcontroller

87C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

## DESCRIPTION

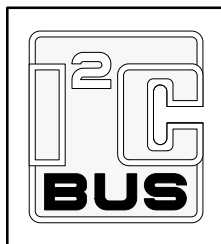
The 87C552 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM
- 80C552—ROMless version of the 83C552
- 87C552—8k bytes EPROM

The 87C552 contains a  $8k \times 8$  volatile  $256 \times 8$  read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I<sup>2</sup>C-bus), a “watchdog” timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C552 can be expanded using standard TTL compatible memories and logic.

In addition, the 87C552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

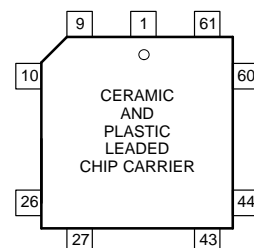
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75 $\mu$ s (0.5 $\mu$ s) and 40% in 1.5 $\mu$ s (1 $\mu$ s). Multiply and divide instructions require 3 $\mu$ s (2 $\mu$ s).



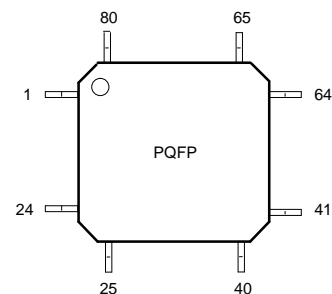
## FEATURES

- 80C51 central processing unit
- $8k \times 8$  EPROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- $256 \times 8$  RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I<sup>2</sup>C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three speed ranges:
  - 16MHz
- Extended temperature ranges
- OTP package available

## PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V <sub>DD</sub>	36	V <sub>SS</sub>
3	STADC	37	V <sub>SS</sub>
4	PWM0	38	NC
5	PWM1	39	P2.0/A08
6	EW	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMSR1	42	P2.3/A11
9	P4.2/CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	PSEN
14	P4.7/CMT1	48	ALE/PROG
15	RST	49	EA/V <sub>PP</sub>
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref-
25	P3.1/TxD	59	AVref+
26	P3.2/INT0	60	AV <sub>SS</sub>
27	P3.3/INT1	61	AV <sub>DD</sub>
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/WR	64	P5.5/ADC5
31	P3.7/RD	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1

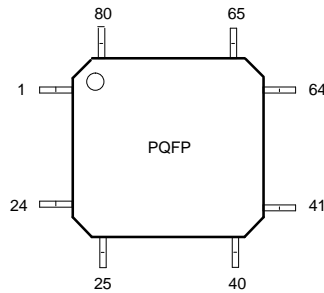


SU00208

# Single-chip 8-bit microcontroller

# 87C552

## PLASTIC QUAD FLAT PACK PIN FUNCTIONS

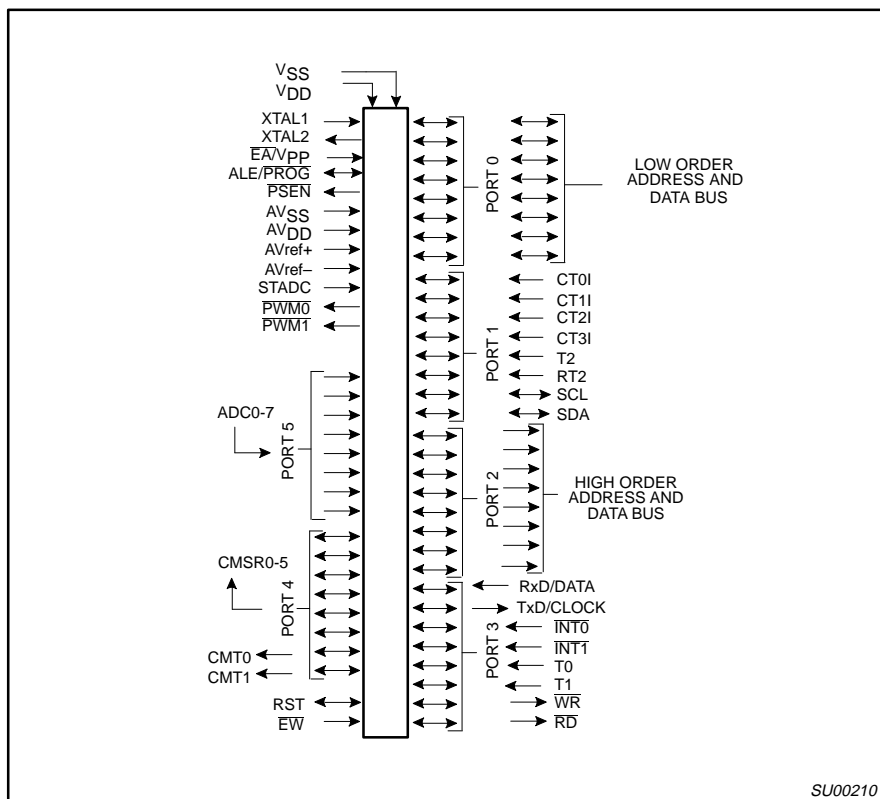


Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	P4.1/CMSR1	21	NC	41	P2.3/A11	61	AV <sub>SS</sub>
2	P4.2/CMSR2	22	NC	42	P2.4/A12	62	NC
3	NC	23	P3.3/INT1	43	NC	63	AV <sub>DD</sub>
4	P4.3/CMSR3	24	P3.4/T0	44	NC	64	P5.7/ADC7
5	P4.4/CMSR4	25	P3.5/T1	45	P2.5/A13	65	P5.6/ADC6
6	P4.5/CMSR5	26	P3.6/WR	46	P2.6/A14	66	P5.5/ADC5
7	P4.6/CMT0	27	P3.7/RD	47	P2.7/A15	67	P5.4/ADC4
8	P4.7/CMT1	28	NC	48	PSEN	68	P5.3/ADC3
9	RST	29	NC	49	ALE/PROG	69	P5.2/ADC2
10	P1.0/CT0I	30	NC	50	EA/V <sub>PP</sub>	70	P5.1/ADC1
11	P1.1/CT1I	31	XTAL2	51	P0.7/AD7	71	P5.0/ADC0
12	P1.2/CT2I	32	XTAL1	52	P0.6/AD6	72	V <sub>DD</sub>
13	P1.3/CT3I	33	IC	53	P0.5/AD5	73	IC
14	P1.4/T2	34	V <sub>SS</sub>	54	P0.4/AD4	74	STADC
15	P1.5/RT2	35	V <sub>SS</sub>	55	P0.3/AD3	75	PWM0
16	P1.6/SCL	36	V <sub>SS</sub>	56	P0.2/AD2	76	PWM1
17	P1.7/SDA	37	NC	57	P0.1/AD1	77	EW
18	P3.0/RxD	38	P2.0/A08	58	P0.0/AD0	78	NC
19	P3.1/TxD	39	P2.1/A09	59	AVref-	79	NC
20	P3.2/INT0	40	P2.2/A10	60	AVref+	80	P4.0/CMSR0

NC = Not Connected  
 IC = Internally Connected (do not use)

SU00209

## LOGIC SYMBOL



SU00210

## Single-chip 8-bit microcontroller

87C552

## ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		NORTH AMERICA PHILIPS PART ORDER NUMBER		DRAWING NUMBER	TEMPERATURE °C AND PACKAGE	FREQ MHz
ROMless	ROM	ROMless	ROM			
PCB80C552-5-16WP	PCB83C552-5WP/xxx	S80C552-4A68	S83C552-4A68	SOT188-3	0 to +70, Plastic Leaded Chip Carrier	16
PCB80C552-5-16H	PCB83C552-5H/xxx	S80C552-4B	S83C552-4B	SOT318-2	0 to +70, Plastic Quad Flat Pack	16
PCF80C552-5-16WP	PCF83C552-5WP/xxx	S80C552-5A68	S83C552-5A68	SOT188-3	-40 to +85, Plastic Leaded Chip Carrier	16
PCF80C552-5-16H	PCF83C552-5H/xxx	S80C552-5B	S83C552-5B	SOT318-2	-40 to +85, Plastic Quad Flat Pack	16
PCA80C552-5-16WP	PCA83C552-5WP/xxx	S80C552-6A68	S83C552-6A68	SOT188-3	-40 to +125, Plastic Leaded Chip Carrier	16
PCA80C552-5-16H	PCA83C552-5H/xxx	S80C552-6B	S83C552-6B	SOT318-2	-40 to +125, Plastic Quad Flat Pack	16
PCB80C552-5-24WP	PCB83C552-5WP/xxx	S80C552-AA68	S83C552-AA68	SOT188-3	0 to +70, Plastic Leaded Chip Carrier	24
PCB80C552-5-24H	PCB83C552-5H/xxx	S80C552-AB	S83C552-AB	SOT318-2	0 to +70, Plastic Quad Flat Pack	24
PCF80C552-5-24WP	PCF83C552-5WP/xxx	S80C552-BA68	S83C552-BA68	SOT188-3	-40 to +85, Plastic Leaded Chip Carrier	24
PCF80C552-5-24H	PCF83C552-5H/xxx	S80C552-BB	S83C552-BB	SOT318-2	-40 to +85, Plastic Quad Flat Pack	24
PCB80C552-5-30WP	PCB83C552-5WP/xxx	S80C552-CA68	S83C552-CA68	SOT188-3	0 to +70, Plastic Leaded Chip Carrier	30
PCB80C552-5-30H	PCB83C552-5H/xxx	S80C552-CB	S83C552-CB	SOT318-2	0 to +70, Plastic Quad Flat Pack	30

## NOTE:

- xxx denotes the ROM code number.

## Single-chip 8-bit microcontroller

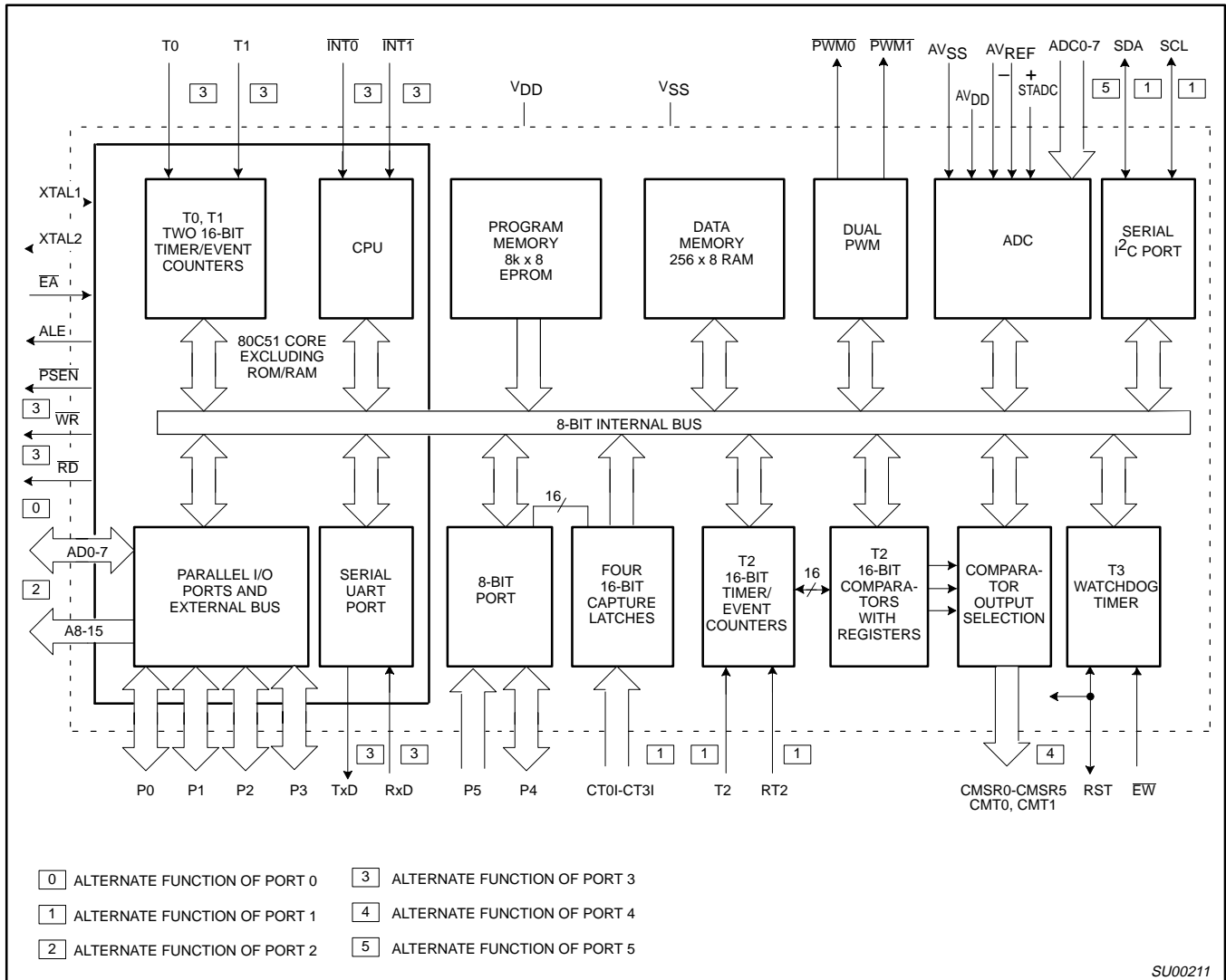
87C552

<b>EPROM</b>	<b>DRAWING NUMBER</b>	<b>TEMPERATURE °C AND PACKAGE</b>	<b>FREQ MHz</b>
S87C552-4A68	SOT188-3	0 to +70, Plastic Leaded Chip Carrier	16
S87C552-4K68	1473A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C552-4BA	SOT318-2	0 to +70, Plastic Quad Flat Pack	16
S87C552-5A68	SOT188-3	-40 to +85, Plastic Leaded Chip Carrier	16
S87C552-5K68	1473A	-40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C552-5BA	SOT318-2	-40 to +85, Plastic Quad Flat Pack	16

# Single-chip 8-bit microcontroller

## 87C552

### BLOCK DIAGRAM



## Single-chip 8-bit microcontroller

87C552

## PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	PLCC	QFP		
V <sub>DD</sub>	2	72	I	<b>Digital Power Supply:</b> +5V power supply pin during normal operation, idle and power-down mode.
STADC	3	74	I	<b>Start ADC Operation:</b> Input starting analog to digital conversion (ADC operation can also be started by software).
PWM <sub>0</sub>	4	75	O	<b>Pulse Width Modulation:</b> Output 0.
PWM <sub>1</sub>	5	76	O	<b>Pulse Width Modulation:</b> Output 1.
EW	6	77	I	<b>Enable Watchdog Timer:</b> Enable for T3 watchdog timer and disable power-down mode.
P0.0-P0.7	57-50	58-51	I/O	<b>Port 0:</b> Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 is also used to input the code byte during programming and to output the code byte during verification.
P1.0-P1.7	16-23	10-17	I/O	<b>Port 1:</b> 8-bit I/O port. Alternate functions include: <b>(P1.0-P1.5):</b> Quasi-bidirectional port pins. <b>(P1.6, P1.7):</b> Open drain port pins. <b>CT0I-CT3I (P1.0-P1.3):</b> Capture timer input signals for timer T2. <b>T2 (P1.4):</b> T2 event input. <b>RT2 (P1.5):</b> T2 timer reset signal. Rising edge triggered. <b>SCL (P1.6):</b> Serial port clock line I <sup>2</sup> C-bus. <b>SDA (P1.7):</b> Serial port data line I <sup>2</sup> C-bus. Port 1 is also used to input the lower order address byte during EPROM programming and verification. A0 is on P1.0, etc.
	16-21	10-15	I/O	
	22-23	16-17	I/O	
	16-19	10-13	I	
	20	14	I	
	21	15	I	
	22	16	I/O	
	23	17	I/O	
P2.0-P2.7	39-46	38-42, 45-47	I/O	<b>Port 2:</b> 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08-A15). Port 2 is also used to input the upper order address during EPROM programming and verification. A8 is on P2.0, A9 on P2.1, through A12 on P2.4.
P3.0-P3.7	24-31	18-20, 23-27	I/O	<b>Port 3:</b> 8-bit quasi-bidirectional I/O port. Alternate functions include: <b>RxD(P3.0):</b> Serial input port. <b>TxD (P3.1):</b> Serial output port. <b>INT<sub>0</sub> (P3.2):</b> External interrupt. <b>INT<sub>1</sub> (P3.3):</b> External interrupt. <b>T0 (P3.4):</b> Timer 0 external input. <b>T1 (P3.5):</b> Timer 1 external input. <b>WR (P3.6):</b> External data memory write strobe. <b>RD (P3.7):</b> External data memory read strobe.
	24	18		
	25	19		
	26	20		
	27	23		
	28	24		
	29	25		
	30	26		
31	27			
P4.0-P4.7	7-14	80, 1-2 4-8	I/O	<b>Port 4:</b> 8-bit quasi-bidirectional I/O port. Alternate functions include: <b>CMSR0-CMSR5 (P4.0-P4.5):</b> Timer T2 compare and set/reset outputs on a match with timer T2. <b>CMT0, CMT1 (P4.6, P4.7):</b> Timer T2 compare and toggle outputs on a match with timer T2.
	7-12	80, 1-2 4-6	O	
	13, 14	7, 8	O	
P5.0-P5.7	68-62, 1	71-64,	I	<b>Port 5:</b> 8-bit input port. <b>ADC0-ADC7 (P5.0-P5.7):</b> Alternate function: Eight input channels to ADC.
RST	15	9	I/O	<b>Reset:</b> Input to reset the 87C552. It also provides a reset pulse as output when timer T3 overflows.
XTAL1	35	32	I	<b>Crystal Input 1:</b> Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used.
XTAL2	34	31	O	<b>Crystal Input 2:</b> Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used.
V <sub>SS</sub>	36, 37	34-36	I	<b>Digital ground.</b>
PSEN	47	48	O	<b>Program Store Enable:</b> Active-low read strobe to external program memory.

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## PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	PLCC	QFP		
ALE/PROG	48	49	O	<b>Address Latch Enable:</b> Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up. This pin is also the program pulse input (PROG) during EPROM programming.
$\overline{EA}/V_{PP}$	49	50	I	<b>External Access:</b> When $\overline{EA}$ is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL low level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float. This pin also receives the 12.75V programming supply voltage ( $V_{PP}$ ) during EPROM programming.
$AV_{REF-}$	58	59	I	<b>Analog to Digital Conversion Reference Resistor:</b> Low-end.
$AV_{REF+}$	59	60	I	<b>Analog to Digital Conversion Reference Resistor:</b> High-end.
$AV_{SS}$	60	61	I	<b>Analog Ground</b>
$AV_{DD}$	61	63	I	<b>Analog Power Supply</b>

**NOTE:**

- To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than  $V_{DD} + 0.5V$  or  $V_{SS} - 0.5V$ , respectively.

### OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

### RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on  $V_{DD}$  and RST must come up at the same time for a proper start-up.

### IDLE MODE

In the idle mode, the CPU puts itself to sleep while some of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers

remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

### POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

**Table 1. External Pin Status During Idle and Power-Down Modes**

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PWM0/PWM1
Idle	Internal	1	1	Data	Data	Data	Data	Data	High
Idle	External	1	1	Float	Data	Address	Data	Data	High
Power-down	Internal	0	0	Data	Data	Data	Data	Data	High
Power-down	External	0	0	Float	Data	Data	Data	Data	High

## Single-chip 8-bit microcontroller

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## Serial Control Register (S1CON) – See Table 2

## S1CON (D8H)

CR2	ENS1	STA	STO	SI	AA	CR1	CR0
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Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT $f_{osc}$			$f_{osc}$ DIVIDED BY
			6MHz	12MHz	16MHz	
0	0	0	23	47	62.5	256
0	0	1	27	54	71	224
0	1	0	31.25	62.5	83.3	192
0	1	1	37	75	100	160
1	0	0	6.25	12.5	17	960
1	0	1	50	100	133 <sup>1</sup>	120
1	1	0	100	200	267 <sup>1</sup>	60
1	1	1	0.25 < 62.5 0 to 225	0.5 < 62.5 0 to 224	0.67 < 56 0 to 223	96 × (256 – (reload value Timer 1)) Timer 1 in Mode 2.

## NOTE:

1. These frequencies exceed the upper limit of 100kHz of the I<sup>2</sup>C-bus specification and cannot be used in an I<sup>2</sup>C-bus application.

ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage on $\bar{E}A/V_{PP}$ to $V_{SS}$	–0.5 to +13	V
Voltage on any other pin to $V_{SS}$	–0.5 to +6.5	V
Input, output DC current on any single I/O pin	5.0	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

## NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.

## DEVICE SPECIFICATIONS

TYPE	SUPPLY VOLTAGE (V)		FREQUENCY (MHz)		TEMPERATURE RANGE (°C)
	MIN	MAX	MIN	MAX	
P87C552-4	4.5	5.5	3.5	16	0 to +70
P87C552-5	4.5	5.5	3.5	16	–40 to +85



## Single-chip 8-bit microcontroller

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## DC ELECTRICAL CHARACTERISTICS

 $V_{SS}, AV_{SS} = 0V$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$I_{DD}$	Supply current operating: PCA8XC552-5-16	See notes 1 and 2 $f_{OSC} = 16MHz$		40	mA
$I_{ID}$	Idle mode: 87C552	See notes 1 and 3 $f_{OSC} = 16MHz$		7	mA
$I_{PD}$	Power-down current: 87C552	See notes 1 and 4; $2V < V_{PD} < V_{DD} \text{ max}$		50	$\mu A$
<b>Inputs</b>					
$V_{IL}$	Input low voltage, except $\overline{EA}$ , P1.6, P1.7		-0.5	$0.2V_{DD}-0.1$	V
$V_{IL1}$	Input low voltage to $\overline{EA}$		-0.5	$0.2V_{DD}-0.3$	V
$V_{IL2}$	Input low voltage to P1.6/SCL, P1.7/SDA <sup>5</sup>		-0.5	$0.3V_{DD}$	V
$V_{IH}$	Input high voltage, except XTAL1, RST		$0.2V_{DD}+0.9$	$V_{DD}+0.5$	V
$V_{IH1}$	Input high voltage, XTAL1, RST		$0.7V_{DD}$	$V_{DD}+0.5$	V
$V_{IH2}$	Input high voltage, P1.6/SCL, P1.7/SDA <sup>5</sup>		$0.7V_{DD}$	6.0	V
$I_{IL}$	Logical 0 input current, ports 1, 2, 3, 4, except P1.6, P1.7	$V_{IN} = 0.45V$		-50	$\mu A$
$I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3, 4, except P1.6, P1.7	See note 6		-650	$\mu A$
$\pm I_{IL1}$	Input leakage current, port 0, $\overline{EA}$ , STADC, $\overline{EW}$	$0.45V < V_I < V_{DD}$		10	$\mu A$
$\pm I_{IL2}$	Input leakage current, P1.6/SCL, P1.7/SDA	$0V < V_I < 6V$ $0V < V_{DD} < 5.5V$		10	$\mu A$
$\pm I_{IL3}$	Input leakage current, port 5	$0.45V < V_I < V_{DD}$		1	$\mu A$
<b>Outputs</b>					
$V_{OL}$	Output low voltage, ports 1, 2, 3, 4, except P1.6, P1.7	$I_{OL} = 1.6mA^7$		0.45	V
$V_{OL1}$	Output low voltage, port 0, ALE, PSEN, PWM0, PWM1	$I_{OL} = 3.2mA^7$		0.45	V
$V_{OL2}$	Output low voltage, P1.6/SCL, P1.7/SDA	$I_{OL} = 3.0mA^7$		0.4	V
$V_{OH}$	Output high voltage, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA	$-I_{OH} = 60\mu A$ $-I_{OH} = 25\mu A$ $-I_{OH} = 10\mu A$	2.4 $0.75V_{DD}$ $0.9V_{DD}$		V V V
$V_{OH1}$	Output high voltage (port 0 in external bus mode, ALE, PSEN, PWM0, PWM1) <sup>8</sup>	$-I_{OH} = 400\mu A$ $-I_{OH} = 150\mu A$ $-I_{OH} = 40\mu A$	2.4 $0.75V_{DD}$ $0.9V_{DD}$		V V V
$V_{OH2}$	Output high voltage (RST)	$-I_{OH} = 400\mu A$ $-I_{OH} = 120\mu A$	2.4 $0.8V_{DD}$		V V
$R_{RST}$	Internal reset pull-down resistor		50	150	k $\Omega$
$C_{IO}$	Pin capacitance	Test freq = 1MHz, $T_{amb} = 25^\circ C$		10	pF
<b>Analog Inputs</b>					
$AV_{DD}$	Analog supply voltage: 87C552 <sup>9</sup>	$AV_{DD} = V_{DD} \pm 0.2V$	4.5	5.5	V
$AI_{DD}$	Analog supply current: operating:	Port 5 = 0 to $AV_{DD}$		1.2	mA
$AI_{ID}$	Idle mode: 87C552			50	$\mu A$
$AI_{PD}$	Power-down mode: 87C552	$2V < AV_{PD} < AV_{DD} \text{ max}$		50	$\mu A$

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## DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
<b>Analog Inputs (Continued)</b>					
AV <sub>IN</sub>	Analog input voltage		AV <sub>SS</sub> -0.2	AV <sub>DD</sub> +0.2	V
AV <sub>REF</sub>	Reference voltage: AV <sub>REF-</sub> AV <sub>REF+</sub>		AV <sub>SS</sub> -0.2	AV <sub>DD</sub> +0.2	V V
R <sub>REF</sub>	Resistance between AV <sub>REF+</sub> and AV <sub>REF-</sub>		10	50	kΩ
C <sub>IA</sub>	Analog input capacitance			15	pF
t <sub>ADS</sub>	Sampling time			8t <sub>CY</sub>	μs
t <sub>ADC</sub>	Conversion time (including sampling time)			50t <sub>CY</sub>	μs
DL <sub>e</sub>	Differential non-linearity <sup>10, 11, 12</sup>			±1	LSB
IL <sub>e</sub>	Integral non-linearity <sup>10, 13</sup>			±2	LSB
OS <sub>e</sub>	Offset error <sup>10, 14</sup>			±2	LSB
G <sub>e</sub>	Gain error <sup>10, 15</sup>			±0.4	%
A <sub>e</sub>	Absolute voltage error <sup>10, 16</sup>			±3	LSB
M <sub>CTC</sub>	Channel to channel matching			±1	LSB
C <sub>t</sub>	Crosstalk between inputs of port 5 <sup>17</sup>	0-100kHz		-60	dB

## NOTES FOR DC ELECTRICAL CHARACTERISTICS:

- See Figures 10 through 15 for I<sub>DD</sub> test conditions.
- The operating supply current is measured with all output pins disconnected; XTAL1 driven with t<sub>r</sub> = t<sub>f</sub> = 10ns; V<sub>IL</sub> = V<sub>SS</sub> + 0.5V; V<sub>IH</sub> = V<sub>DD</sub> - 0.5V; XTAL2 not connected; E<sub>A</sub> = R<sub>ST</sub> = Port 0 = E<sub>W</sub> = V<sub>DD</sub>; STADC = V<sub>SS</sub>.
- The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with t<sub>r</sub> = t<sub>f</sub> = 10ns; V<sub>IL</sub> = V<sub>SS</sub> + 0.5V; V<sub>IH</sub> = V<sub>DD</sub> - 0.5V; XTAL2 not connected; Port 0 = E<sub>W</sub> = V<sub>DD</sub>; E<sub>A</sub> = R<sub>ST</sub> = STADC = V<sub>SS</sub>.
- The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = E<sub>W</sub> = V<sub>DD</sub>; E<sub>A</sub> = R<sub>ST</sub> = STADC = XTAL1 = V<sub>SS</sub>.
- The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I<sup>2</sup>C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
- Pins of ports 1 (except P1.6, P1.7), 2, 3, and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V<sub>IN</sub> is approximately 2V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V<sub>OLs</sub> of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I<sub>OL</sub> can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V<sub>OH</sub> on ALE and PSEN to momentarily fall below the 0.9V<sub>DD</sub> specification when the address bits are stabilizing.
- The following condition must not be exceeded: V<sub>DD</sub> - 0.2V < AV<sub>DD</sub> < V<sub>DD</sub> + 0.2V.
- Conditions: AV<sub>REF-</sub> = 0V; AV<sub>DD</sub> = 5.0V. Measurement by continuous conversion of AV<sub>IN</sub> = -20mV to 5.12V in steps of 0.5mV, deriving parameters from collected conversion results of ADC. AV<sub>REF+</sub> (87C552) = 4.977V. ADC is monotonic with no missing codes.
- The differential non-linearity (DL<sub>e</sub>) is the difference between the actual step width and the ideal step width. (See Figure 1.)
- The ADC is monotonic; there are no missing codes.
- The integral non-linearity (IL<sub>e</sub>) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 1.)
- The offset error (OS<sub>e</sub>) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 1.)
- The gain error (G<sub>e</sub>) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. (See Figure 1.)
- The absolute voltage error (A<sub>e</sub>) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
- This should be considered when both analog and digital signals are simultaneously input to port 5.

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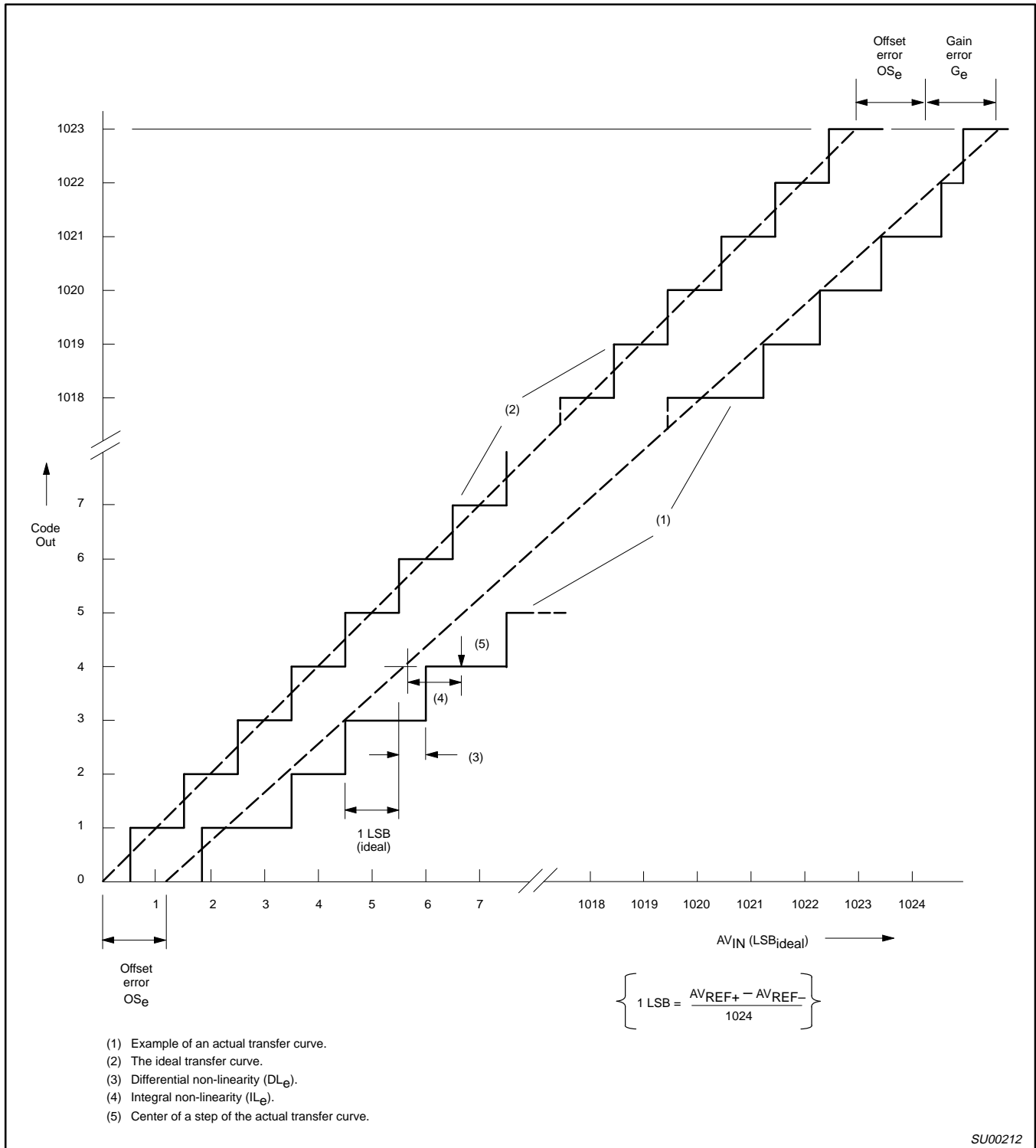


Figure 1. ADC Conversion Characteristic

## Single-chip 8-bit microcontroller

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AC ELECTRICAL CHARACTERISTICS<sup>1, 2</sup>

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	2	Oscillator frequency					3.5	16	MHz
$t_{LHLL}$	2	ALE pulse width	127		85		$2t_{CLCL}-40$		ns
$t_{AVLL}$	2	Address valid to ALE low	28		8		$t_{CLCL}-55$		ns
$t_{LLAX}$	2	Address hold after ALE low	48		28		$t_{CLCL}-35$		ns
$t_{LLIV}$	2	ALE low to valid instruction in		234		150		$4t_{CLCL}-100$	ns
$t_{LLPL}$	2	ALE low to $\overline{PSEN}$ low	43		23		$t_{CLCL}-40$		ns
$t_{PLPH}$	2	$\overline{PSEN}$ pulse width	205		143		$3t_{CLCL}-45$		ns
$t_{PLIV}$	2	$\overline{PSEN}$ low to valid instruction in		145		83		$3t_{CLCL}-105$	ns
$t_{PXIX}$	2	Input instruction hold after $\overline{PSEN}$	0		0		0		ns
$t_{PXIZ}$	2	Input instruction float after $\overline{PSEN}$		59		38		$t_{CLCL}-25$	ns
$t_{AVIV}$	2	Address to valid instruction in		312		208		$5t_{CLCL}-105$	ns
$t_{PLAZ}$	2	$\overline{PSEN}$ low to address float		10		10		10	ns
<b>Data Memory</b>									
$t_{AVLL}$	3, 4	Address valid to ALE low	43		23		$t_{CLCL}-40$		ns
$t_{RLRH}$	3	$\overline{RD}$ pulse width	400		275		$6t_{CLCL}-100$		ns
$t_{WLWH}$	3	$\overline{WR}$ pulse width	400		275		$6t_{CLCL}-100$		ns
$t_{RLDV}$	3	$\overline{RD}$ low to valid data in		252		148		$5t_{CLCL}-165$	ns
$t_{RHDX}$	3	Data hold after $\overline{RD}$	0		0		0		ns
$t_{RHDZ}$	3	Data float after $\overline{RD}$		97		55		$2t_{CLCL}-70$	ns
$t_{LLDV}$	3	ALE low to valid data in		517		350		$8t_{CLCL}-150$	ns
$t_{AVDV}$	3	Address to valid data in		585		398		$9t_{CLCL}-165$	ns
$t_{LLWL}$	3, 4	ALE low to $\overline{RD}$ or $\overline{WR}$ low	200	300	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
$t_{AVWL}$	3, 4	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	203		120		$4t_{CLCL}-130$		ns
$t_{QVWX}$	4	Data valid to $\overline{WR}$ transition	23		3		$t_{CLCL}-60$		ns
$t_{DW}$	4	Data before $\overline{WR}$	433		288		$7t_{CLCL}-150$		ns
$t_{WHQX}$	4	Data hold after $\overline{WR}$	33		13		$t_{CLCL}-50$		ns
$t_{RLAZ}$	4	$\overline{RD}$ low to address float		0		0		0	ns
$t_{WHLH}$	3, 4	$\overline{RD}$ or $\overline{WR}$ high to ALE high	43	123	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
<b>External Clock</b>									
$t_{CHCX}$	5	High time <sup>3</sup>	20		20		20		ns
$t_{CLCX}$	5	Low time <sup>3</sup>	20		20		20		ns
$t_{CLCH}$	5	Rise time <sup>3</sup>		20		20		20	ns
$t_{CHCL}$	5	Fall time <sup>3</sup>		20		20		20	ns
<b>Serial Timing – Shift Register Mode<sup>4</sup></b> (Test Conditions: $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ ; $V_{SS} = 0\text{V}$ ; Load Capacitance = 80pF)									
$t_{XLXL}$	6	Serial port clock cycle time	1.0		0.75		$12t_{CLCL}$		$\mu\text{s}$
$t_{QVXH}$	6	Output data setup to clock rising edge	700		492		$10t_{CLCL}-133$		ns
$t_{XHQX}$	6	Output data hold after clock rising edge	50		8		$2t_{CLCL}-117$		ns
$t_{XHDX}$	6	Input data hold after clock rising edge	0		0		0		ns
$t_{XHDX}$	6	Clock rising edge to input data valid		700		492		$10t_{CLCL}-133$	ns

## NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and  $\overline{PSEN}$  = 100pF, load capacitance for all other outputs = 80pF.
- $t_{CLCL} = 1/f_{OSC}$  = one oscillator clock period.  
 $t_{CLCL} = 83.3\text{ns}$  at  $f_{OSC} = 12\text{MHz}$ .  
 $t_{CLCL} = 62.5\text{ns}$  at  $f_{OSC} = 16\text{MHz}$ .
- These values are characterized but not 100% production tested.

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## AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	INPUT	OUTPUT
<b>I<sup>2</sup>C Interface (Refer to Figure 9)<sup>5</sup></b>			
t <sub>HD;STA</sub>	START condition hold time	≥ 14 t <sub>CLCL</sub>	> 4.0μs <sup>1</sup>
t <sub>LOW</sub>	SCL low time	≥ 16 t <sub>CLCL</sub>	> 4.7μs <sup>1</sup>
t <sub>HIGH</sub>	SCL high time	≥ 14 t <sub>CLCL</sub>	> 4.0μs <sup>1</sup>
t <sub>RC</sub>	SCL rise time	≤ 1μs	– <sup>2</sup>
t <sub>FC</sub>	SCL fall time	≤ 0.3μs	< 0.3μs <sup>3</sup>
t <sub>SU;DAT1</sub>	Data set-up time	≥ 250ns	> 20 t <sub>CLCL</sub> – t <sub>RD</sub>
t <sub>SU;DAT2</sub>	SDA set-up time (before rep. START cond.)	≥ 250ns	> 1μs <sup>1</sup>
t <sub>SU;DAT3</sub>	SDA set-up time (before STOP cond.)	≥ 250ns	> 8 t <sub>CLCL</sub>
t <sub>HD;DAT</sub>	Data hold time	≥ 0ns	> 8 t <sub>CLCL</sub> – t <sub>FC</sub>
t <sub>SU;STA</sub>	Repeated START set-up time	≥ 14 t <sub>CLCL</sub>	> 4.7μs <sup>1</sup>
t <sub>SU;STO</sub>	STOP condition set-up time	≥ 14 t <sub>CLCL</sub>	> 4.0μs <sup>1</sup>
t <sub>BUF</sub>	Bus free time	≥ 14 t <sub>CLCL</sub>	> 4.7μs <sup>1</sup>
t <sub>RD</sub>	SDA rise time	≤ 1μs	– <sup>2</sup>
t <sub>FD</sub>	SDA fall time	≤ 0.3μs	< 0.3μs <sup>3</sup>

**NOTES:**

1. At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1μs.
3. Spikes on the SDA and SCL lines with a duration of less than 3 t<sub>CLCL</sub> will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400pF.
4. t<sub>CLCL</sub> = 1/f<sub>OSC</sub> = one oscillator clock period at pin XTAL1. For 62ns (42s) < t<sub>CLCL</sub> < 285ns (16MHz (24Hz) > f<sub>OSC</sub> > 3.5MHz) the SI01 interface meets the I<sup>2</sup>C-bus specification for bit-rates up to 100 kbit/s.
5. These values are guaranteed but not 100% production tested.

# Single-chip 8-bit microcontroller

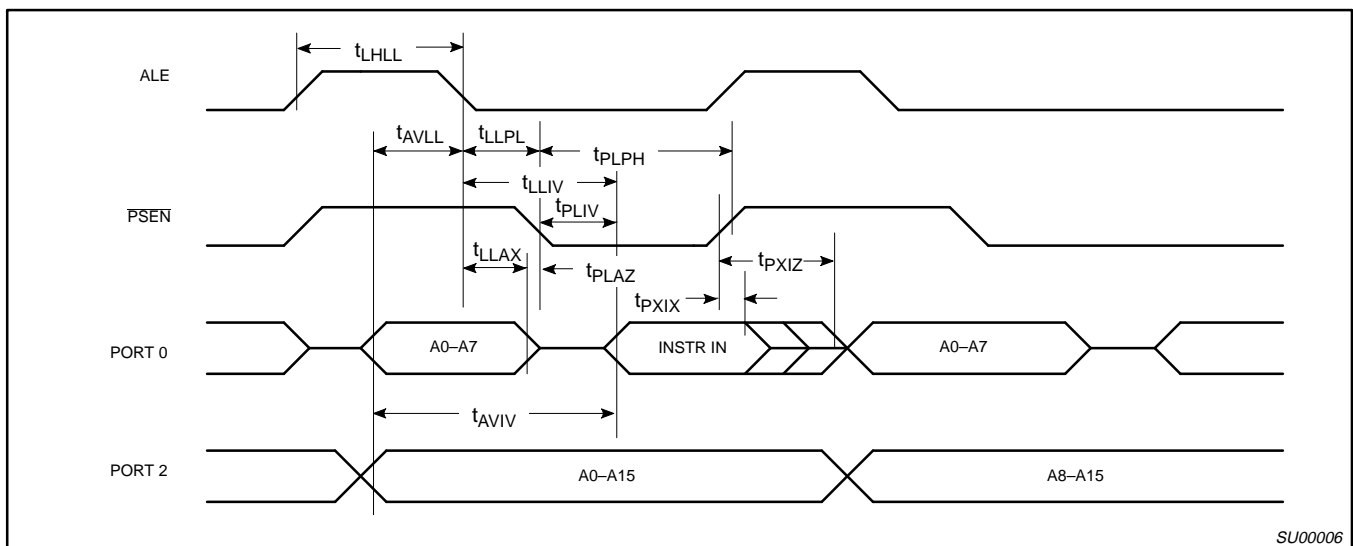
87C552

## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:  
 A – Address  
 C – Clock  
 D – Input data  
 H – Logic level high  
 I – Instruction (program memory contents)  
 L – Logic level low, or ALE  
 P –  $\overline{\text{PSEN}}$

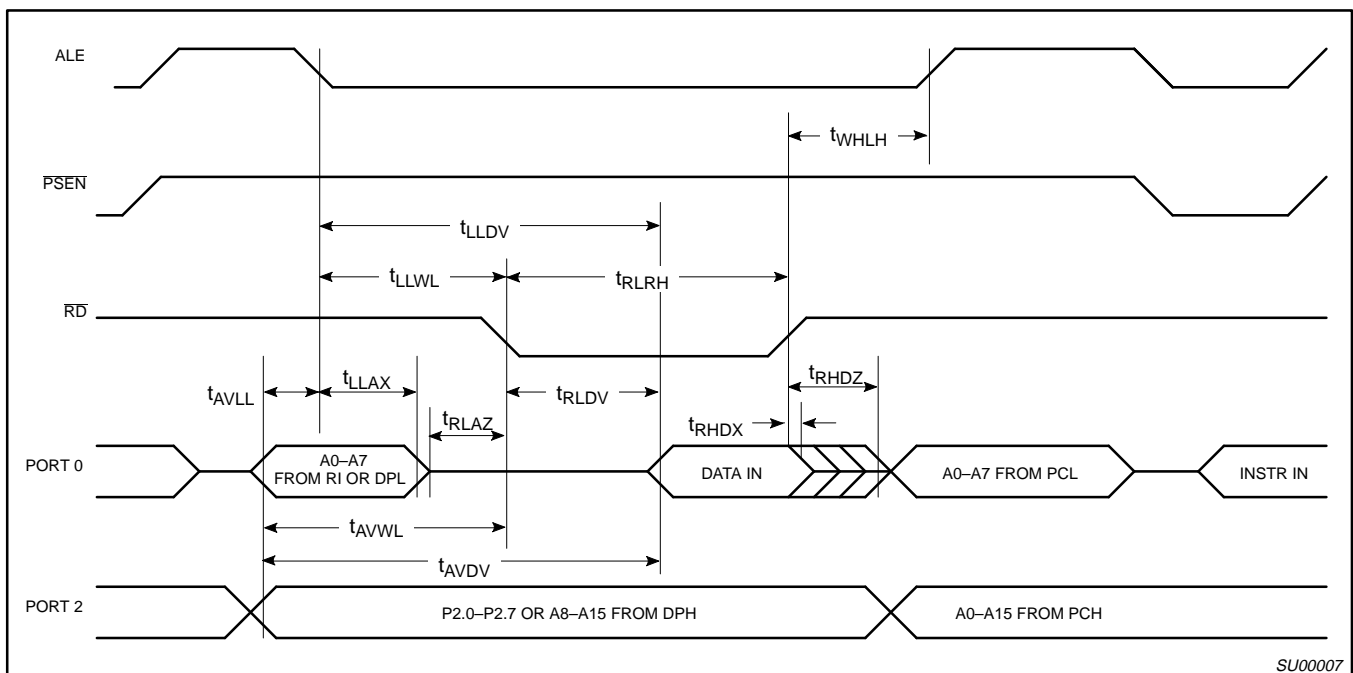
Q – Output data  
 R –  $\overline{\text{RD}}$  signal  
 t – Time  
 V – Valid  
 W –  $\overline{\text{WR}}$  signal  
 X – No longer a valid logic level  
 Z – Float

**Examples:**  $t_{\text{AVLL}}$  = Time for address valid to ALE low.  
 $t_{\text{LLPL}}$  = Time for ALE low to  $\overline{\text{PSEN}}$  low.



SU00006

Figure 2. External Program Memory Read Cycle



SU00007

Figure 3. External Data Memory Read Cycle

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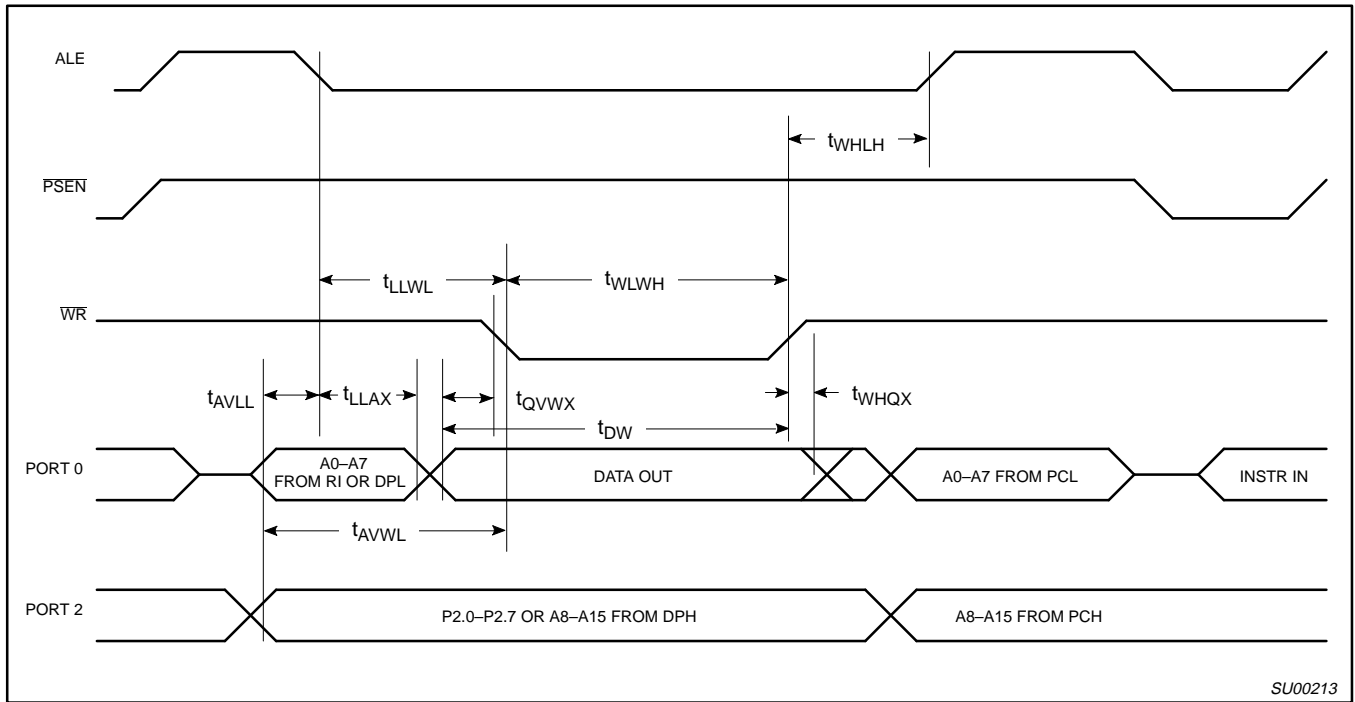


Figure 4. External Data Memory Write Cycle

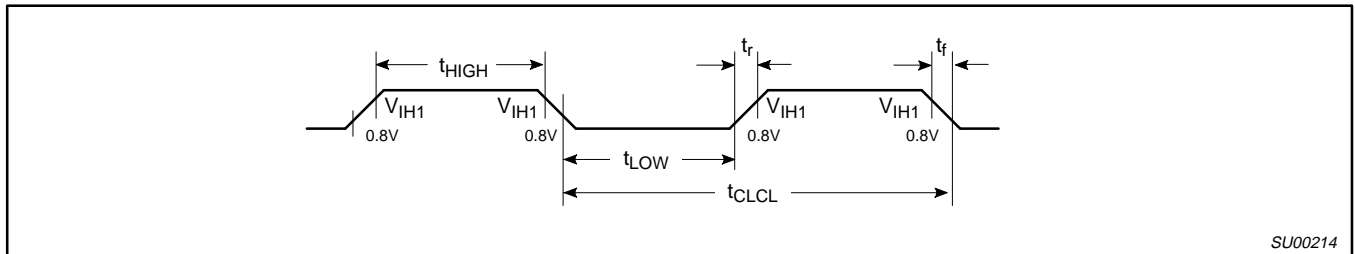


Figure 5. External Clock Drive XTAL1

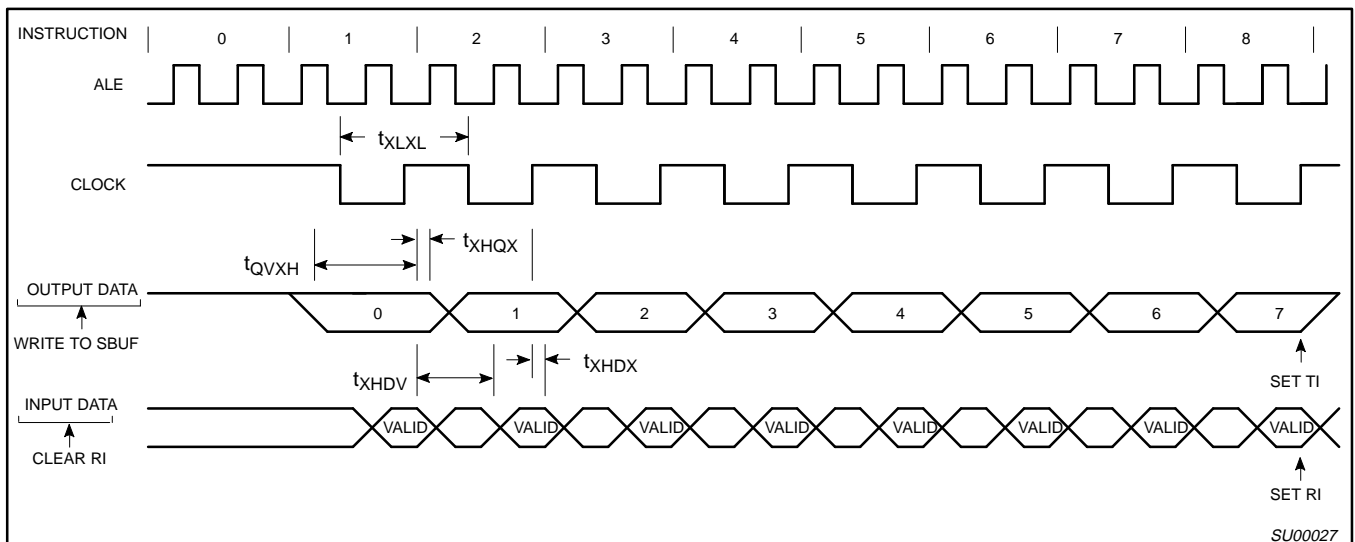


Figure 6. Shift Register Mode Timing

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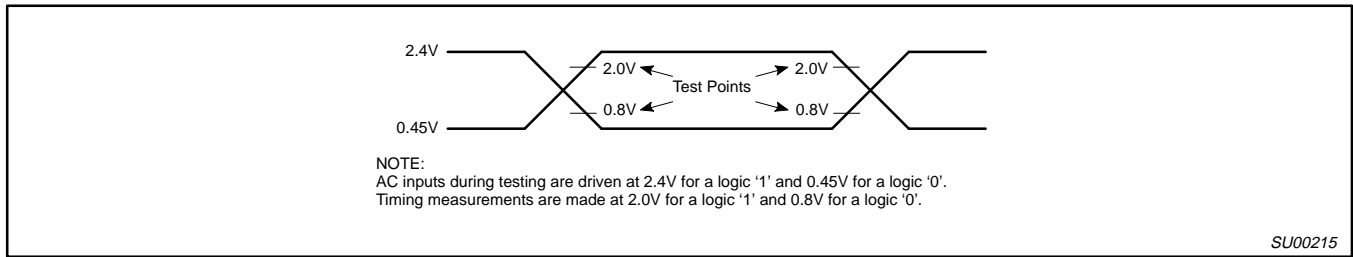


Figure 7. AC Testing Input/Output

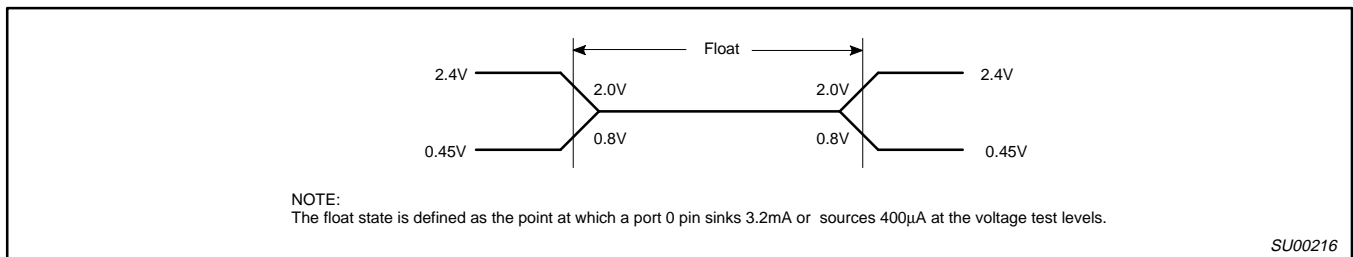


Figure 8. AC Testing Input, Float Waveform

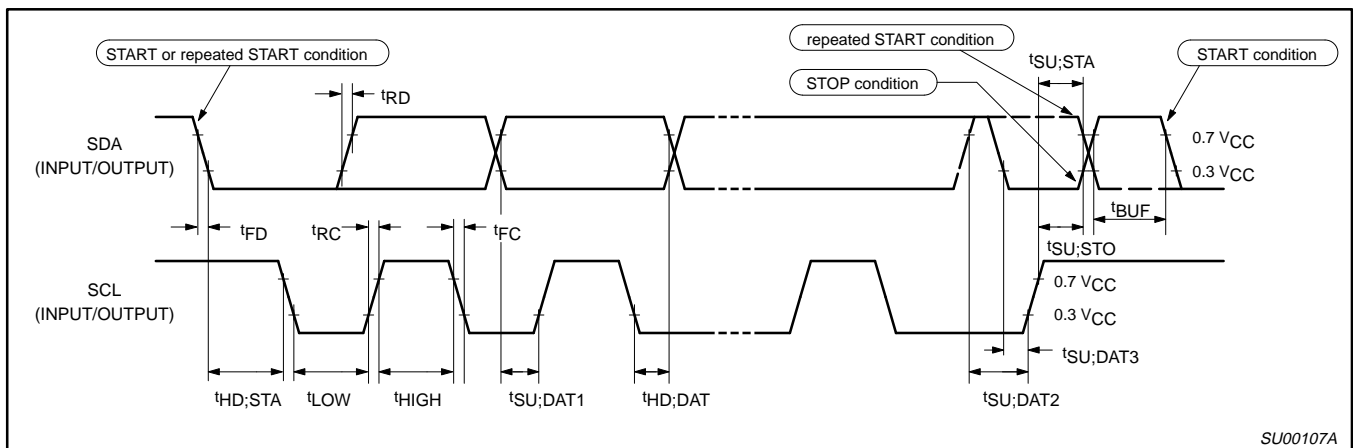


Figure 9. Timing SIO1 (I<sup>2</sup>C) Interface



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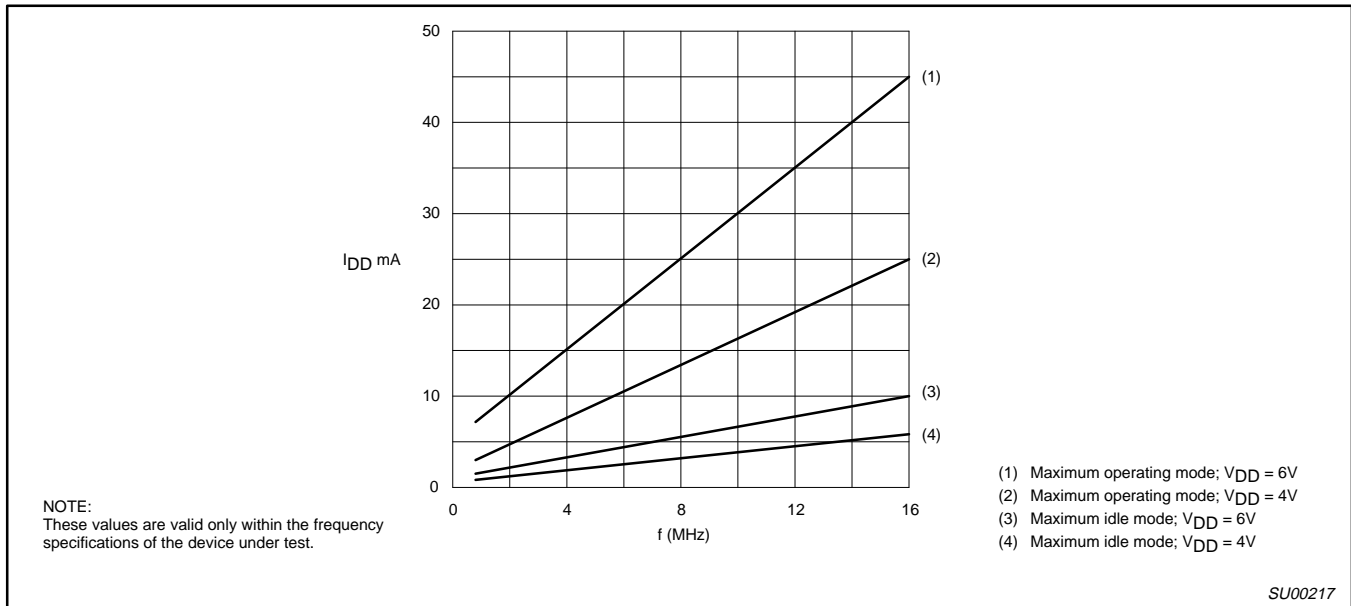


Figure 10. 16MHz Version Supply Current ( $I_{DD}$ ) as a Function of Frequency at XTAL1 ( $f_{osc}$ )

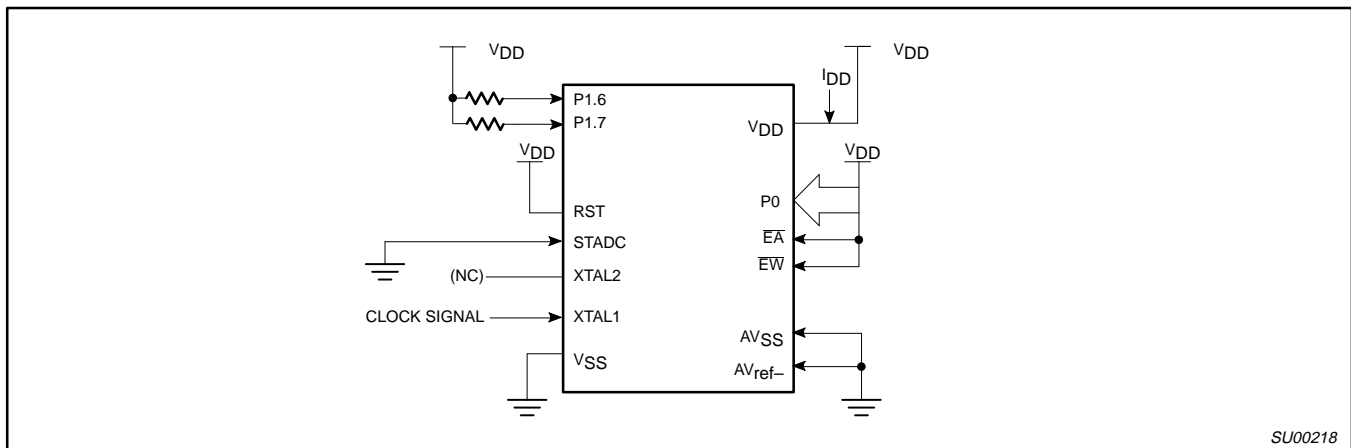
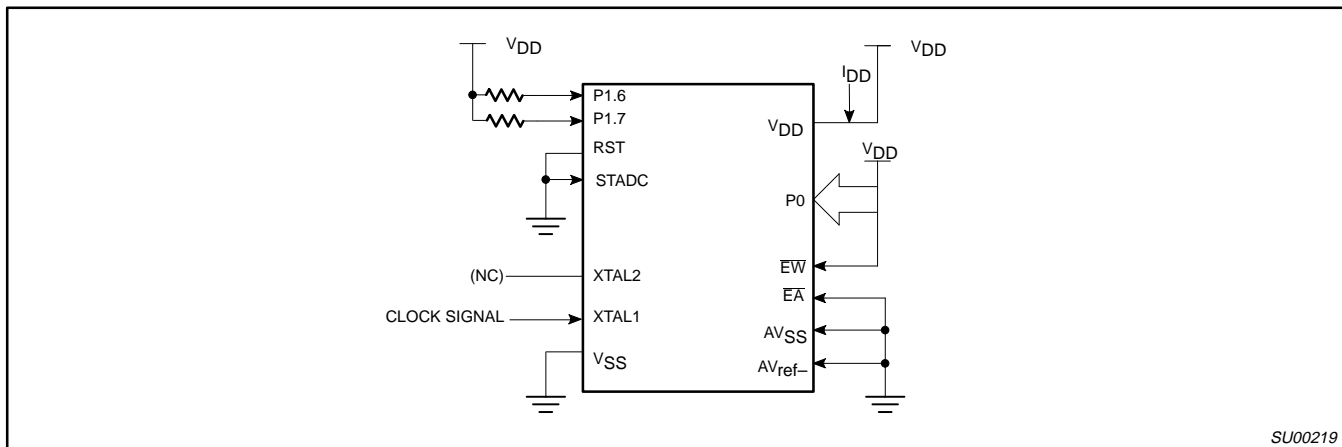


Figure 11.  $I_{DD}$  Test Condition, Active Mode  
All other pins are disconnected<sup>1</sup>

1. Active Mode:
  - a. The following pins must be forced to  $V_{DD}$ :  $\overline{EA}$ , RST, Port 0, and  $\overline{EW}$ .
  - b. The following pins must be forced to  $V_{SS}$ : STADC,  $AV_{SS}$ , and  $AV_{ref-}$ .
  - c. Ports 1.6 and 1.7 should be connected to  $V_{DD}$  through resistors of sufficiently high value such that the sink current into these pins cannot exceed the  $I_{OL1}$  spec of these pins.
  - d. The following pins must be disconnected: XTAL2 and all pins not specified above.

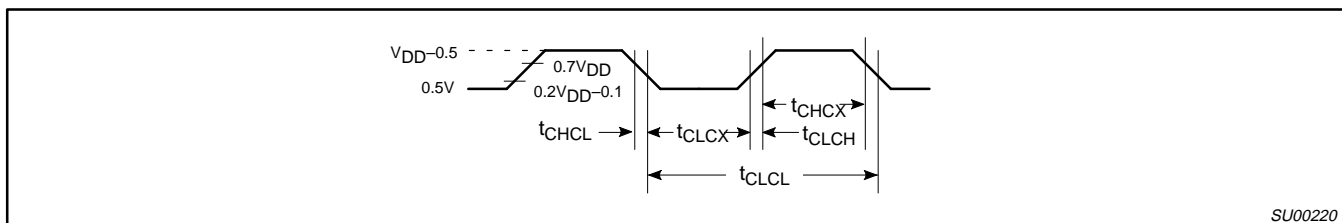
# Single-chip 8-bit microcontroller

# 87C552

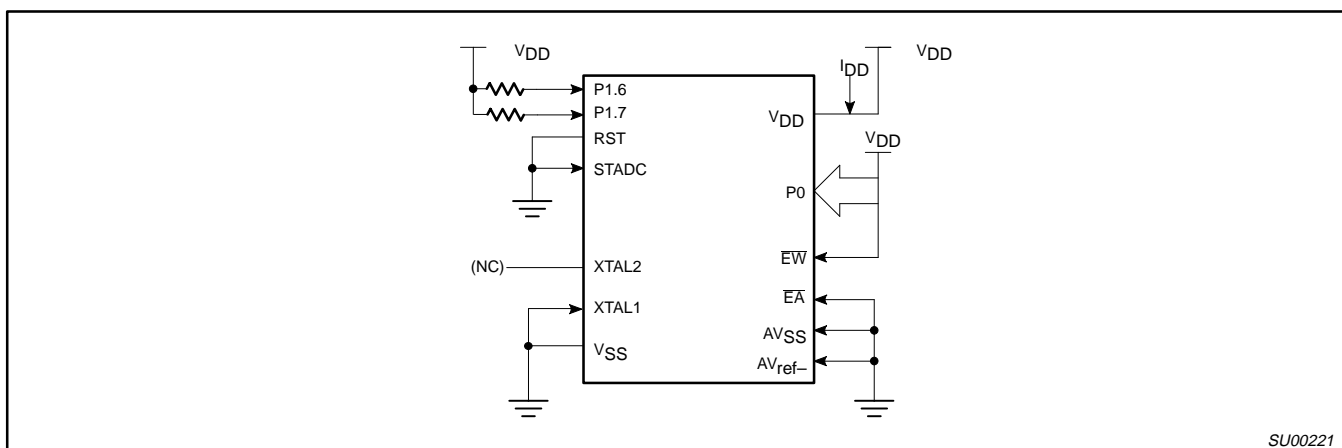


**Figure 12. I<sub>DD</sub> Test Condition, Idle Mode**  
All other pins are disconnected<sup>2</sup>

2. Idle Mode:
  - a. The following pins must be forced to V<sub>DD</sub>: Port 0 and  $\overline{EW}$ .
  - b. The following pins must be forced to V<sub>SS</sub>: RST, STADC, AV<sub>SS</sub>, AV<sub>ref-</sub>, and  $\overline{EA}$ .
  - c. Ports 1.6 and 1.7 should be connected to V<sub>DD</sub> through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I<sub>OL1</sub> spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
  - d. The following pins must be disconnected: XTAL2 and all pins not specified above.



**Figure 13. Clock Signal Waveform for I<sub>DD</sub> Tests in Active and Idle Modes**  
t<sub>CLCH</sub> = t<sub>CHCL</sub> = 5ns



**Figure 14. I<sub>DD</sub> Test Condition, Power Down Mode**  
All other pins are disconnected. V<sub>DD</sub> = 2V to 5.5V<sup>3</sup>

3. Power Down Mode:
  - a. The following pins must be forced to V<sub>DD</sub>: Port 0 and  $\overline{EW}$ .
  - b. The following pins must be forced to V<sub>SS</sub>: RST, STADC, XTAL1, AV<sub>SS</sub>, AV<sub>ref-</sub>, and  $\overline{EA}$ .
  - c. Ports 1.6 and 1.7 should be connected to V<sub>DD</sub> through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I<sub>OL1</sub> spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
  - d. The following pins must be disconnected: XTAL2 and all pins not specified above.

# Single-chip 8-bit microcontroller

# 87C552

## EPROM CHARACTERISTICS

The 87C552 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V<sub>PP</sub> (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C552 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C552 manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 15 and 16. Figure 17 shows the circuit configuration for normal program memory verification.

## Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 15. Note that the 87C552 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 15. The code byte to be programmed into that location is applied to port 0. RST, PSEN, and pins of ports 2 and 3 specified in Table 3 are held at the "Program Code Data" levels indicated in Table 3. The ALE/PROG is pulsed low 25 times as shown in Figure 16.

To program the encryption table, repeat the 25-pulse programming sequence for

addresses 0 through 1FH, using the "Pgm Encryption Table" levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25-pulse programming sequence using the "Pgm Lock Bit" levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the EA/V<sub>PP</sub> pin must not be allowed to go above the maximum specified V<sub>PP</sub> level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V<sub>PP</sub> source should be well regulated and free of glitches and overshoot.

## Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 17. The other pins are held at the "Verify Code Data" levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

## Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips Components

(031H) = 94H indicates 87C552

## Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

## Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to the light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000μW/cm<sup>2</sup> rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient. Erasure leaves the array in an all 1s state.

**Table 3. EPROM Programming Modes**

MODE	RST	PSEN	ALE/PROG	EA/V <sub>PP</sub>	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V <sub>PP</sub>	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V <sub>PP</sub>	1	0	1	0
Pgm lock bit 1	1	0	0*	V <sub>PP</sub>	1	1	1	1
Pgm lock bit 2	1	0	0*	V <sub>PP</sub>	1	1	0	0

### NOTES:

- 0 = Valid low for that pin; 1 = valid high for that pin.
- V<sub>PP</sub> = 12.75V ±0.25V.
- V<sub>DD</sub> = 5V ±10% during programming and verification.
- ALE/PROG receives 25 programming pulses while V<sub>PP</sub> is held at 12.75V. Each programming pulse is low for 100μs (±10μs) and high for a minimum of 10μs.

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Single-chip 8-bit microcontroller

87C552

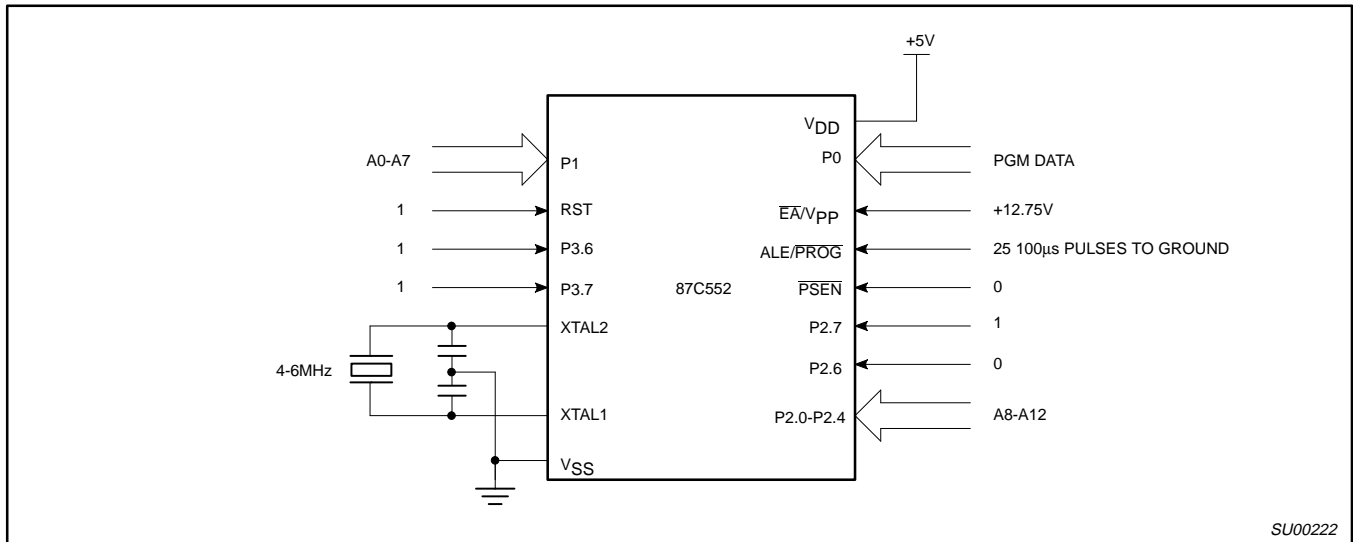


Figure 15. Programming Configuration

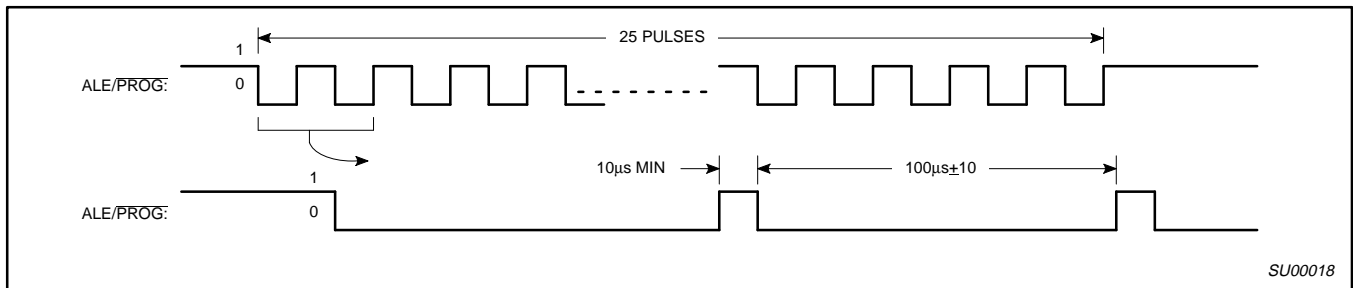


Figure 16. PROG Waveform

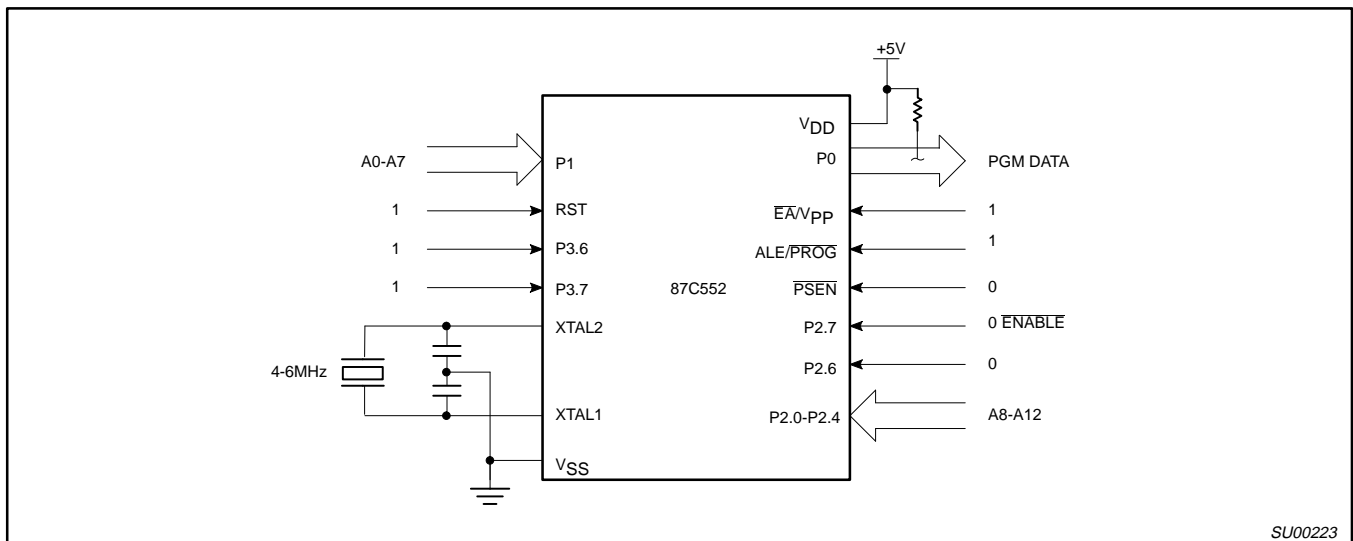


Figure 17. Program Verification

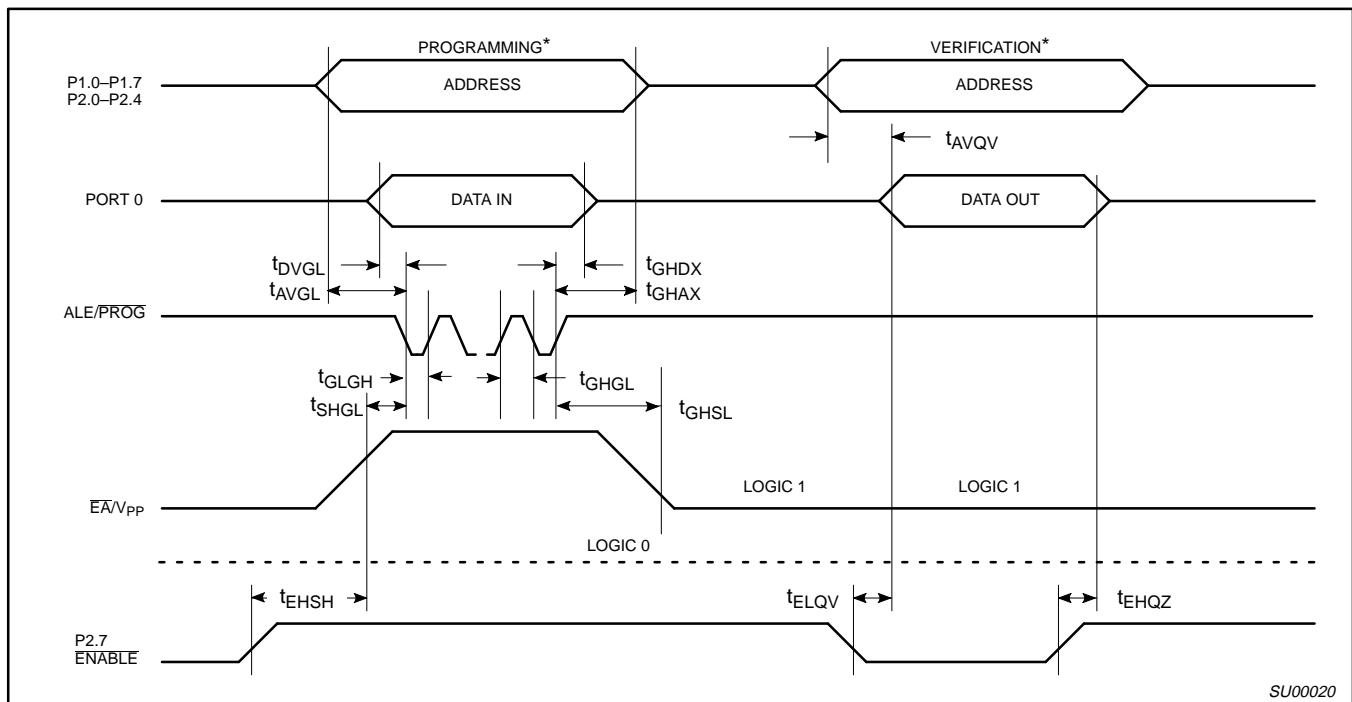
# Single-chip 8-bit microcontroller

# 87C552

## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T<sub>amb</sub> = 21°C to +27°C, V<sub>DD</sub> = 5V±10%, V<sub>SS</sub> = 0V

SYMBOL	PARAMETER	MIN	MAX	UNIT
V <sub>PP</sub>	Programming supply voltage	12.5	13.0	V
I <sub>PP</sub>	Programming supply current		50	mA
1/t <sub>CLCL</sub>	Oscillator frequency	4	6	MHz
t <sub>AVGL</sub>	Address setup to $\overline{\text{PROG}}$ low	48t <sub>CLCL</sub>		
t <sub>GHAX</sub>	Address hold after $\overline{\text{PROG}}$	48t <sub>CLCL</sub>		
t <sub>DVGL</sub>	Data setup to $\overline{\text{PROG}}$ low	48t <sub>CLCL</sub>		
t <sub>GHDx</sub>	Data hold after $\overline{\text{PROG}}$	48t <sub>CLCL</sub>		
t <sub>EHS</sub>	P2.7 (ENABLE) high to V <sub>PP</sub>	48t <sub>CLCL</sub>		
t <sub>SHGL</sub>	V <sub>PP</sub> setup to $\overline{\text{PROG}}$ low	10		µs
t <sub>GHSL</sub>	V <sub>PP</sub> hold after $\overline{\text{PROG}}$	10		µs
t <sub>GLGH</sub>	$\overline{\text{PROG}}$ width	90	110	µs
t <sub>AVQV</sub>	Address to data valid		48t <sub>CLCL</sub>	
t <sub>ELQZ</sub>	ENABLE low to data valid		48t <sub>CLCL</sub>	
t <sub>EHQZ</sub>	Data float after ENABLE	0	48t <sub>CLCL</sub>	
t <sub>GHGL</sub>	$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low	10		µs



\* FOR PROGRAMMING VERIFICATION SEE FIGURE 17.  
FOR VERIFICATION CONDITIONS SEE TABLE 3.

Figure 18. EPROM Programming and Verification



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.