MICROCHIP

AN598

Plastic Packaging and the Effects of Surface Mount Soldering Techniques

Author: *John Barber*
Surface Mount Technology Team

PURPOSE

This application note is intended to inform and assist the customers of Microchip Technology Inc. with Surface Mount Devices (SMD's). The process of packaging a semiconductor in plastic brings to pass a somewhat unlikely marriage of different materials. In order to minimize potential adverse effects of surface mount solder techniques, it is worthwhile to understand the interaction of the package materials during the time they are subjected to thermal stress. Understanding both the limits of thermal stressing that SMD's can withstand and how those stresses interact to produce failures are crucial to successfully maintaining reliability in the finished product. A recommended Infrared (IR) solder profile is provided as a reference later.

The electronics industry has moved to smaller and thinner surface mount packaging in the progress toward miniaturization of circuits. This trend has necessitated the use of lower profile and smaller footprint packages. There has been an increase in reliability problems corresponding with the shrinking size of plastic SMD's. These problems manifest themselves in such ways as moisture sensitivity, cracked packages, open bond wires and intermittent continuity failures. Problems of this type are not present in the devices prior to assembly onto printed circuit boards but are the result of thermally induced stressing to the part during assembly or any rework such as desoldering.

WHAT CAN HAPPEN DURING THE SOLDER PROCESS

In surface mount soldering both the body and leads are intentionally heated. This direct heating of the reduced sized device package is at the heart of the problems experienced with Surface Mount Technology (SMT). Older techniques were concerned with the heating of the leads only. Some degree of heating was present in the body due to the thermal conductivity of the leadframe but this did not produce the same level of stress that devices are now subject to with SMT.

The heat from soldering causes a buildup of additional stresses within the device that were not present from the manufacturing process. Board level solder processes, such as IR reflow and Vapor phase reflow, are well-known areas where temperatures can reach levels sufficient to cause failure of the package integrity. A plastic semiconductor package forms a rigid system where the various components are locked together. Differences in the physical expansion rate of materials will result in internal package stresses because the constituent parts cannot move. When a package is heated, the stresses in the device are applied to the die in such a way that the maximum areas of stress[1] are at the corners. Forces can build to the point where the areas of adhesion between different components of the package give way causing device failure. Failure modes associated with excess stress include delamination of surfaces, fracturing of bond wires, die cracking, cratering of bond pads and package cracking.

Moisture sensitivity of plastic packages has been a concern for semiconductor manufacturers. Moisture can and will permeate any molding compound. The rate of permeation will vary with package compound thickness and type. Relative humidity will also play a role in the time required to saturate a device.

Moisture content will affect the ability of a device to withstand the stresses of surface mount soldering. If sufficient moisture is present inside of a device during soldering, high temperatures can cause steam which has the potential to crack the package. This type of damage is commonly called "pop-corning"[2].

Moisture can lead to corrosion of exposed aluminum metallization inside the device. Fortunately, a film of water is required[3] for corrosion to take place. Water vapor alone is not sufficient to produce the onset of corrosion. It is difficult to collect a film of water inside a package where there is no defect.

Chemical compatibility is important to control corrosion of aluminum (especially in the presence of moisture). Most molding compounds and die attach epoxies contain free ions that can lead to corrosion under conditions where moisture is available to support the chemical reaction(s). Careful selection and handling of materials minimize the number of chemical impurities in the device that could lead to corrosion.

© 1995 Microchip Technology Inc.

MATERIAL INTERACTIONS

To understand the significance of what is happening to a device during solder reflow, it is necessary to understand something about a few specific material properties and how those properties interact. Physical properties of interest[4] are listed for reference in Table 2. These properties will be defined as needed to explain various concepts.

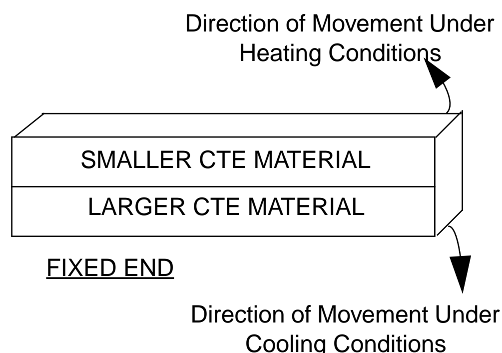
There are five major components used in a plastic package. Basic package components are: (1) epoxy molding compound, (2) leadframe made of copper or Alloy 42, (3) die attach epoxy, (4) silicon die and (5) gold bond wires. Molding compounds have several significant contributing factors that define their performance. These must be considered by the manufacturer when a selection is made. These items are Temperature of Glass Transition (Tg), Coefficient of Thermal Expansion (CTE), moisture absorption characteristics, flexural modulus and strength, and thermal conductivity. In reality, molding compound suppliers provide the test bed for development of compounds, only a few of the very large semiconductor manufacturers have published data[5] suggesting independent experimentation into this area. Leadframes used by Microchip are copper with a silver plated area for die attach and wire bonding. Die attach material is typically a silver filled epoxy. The silver is added for thermal and electrical conduction. Plastic devices have gold bond wires.

Thermally induced transients generated during surface mount soldering can have a significant impact on the reliability of plastic encapsulated devices in the field. In most cases, thermal transients below 125°C are not of sufficient magnitude to cause damage to the part. As a device experiences a significant thermal transient, such as would result from IR reflow soldering, the differing materials expand and contract at unequal rates. The CTE describes the behavior of a material as it expands or contracts when subjected to a temperature change. Materials with similar expansion coefficients will have similar thermal behavior if the phase boundaries are not approached. The CTE characterizes performance over a given temperature range. Table 2 shows that there is a change in the coefficient (ΔCE) of roughly 12.9 (16 - 3.1 = 12.9) between a copper leadframe and silicon, and a ΔCE of 4.4 (7.5 - 3.1 = 4.4) between silicon and lowest stress molding compounds available. The rate of expansion and contraction is not a simple linear relationship with temperature change. The rate can vary dramatically with the phase of the material. For example, molding compounds will greatly increase the rate of expansion when temperatures above the Tg is reached.

In general terms, Tg is the temperature where the material changes from a solid to something more like a plastic or vice versa. More precisely, the temperature of glass transition would be the temperature at which atoms, in chains of 30 to 40 atom groups, start to move. Generally, Tg is in the area of 170°C for molding compounds. Several factors affect Tg such as the basic formulation of the resin from the supplier, cure time and the temperature used in the manufacturing process. A common misconception when trying to relate to these concepts is to assume that the entire package is at the same temperature at any given moment in time. This is not the case.

To aid in understanding the effects of CTE mismatching, take, for example, a bi-metallic strip. They can be found in every automobile and are used in turn signal flasher units for controlling the flashing action of the lights used as turn indicators. Inside the flasher unit the contact arm is formed by use of a bi-metallic strip to make and break electrical contact.

The metals used in the construction of a bi-metallic strip have different CTE's and are specifically chosen to produce a desired effect. These two materials are bonded so that they move together. In the automobile example, current flowing through the bi-metallic strip causes local heating of the strip. Due to the unequal CTE's, the strip will bend away from the contact as it is heated which causes the circuit to open. When current stops flowing in the strip, heating also stops. The bending action of the strip is produced by unequal expansion on one side of the strip. As the strip cools, it will move back thus making contact again allowing current induced heating which starts the cycle over again. In similar fashion as bi-metallic strip, the die in a plastic package will be stressed when subjected to a thermal transient.



Adhesion of materials is a matter of importance since it is in areas of delamination that moisture can collect. The collecting of moisture can lead to corrosion problems.

Differing rates of expansion and contraction can make joining two materials a distinct challenge. Especially if the materials are significantly different in other characteristics that affect surface adhesion. Some materials that are not suitable for use in the packaging system require special adhesion promoting modifications of the surfaces. The topic of adhesion is beyond the scope of this work, but is an important factor and should be given careful attention[6].

© 1995 Microchip Technology Inc.

The property known as "Fracture Toughness" is the ability of the material to resist the propagation of a fracture once the defect has been initiated. Silicon has a very low fracture toughness, therefore, a fracture will readily propagate in silicon. An example of a material at the other end of the spectrum would be Gold, one of the ductile metals, which has a high fracture toughness. This property is responsible for the tendency for glass or tungsten carbide to shatter rather than simply chip or crack. In semiconductor devices, fracture toughness should be considered when cratering and die cracking are a problem.

The closest point to a zero stress state in a plastic package is at the temperature used to cure the molding compound (≅175°C). Present plastic molding compounds are thermosetting polymers. Thermosetting means that the compound sets up and becomes hard as a result of being heated. A cooling cycle after the set up period does not undo the process. The molding compound is held at an elevated temperature for the time period required to harden or cure. During the subsequent cooling, after cure, stresses are trapped in the package because of the differing CTE's. This trapping of stress results in a net compressive force, at room temperature, on the die surface in a plastic molded device. As external stresses such as thermal stress from soldering are presented, if stresses are of sufficient magnitude, the material strength will be exceeded resulting in package damage. Manufacturing processes tend to leave stresses trapped inside the devices. Thickness of the die attach material is regulated to control stressing levels due to its presence. A thin die attach will result in higher tensile stress on the die surface after die attach. The interaction of the die attach material and the molding compound result in the compressive stress on the die surface[7] after packaging. Low stress molding compounds are used on SMD's to minimize the thermal stresses generated during soldering operations.

FAILURE MODES AND MECHANISMS

Let us now review the types of damage that may be seen as a result of SMT soldering. Package damage may be manifested in several ways and may not always result in immediate device failure. Following is a list of failure types and their morphology:

1. Delamination of the molding compound along the leadframe interface and or die surface can take place. This delamination, or separation, can provide a path for moisture and contaminant ingress and pooling along the interfaces where the materials are no longer adhering to each other. This condition may lead to corrosion related problems[8].
2. Cracking of the mold compound can produce immediate failure if the crack crosses a bond wire or it can allow similar moisture effects[9] as in delamination. It can also produce intermittent contact problems.
3. Cracking of the die is generally seen as a functional failure but can be temperature sensitive if the crack is in a more benign area of the die.
4. Cratering of wire bonds is characterized as a phenomenon where portions of the silicon below the ball bond are fractured. The ball bonds pull up "plugs" or "chunks" of silicon, thereby, leaving crater shaped damaged spots in the bulk silicon below the bond pad. Cratering is a possible result of lateral stress on ball bonds. A cratering failure will typically but not always show up during electrical testing. However, it can lay dormant until another temperature excursion comes along which causes the Al metal conductor (bond pad) to open. This is a result of the soft nature of the aluminum used for interconnects in semiconductor devices. The silicon below a bond pad can be damaged without breaking contact in the aluminum. Intermittent or thermally sensitive continuity failures may be produced.
5. Moisture inside the device may collect in the die attach, along material interfaces (primarily leadframe to mold compound and leadframe to die surface) or in the molding compound. Rapid heating causes pressure build up as the moisture expands. This results in delamination and cracking of the package along with the failure modes associated with those phenomena.
6. Corrosion is heavily related to moisture effects and is intensified by delamination and cracks. The typical failure mode for corrosion is loss of continuity since the area most often affected is in the bond pads where there is no passivation layer to give additional protection to the metal.

HOW TO CORRECT THIS PROBLEM: A CASE STUDY

After the device leaves the factory there are two things that need to be done to maintain reliability.

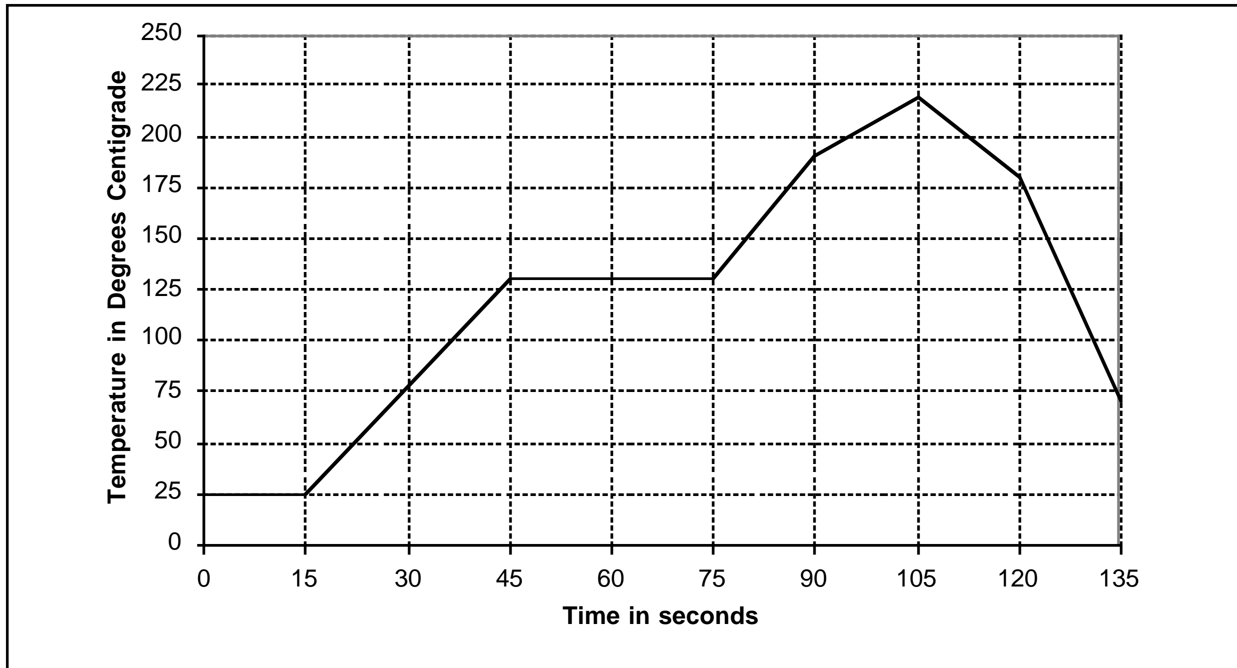
1. The exposure to thermal stressing needs to be minimized. This is not always an easy task in light of the varied components that may go onto a single board. Some will require different conditions to solder due to there bulk size.

   Microchip carried out a partial factorial experiment on 32-lead PLCC devices with the intent of verifying an industry standard profile and providing a specification for our various customers. The devices were subjected to IR solder reflow profiles with ramp rates ranging from 1.5°C/second to 4°C/second and maximum temperatures from 220°C to 310°C (Table 1).

TABLE 1: 32-LEAD PLCC PACKAGE PARTIAL FACTORIAL EXPERIMENT

Variables used in the analysis	Conditions								
M = Maximum Temperature (C)	220	235	250	265	280	295	310	7	
R = Ramp Rate (C/second)	1.5	2	3	4				4	
P = Number of Passes	1	2						2	56 Total Conditions

EXAMPLE 1: IR REFLOW PROFILE



1. (Continued)

No drypack state was employed and the parts were allowed to sit on the shelf in excess of 30 days prior to temperature exposure. The RH of the room was not recorded but is estimated to be approximately 60%. This condition was employed to insure that worst case conditions were evaluated.

Our experiments, to determine optimum soldering temperatures, indicated that a maximum temperature of 220°C should be observed during solder processing. The temperature ramp rate was found to be a less significant factor but should be kept in the range of 2 to 5°C per second. Very slow ramp rates, i.e. those of less than 2°C per second, show a slight decrease in performance. Ramp rates of 3°C showed the best performance and should be used whenever possible. Results from the experiment independently confirm the exposure recommendations set forth in IPC-SM-786[10]. A sample profile for IR reflow is illustrated by the graph in Example 1.

Prior to exposure to the IR temperature profiles all parts were electrically good and were examined by Scanning Acoustic Microscopy (SAM) to verify a defect free state and establish a baseline. After exposure to the IR profiles, all parts were again tested electrically and examined via SAM. Delamination can be easily detected by use of SAM. No package cracks were observed after temperature exposure. Only limited electrical failures occurred and all were at temperatures above 220°C.

In the experiments a thermocouple was interfaced to the exterior of a device and passed through an IR reflow oven. Both the maximum temperature and ramp rate were recorded in this manner. General trends for temperature sensitivity in relationship to maximum temperature and ramp rate are presented in the graphs shown in Example 2 and Example 3.

Pass/fail criteria for the experiments was primarily the extent of delamination, observed by Scanning Acoustic Microscopy, after exposure to two passes through an IR reflow oven. Top side die delamination and delamination in areas of the leadframe where the bonds are made are classed as unacceptable. Some delamination along non critical areas are classed as acceptable (i.e., no delamination extending to the exterior of the

© 1995 Microchip Technology Inc.

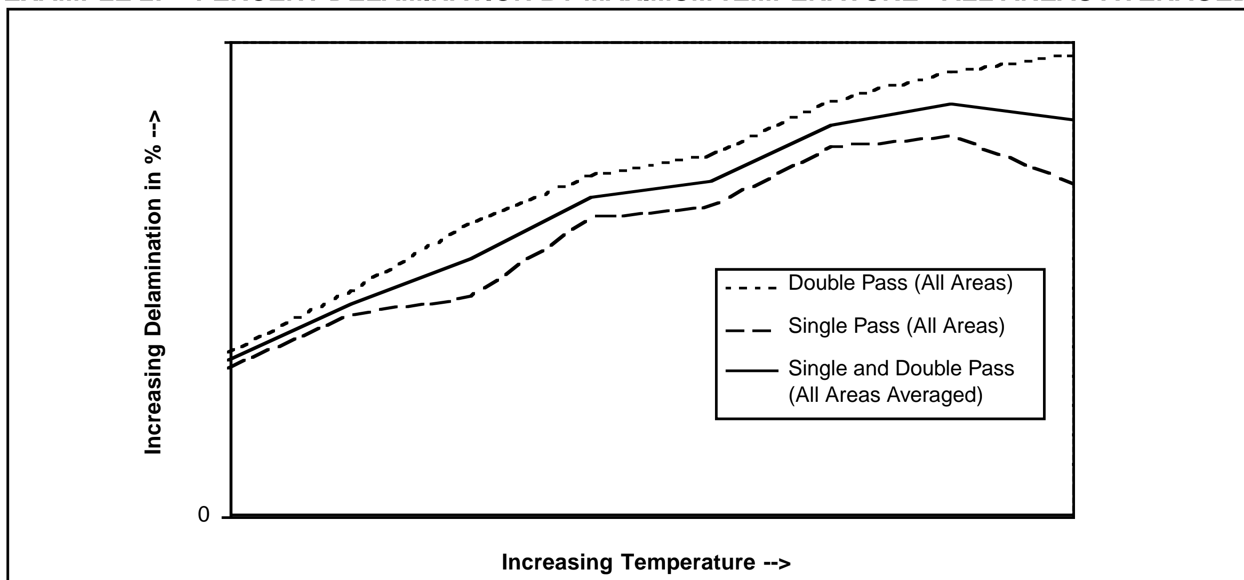
package or covering more than minor portions of the leadframe). Specific information on pass/fail criteria can be found in IPC - SM - 786.

Maximum temperature should not exceed 220°C.
Temperature ramp rate should be between 2 to 5°C per second.

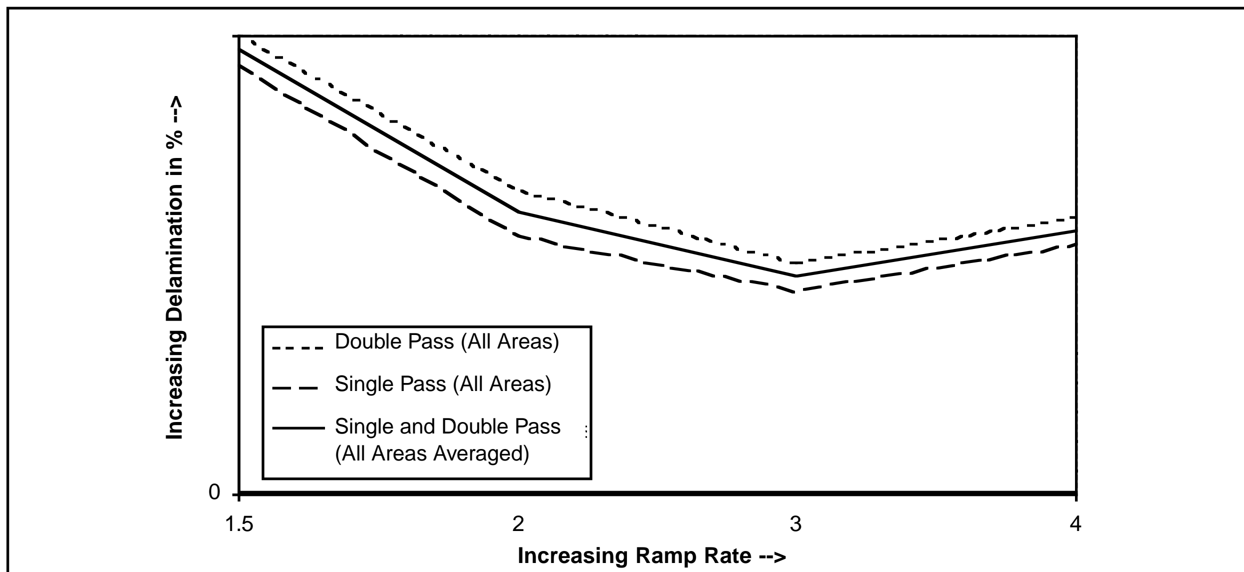
Use of the above temperature profile will increase the reliability of the device following board level assembly.

2. The second item that must be observed is the dry packing of SM devices. Dry packing is a standard product packaging procedure for surface mount devices. This practice guarantees to the customer that devices are shipped in a dry state. All devices are sealed inside plastic bags with a moisture indicator to monitor moisture when they are shipped. Customers should be aware of this practice and maintain the dry packed state until the time of use. Shelf life[11] for opened parts is a function of package style and ambient conditions. A small increase in failure rate will be experienced if the drypack condition is violated.

EXAMPLE 2: PERCENT DELAMINATION BY MAXIMUM TEMPERATURE - ALL AREAS AVERAGED



EXAMPLE 3: DELAMINATION BY RAMP RATE AT 220°C



CONCLUSION

Significant thermal stressing can cause a diverse list of package or device failures. To minimize any damage caused by high temperature exposure, moisture content needs to be controlled in electronic devices.

Experiments conducted by Microchip validate the recommendation of IPC - SM - 786 to limit maximum temperature exposure during surface mount soldering to 220°C. A temperature ramp rate of 2°C/second to 5°C/second will also serve to safeguard the reliability of the device.

Microchip is committed to the principles of continuous improvement. Product reliability and customer satisfaction are a primary focus. For this reason, new packaging technology enhancements are continually evaluated to improve the performance of Microchip devices.

TABLE 2: PHYSICAL PROPERTIES OF COMMON MATERIALS USED IN PLASTIC PACKAGING OF SEMICONDUCTOR DEVICES

Material	Coefficient of Thermal Expansion in 10^6/°C (CTE)	Temp. of Glass Transition in °C (Tg)	Modulus of Elasticity in 10^6 psi (10^3 MPa.) (E)	Tensile Strength in 10^3 psi
Silicon (Si)	2.3-4.2		19-29	16-25
Alloy 42 Leadframe	4.0- 4.7		21	75
Alumina (Al_2O_3)	6.5-8.8		37	25-50
Gold Eutectic Die Attach	14.2		12.5	16
Copper Leadframe	16-18		17.3	60
Pb -- Sn Die Attach	29		1-2.5	1-4
Epoxy Mold Compounds (α_1 is for Temperatures below Tg, (α_2 is for temperatures above Tg)	7.5-28 α_1 20-22 ppm/°C α_2 60-65 ppm/°C[12]	145-170	1.8-3	10-20
Epoxy Die Attach	20-70		0.4	1-8
Polyimide Die Attach	35-60		0.6	1-8
Unfilled Epoxies	60-70			
Unfilled Silicones	300			

© 1995 Microchip Technology Inc.

ENDNOTES

1. Thomas M. Moore and Robert G. McKenna, *Characterization of Integrated Circuit Packaging Materials* (Stoneham: Butterworth - Heinemann, 1993), pp. 68.
2. A.S. Chen, et al., "A Study of the Interaction of Molding Compound and Die Attach Adhesive, with regards to Package Cracking", Proceedings of the 44th Electronic Components & Technology Conference. 1994, pp. 115-120.

   Michael Tencer, "Moisture Ingress into Nonhermetic Enclosures and Packages. A Quasi-Steady State Model for Diffusion and Attenuation of Ambient Humidity Variations", Proceedings of the 44th Electronic Components & Technology Conference. 1994, pp. 196-209.
3. Thomas M. Moore and Robert G. McKenna, *Characterization of Integrated Circuit Packaging Materials* (Stoneham: Butterworth - Heinemann, 1993), pp. 13.
4. George G. Harman, *Wirebonding In Microelectronics* (International Society for Hybrid Microelectronics, 1991), pp. 160.

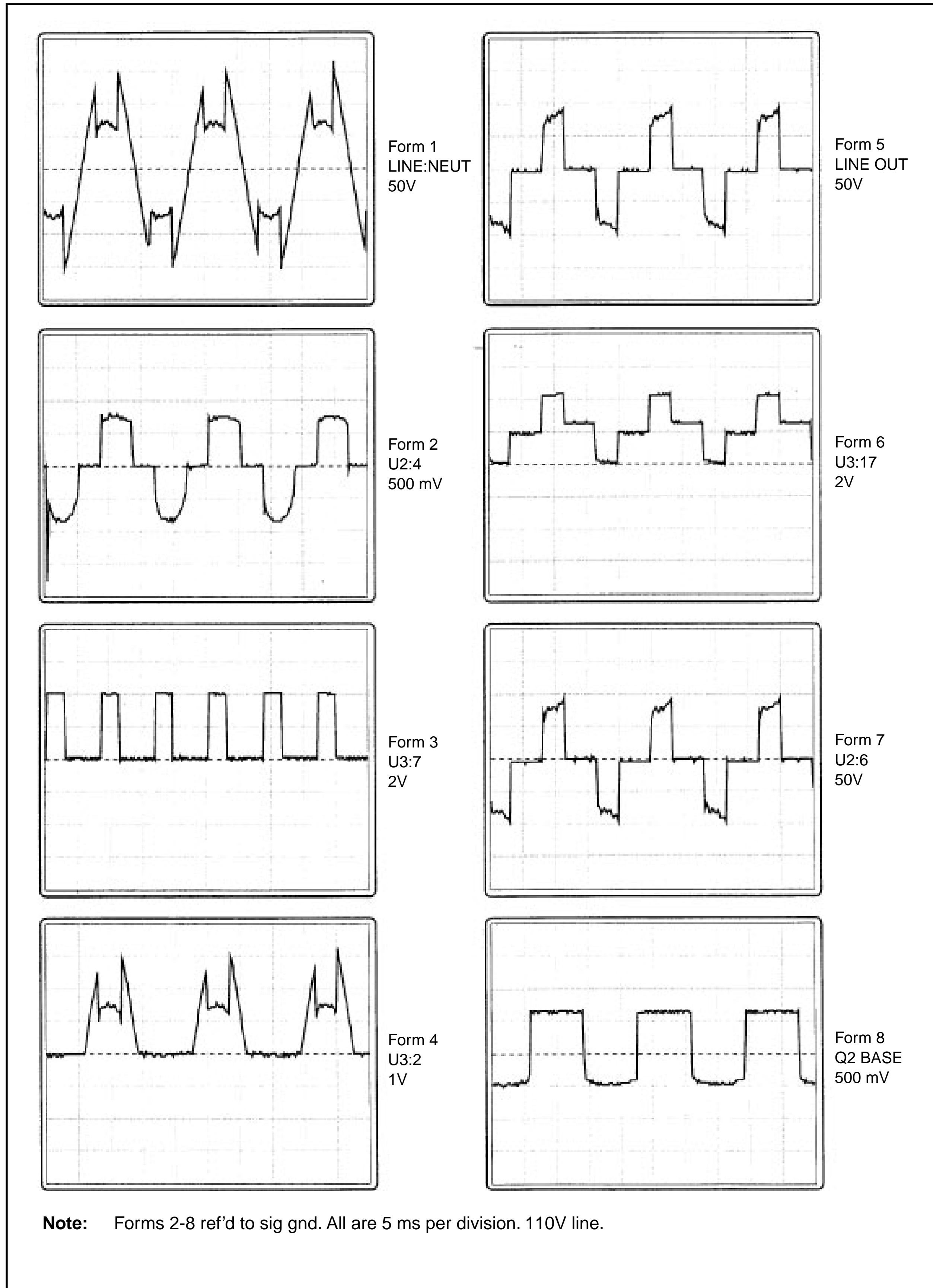
   Justin C. Bolger, Short course notes. *Advanced Microelectronics Assembly Technology: Reliability & Yield Issues of Materials, Plastic Molding and Wire Bonding*, Univ. Of Ariz. February 8-11, 1994, pp. C2.
5. Samuel S. Kim, "Improving Plastic Package Reliability Through Enhanced Mold Compound Adhesion", Tutorial of the International Reliability Physics Symposium, 1992, pp. 2d.1-2d.17.
6. H. Ohsuga, et al., "Development of Molding Compounds Suited for Copper Leadframes", Proceedings of the 44th Electronic Components & Technology Conference. 1994, pp. 141-146.
7. Justin C. Bolger, Short course notes. *Advanced Microelectronics Assembly Technology: Reliability & Yield Issues of Materials, Plastic Molding and Wire Bonding*, Univ. Of Ariz. February 8-11, 1994, pp. C6.
8. T.M. Moore, S.J. Kelsall. "The Impact of Delamination on Stress-Induced and Contamination-Related Failure in Surface Mount IC's", *Proceedings of the International Reliability Physics Symposium*. 1992, pp. 169-176.

   T.R. Conrad and R. L. Shook. "Impact of Moisture/Reflow Induced Delaminations on Integrated Circuit Thermal Performance", Proceedings of the 44th Electronic Components & Technology Conference. 1994, pp. 527-531.
9. T.M. Moore, S.J. Kelsall. *Op. Cit.*, pp. 169-176.
10. IPC - SM - 786A is obtainable from the Institute for Interconnecting and Packaging of Electronic Circuits, 7830 N. Lincoln Ave., Lincolnwood, ILL. 60646.
11. IPC - SM - 786A, Table 4-2 (See endnote above).
12. Thomas M. Moore and Robert G. McKenna, *Characterization of Integrated Circuit Packaging Materials* (Stoneham: Butterworth - Heinemann, 1993), pp. 49.

An Excellent Reference Article --

L.T. Nguyen, "Reliability of Postmolded IC Packages", Transactions of the ASME, Journal of Electronic Packaging, December 1993, Vol. 115, pp. 346-355.

FIGURE 10: MTE1122 CIRCUIT WAVEFORMS



Note: Forms 2-8 ref'd to sig gnd. All are 5 ms per division. 110V line.

© 1995 Microchip Technology Inc.

TABLE 3: BILL OF MATERIALS FOR MTE1122 ENERGY MANAGEMENT CONTROL DEMO BOARD

Item	Qty.	Reference	Value	Desc.ription		Mfg.
1	1	C1	100 µF	16V	electrolytic	
2	1	C2	1 µF	250VAC	film	
3	1	C3	220 µF	16V	electrolytic	
4	2	C4,C5	100 pF		ceramic	
5	1	C6	0.1 µF		ceramic	
6	1	C7	1 µF	50V	electrolytic	
7	1	C8	2.2 µF	250VAC	film	
8	2	C9,C10	0.1 µF	250VAC	film	
9	3	D1,D2, D8	1N4007			
10	1	D3	LED	green		
11	1	D4	1N5226			
12	1	D5	1N4733			
13	2	D6,D7	1N5230			
14	1	L1	100 µH	4632	RF Choke	JW Miller
15	1	Q1	TP2907			
16	1	Q2	TP2222A			
17	1	Q3	Q4015L5			Teccor
18	1	R1	470 1/2W			
19	1	R2	330 1/2W			
20	1	R3	560			
21	1	R4	270 1/2W			
22	2	R5, R15	30K			
23	1	R14	30K 1/2W			
24	1	R6	15K			
25	1	R7	560			
26	1	R8	2.4K			
27	1	R9	1M 1/2W			
28	2	R10,R13	562K 1%			
29	2	R11,R12	12.1K 1%			
30	1	R16	10K			
31	1	U1	TLC271CP	opamp		TI
32	1	U2	TLP3023	opto-triac		Seimens
33	1	U3	MTE1122			Microchip
34	1	Y1	4 MHz	ceramic resonator		
35	1			heatsink	as needed	

Note 1: C2,8,9,10 MUST be AC-rated capacitors. THIS IS CRUCIAL!

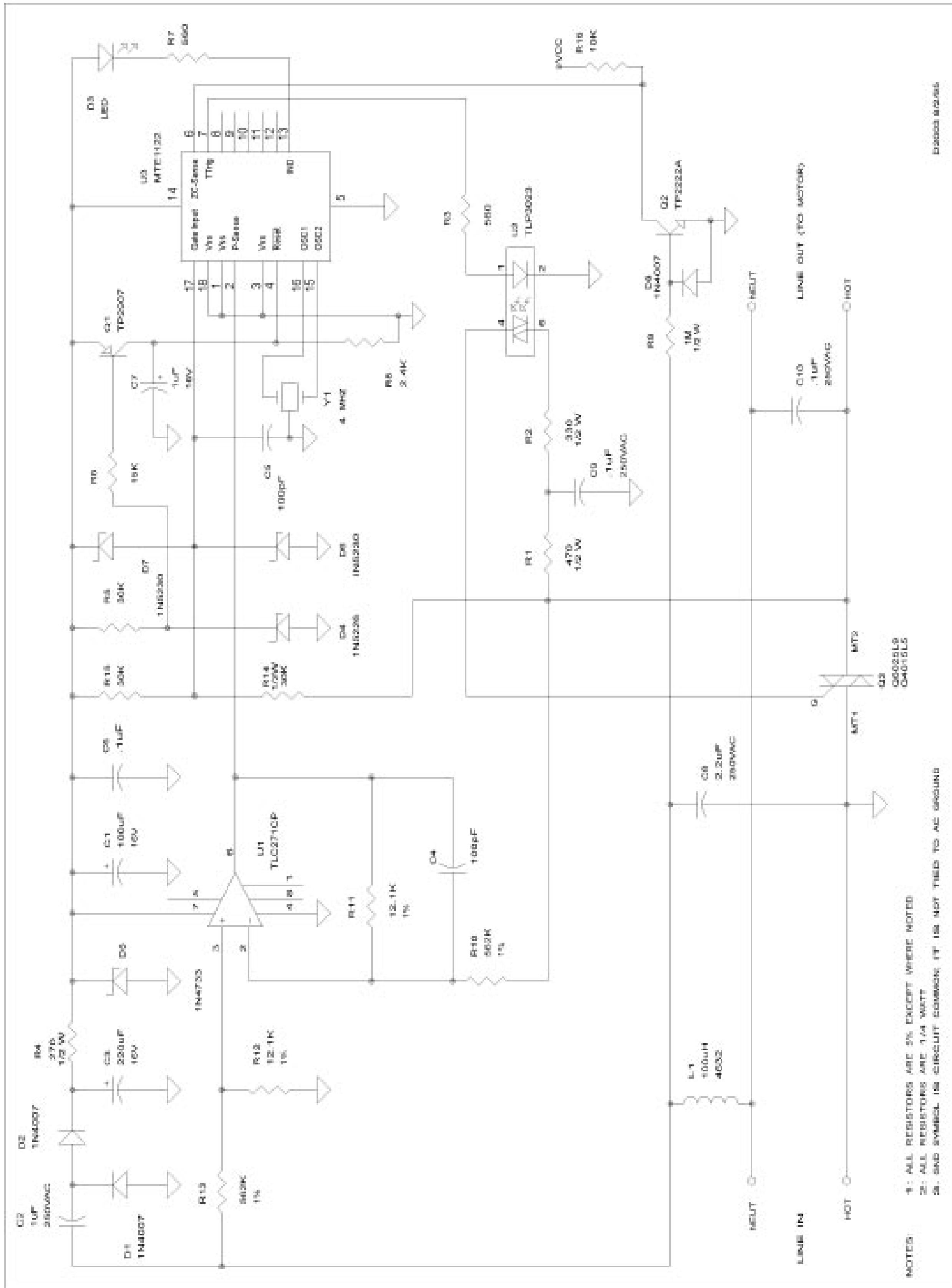
Note 2: Q3 can be sized to fit the load. A 400V 15A part is called out in the parts list and on the schematic; a 600V 25A part is also listed on the schematic for reference. Nearly any triac can be used here, as long as its trigger current does not exceed that supplied by U2 (typically 50 mA). For higher current applications, two SCR's back-to-back perform well. Performance is improved slightly if the device is NOT operated at its current limit.

Note 3: Any opto-triac meeting the current-transfer and current handling specs of the TLP3023 can be used.

Note 4: A heat sink is called out. Its size will depend on the particular Triac used, the operating temperature, and the load. Contact a heat sink manufacturer for specific information.

© 1995 Microchip Technology Inc.

FIGURE 11: SCHEMATIC DIAGRAM



© 1995 Microchip Technology Inc.

WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 786-7277
Technical Support: 602 786-7627
Web: http://www.mchip.com/microchip

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770 640-0034 Fax: 770 640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508 480-9990 Fax: 508 480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 708 285-0071 Fax: 708 285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 214 991-7177 Fax: 214 991-8588

Dayton
Microchip Technology Inc.
35 Rockridge Road
Englewood, OH 45322
Tel: 513 832-2543 Fax: 513 832-2841

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 455
Irvine, CA 92715
Tel: 714 263-1888 Fax: 714 263-1338

New York
Microchip Technology Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

ASIA/PACIFIC

Hong Kong
Microchip Technology
Unit No. 3002-3004, Tower 1
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T. Hong Kong
Tel: 852 2 401 1200 Fax: 852 2 401 3431

Korea
Microchip Technology
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku,
Seoul, Korea
Tel: 82 2 554 7200 Fax: 82 2 558 5934

Singapore
Microchip Technology
200 Middle Road
#10-03 Prime Centre
Singapore 188980
Tel: 65 334 8870 Fax: 65 334 8850

Taiwan
Microchip Technology
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2 717 7175 Fax: 886 2 545 0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire SL8 5AJ
Tel: 44 0 1628 851077 Fax: 44 0 1628 850259

France
Arizona Microchip Technology SARL
2 Rue du Buisson aux Fraises
91300 Massy - France
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Muenchen, Germany
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Pegaso Ingresso No. 2
Via Paracelso 23, 20041
Agrate Brianza (MI) Italy
Tel: 39 039 689 9939 Fax: 39 039 689 9883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shin Yokohama
Kohoku-Ku, Yokohama
Kanagawa 222 Japan
Tel: 81 45 471 6166 Fax: 81 45 471 6122

9/22/95

All rights reserved. © 1995, Microchip Technology Incorporated, USA.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights. The Microchip logo and name are registered trademarks of Microchip Technology Inc. All rights reserved. All other trademarks mentioned herein are the property of their respective companies.