Comlinear Corporation

Wideband, High Speed Operational Amplifiers

CLC300

APPLICATIONS:

- digital communications
- baseband and video communications
- instrument input/output amplifiers
- fast A to D, D to A conversion
- graphic CRT video drive amp
- coaxial cable line driver

FEATURES:

- −3dB bandwidth of 85MHz
- new design topology eliminates gain-bandwidth trade-off
- 3000V/μsec slew rate
- 4ns rise and fall time
- 100mA output current
- low distortion, linear phase

DESCRIPTION:

The CLC300 operational amplifier is a unique, proprietary Comlinear design providing a **DC-85MHz –3dB bandwidth that is virtually independent of gain setting.** Rise and fall times of 4nsec and drive capability of $22V_{pp}$ and 100mA add to the CLC300's impressive specifications.

Ease-of-use is a design goal at Comlinear, and the CLC300 is a success in this area as well. Using the CLC300 is as easy as adding power supplies and a gain-setting resistor. And unlike conventional op amp designs in which optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of −1, maximum slew rate at a gain of +1, et cetera, the CLC300 offers consistent performance at gain settings from 1 to 40 inverting or non-inverting. As a result, designing with the CLC300 is greatly simplified. And since **no external compensation is necessary,** "tweeks" on the production line have been eliminated, making the CLC300 an efficient component for use in production situations.

Flat gain and phase response from DC to 45MHz and superior rise and fall times make the CLC300 an ideal amplifier for a broad range of pulse, analog, and digital applications. A **45MHz full power bandwidth** ($20V_{pp}$ into 100Ω) and 3000V/μsec slew rate eliminate the need for power buffers in many applications such as driving "flash" A to D converters or line-driving. For applications requiring lower power consumption, the CLC300 can operate on supplies as low as 5V. Fast overload recovery (20nsec) helps prevent loss of data in communications applications and flat phase response reduces distortion, even when data must be sent over extended lengths of line.

The CLC300A is packaged in a 24-pin ceramic DIP and is specified over a temperature range of –25°C to +85°C. The CLC300B has been discontinued and is no longer in production.

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

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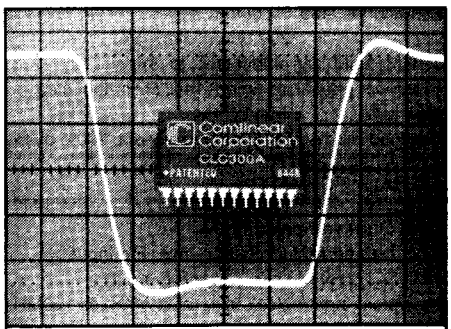
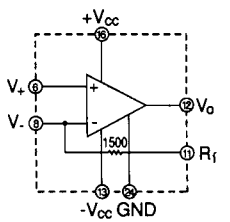
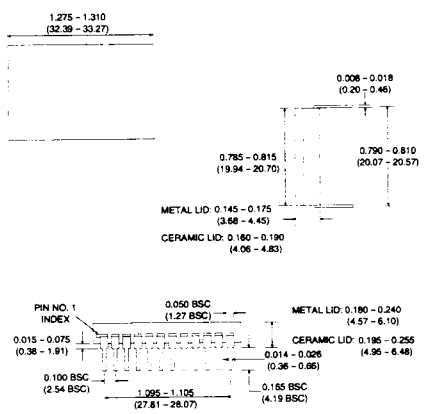




CLC300 Equivalent Circuit Diagram

Pin 11 provides access to a 1500Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired. All undesignated pins are internally unconnected.

Package Dimensions



magnitude of gain [$\lvert V_{out}/V_{in} \rvert$]	4*	20		40	
Parameter and Conditions	typ	min[2]	typ	max[2]	typ	units
FREQUENCY DOMAIN RESPONSE						
• −3dB bandwidth, $V_{out} < 4V_{pp}$	105	75	85		70	MHz
$V_{out} = 20V_{pp}$	45		45		45	MHz
• gain flatness, 100KHz to 20MHz	±0.25		±0.08	±0.3	±0.25	dB
20MHz to 45MHz	±0.5		±0.25	±0.6	±1	dB
• phase shift	1		1.6		2	deg/MHz
• deviation from linear phase, DC to 45MHz	2		3		5	degree
• reverse isolation	60		70		70	dB
• distortion—refer to graphs						
TIME DOMAIN RESPONSE						
• rise and fall time, 5V output step	3		4		5	ns
20V output step	7		7		7	ns
• settling time, 10V output step, to .8%	20		20		25	ns
• overshoot (input rise time ≤1ns), 5V output step	5		5		5	%
• slew rate	3		3		3	V/ns
• overload recovery (<50ns pulse width, 200% overdrive)	20		20		20	ns

GENERAL INFORMATION	min[2]	typ	max[2]	units
• input offset voltage (drift)		10(25)	32	mV(μV/°C)
• input bias current (drift), non-inverting input		10(20)	30	μA(nA/°C)
inverting input		30(50)	100	μA(nA/°C)
• equivalent input noise[1], integrated 5MHz to 100MHz ($R_S = 50\Omega$, gain = 20)		22	56	μV
• second/third harmonic distortion (@ 20MHz, +10dBm)		48	38	−dBc
• input impedance, non-inverting input		100K/3		Ω/pF
• power supply rejection ratio (referred to input)	45	60		dB
• common mode rejection ratio (referred to input)		64		dB
• output drive voltage current		10, 100		V, mA
• supply current		24	33	mA

- supply voltage ($\pm V_{cc}$) 16V (±5V min.)
- output current (I_O) 100mA
- input voltage (V_{imax}) $(\lvert V_{cc} \rvert - 2.5)/A_v$
- common mode input voltage $\pm ½ \lvert V_{cc} \rvert$
- power dissipation, refer to graph
- junction temperature (T_J) 150°C
- operating temperature (T_A) −25 to +85°C
- storage temperature −55 to +150°C
- still air thermal resistance (θ_{ca}) 25°C/W

[1] For Noise Figure, refer to Distortion and Noise Section in text.
[2] All min/max parameters are tested 100% at +25°C, $A_v = +20$, $R_L = 100\Omega$, and $V_{cc} = \pm 15V$.
*refer to Low Gain Operation section.

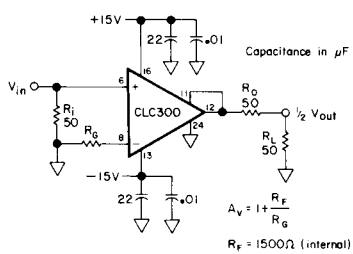


Figure 1: recommended non-inverting gain circuit

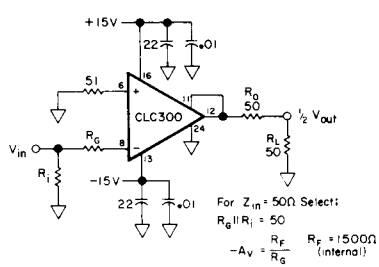
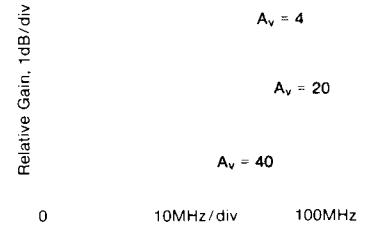
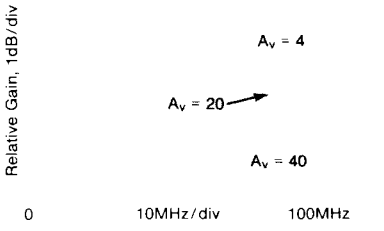


Figure 2: recommended inverting gain circuit

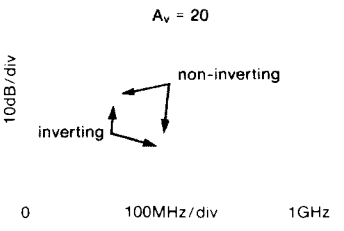
Non-Inverting Gain



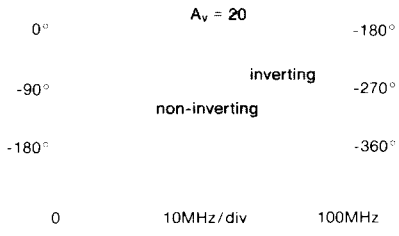
Inverting Gain



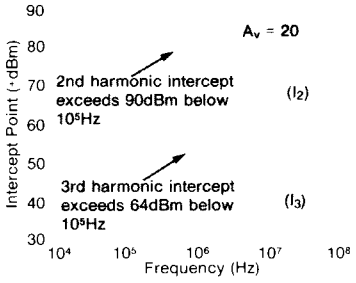
Broadband Inverting and Non-Inverting Gain



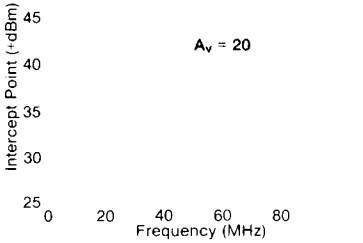
Inverting and Non-Inverting Phase



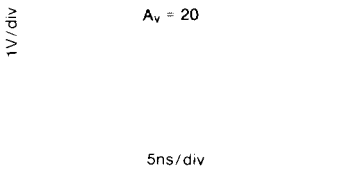
2nd and 3rd Harmonic Distortion Intercept



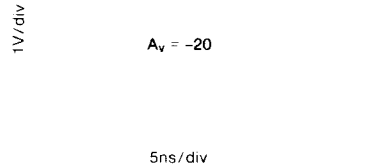
2-Tone 3rd Order Intermod. Intercept



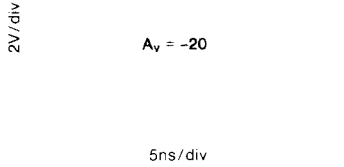
Non-Inverting Small Signal Pulse Response



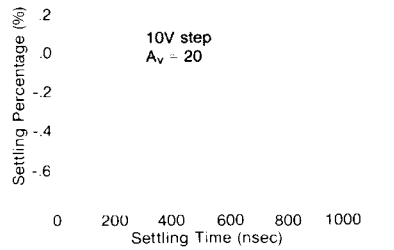
Inverting Small Signal Pulse Response



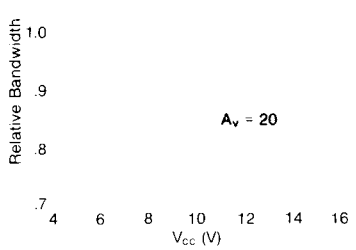
Large Signal Pulse Response



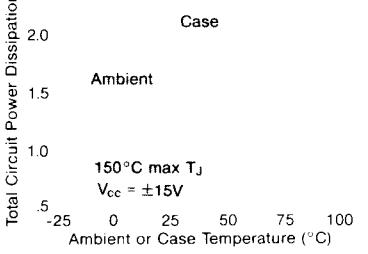
Settling Time



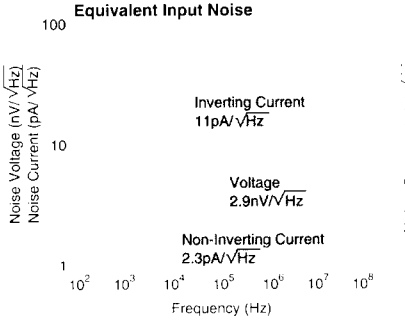
Relative Bandwidth vs. V_{cc}



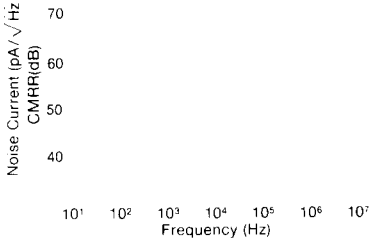
Power Dissipation Derating



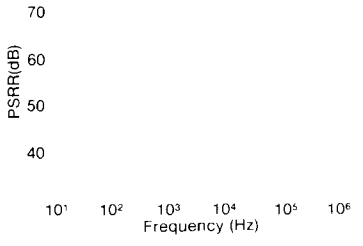
Equivalent Input Noise



Common Mode Rejection Ratio



Power Supply Rejection Ratio



Layout Considerations (continued)

During pc board layout keep all traces short and direct. The resistive bodies of R_F and R_G should be as close as possible to pin 8 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 8 and 6. In other areas, use as much ground plane as possible on one side of the pc board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF should be close to pins 13 and 16. Larger tantalum capacitors should also be placed within one inch of these pins. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches. Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase.

Controlling Bandwidth and Passband Response

As with any op amp, the ratio of the two feedback resistors R_F and R_G determines the gain of the CLC300. Unlike conventional op amps, however, the closed loop pole-zero response of the CLC300 is affected very little by the value of R_G. R_G scales the magnitude of the gain, but does not change the value of the feedback. This is possible due to a proprietary circuit topology. R_F does influence the feedback and so the CLC300 has been internally compensated for optimum performance with $R_F = 1500\Omega$, but any value of $R_F > 500\Omega$ may be used with a single capacitor placed between pins 8 and 12 for compensation. See Table1. As R_F decreases, C_c must increase to maintain flat gain. Large values of R_F and C_c can be used together or separately to reduce the bandwidth. This may be desirable for reducing the noise bandwidth in applications not requiring the full frequency response available.

Table1: Bandwidth versus R_F and C_c (A_V = +20)

R_F (KΩ)	C_c (pF)	$f_{\pm 0.3dB}$ (MHz)	$f_{-3.0dB}$ (MHz)
10.0	0	2	5
5.0	0	3	12
2.0	0	8	40
1.5	0	45	85
1.0	0.3	90	115
.75	1.1	95	130
0.50	1.9	110	135

Low Gain Operation

The small amount of stray capacitance present at the inverting input can cause peaking which increases with decreasing gain. The gain setting resistor R_G is effectively in parallel with this capacitance and so a frequency domain pole results. With small R_G (Gain > 8), this pole is at a high frequency and it affects the closed loop gain of the CLC300 only slightly. At lower values of gain, this pole becomes significant. For example, at a gain of +2, the gain may peak as much as 3dB at 75MHz, and have a bandwidth exceeding 150MHz. The same behavior does not exist for low inverting gains, however, since the inverting input is a virtual ground which maintains a constant voltage across the stray capacitance. Even at inverting gains $\ll 1$, the frequency response remains unchanged.

To avoid the peaking at low non-inverting gains, place a resistor R_p in series with the input signal path just ahead of pin 6, the non-inverting input. This forms a low pass filter with the capacitance at pin 6 which can be made to cancel the peaking due to the capacitance at pin 8, the inverting input. At a gain of +2, for example, choosing R_p such that the source impedance in parallel with R_i (see Figure 1), plus R_p equals 175Ω will flatten the frequency response. For larger gains, R_p will decrease.

Settling Time, Offset, and Drift

After an output transition has occurred, the output settles very rapidly to final value and no change occurs for several microseconds. Thereafter, thermal gradients inside the CLC300 will cause the output to begin to drift. When this cannot be tolerated, or when the initial offset voltage and drift is unacceptable, the use of a composite amplifier is advised. This technique reduces the offset and drift to that of a monolithic, low frequency op amp, such as an LF356A. The composite amplifier technique is fully described in the CLC103 Data Sheet.

A simple offset adjustment can be implemented by connecting the wiper of a potentiometer, whose end terminals connect to ±15V, through a 20K resistor to pin 8 of the CLC300. Variations of this technique are described in Application Note 200-1, Designer's Guide for 200 Series Op Amps.

Overload Protection

To avoid damage to the CLC300, care must be taken to insure that the input voltage does not exceed $(|V_{cc}| - 2.5)/A_V$. High speed, low capacitance diodes should be used to limit the maximum input voltage to safe levels if a potential for overload exists.

If in the non-inverting configuration the resistor R_i, which sets the input impedance, is large, the bias current at pin 6, which is typically a few μA but which may be as large as 18μA, can create a large enough input voltage to exceed the overload condition. It is therefore recommended that $R_i < [(|V_{cc}| - 2.5)/A_V]/(18\mu A)$.

Distortion and Noise

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC300. First, convert the output voltage (V_O) to $V_{RMS} = V_{pp}/2\sqrt{2}$ and then to $P = 10\log_{10}(20V_{RMS}^2)$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$ dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$ dB below P, as will the two tone third order intermodulation products. These approximations are useful for $P < -1$dB compression levels.

Approximate noise figure can be determined for the CLC300 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB:

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off of the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes

For information on the use of the CLC300 in a wide variety of applications, refer to application note AN200-1.