

FMM5007VF

Ku Band Power Amplifier MMIC

FEATURES

- High Output Power: 31.0dBm(typ.)
- High Linear Gain: 20.0dB(typ.)
- Low Input VSWR
- Impedance Matched $Z_{in}/Z_{out} = 50\Omega$
- Small Hermetic Metal-Ceramic SMT Package(VF-pkg)



DESCRIPTION

The FMM5007VF is a MMIC amplifier that contains a three-stage amplifier, internally matched, for standard communications in the 14.0 to 14.5GHz frequency range. This product is well suited for VSAT applications as a driver or output stage.

Eudyna's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
DC Input Voltage	VDD	12	V
DC Input Voltage	VGG	-7	V
Input Power	Pin	20	dBm
Storage Temperature	Tstg	-55 to +125	°C

RECOMMENDED OPERATING CONDITION

Item	Symbol	Condition	Unit
DC Input Voltage	VDD	10	V
DC Input Voltage	VGG	-5	V
Operating Case Temperature	Tc	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (Case Temperature Tc=25°C)

Item	Symbol	Condition	Limit			Unit
			Min.	Typ.	Max.	
Frequency	f	VDD=10V VGG=-5V f=14.0-14.5GHz	14.0	-	15	GHz
Output Power at 1dB G.C.P.	P1dB		30.0	31.0	-	dBm
Linear Gain	G		18.0	20.0	-	dB
Gain Flatness	ΔG		-	1.0	1.5	dB
Input VSWR	VSWRi		-	2:1	2.3:1	-
Output VSWR	VSWRo		-	2.3:1	3:1	-
Power Monitor (Rmon=10Kohm)	Vmon		Pout=30dBm	-	3.5	-
DC Input Current	IDD	VDD=10V	-	1000	1200	mA
DC Input Current	IGG	VGG=-5V	-	15	20	mA

G.C.P.:Gain Compression Point

ESD	Class 0	~ 199V
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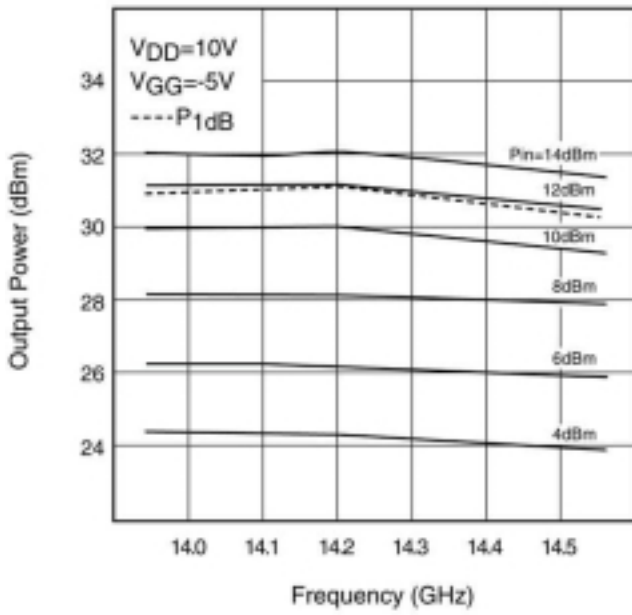
Note : Based on EIAJ ED-4701 C-111A(C=100pF, R=1.5k Ω)

CASE STYLE	VF
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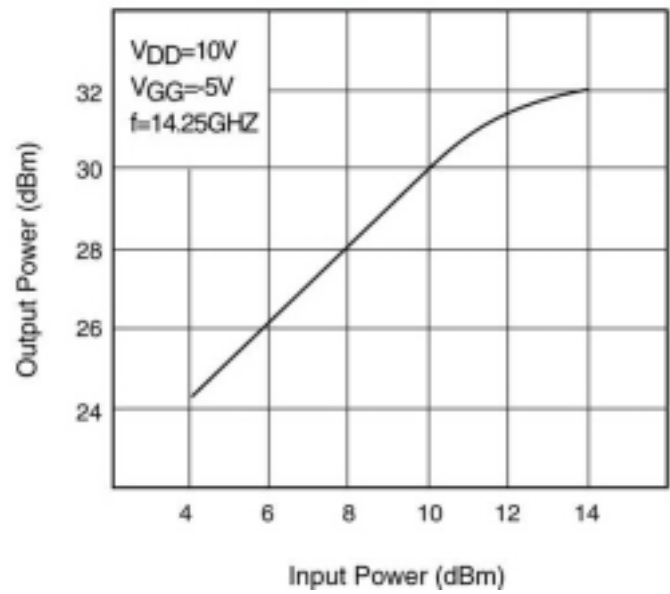
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OUTPUT POWER vs. FREQUENCY



OUTPUT POWER vs. INPUT POWER

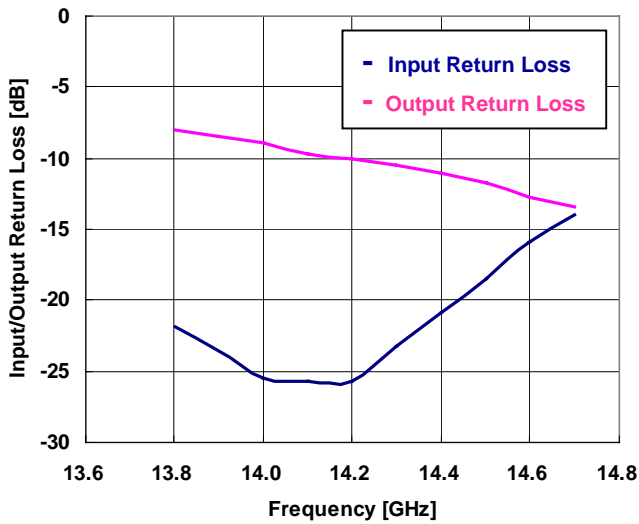


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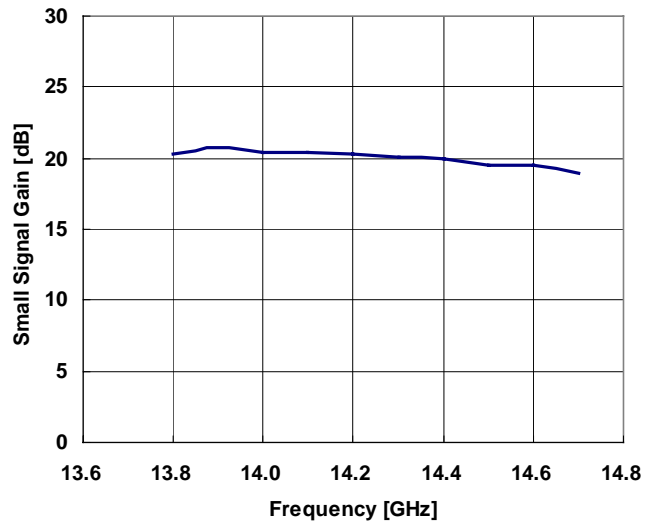
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■ S-PARAMETER

INPUT/OUTPUT RETURN LOSS vs. FREQUENCY
Vdd=10V, Vgg=-5V



SMALL SIGNAL GAIN vs. FREQUENCY
Vdd=10V, Vgg=-5V



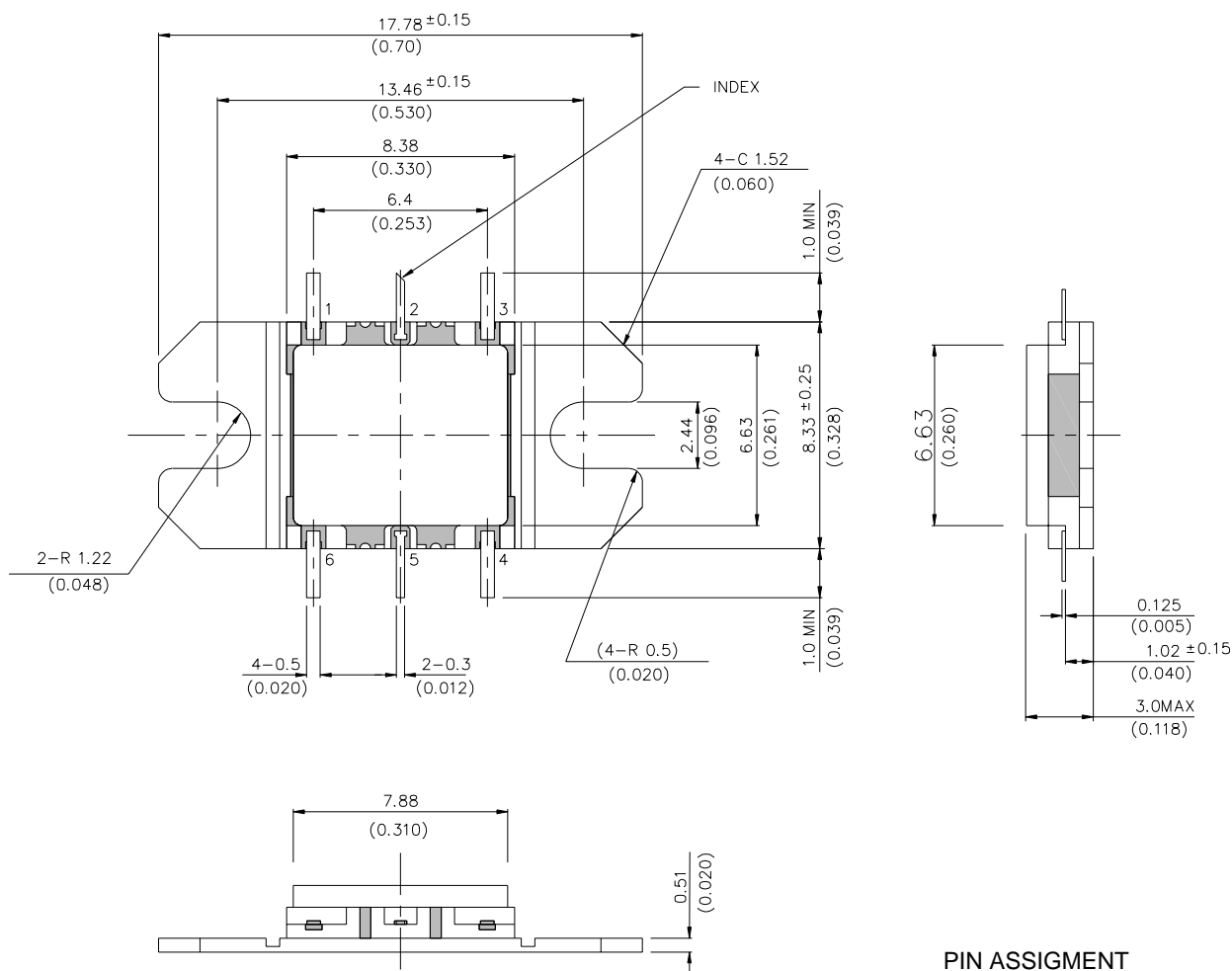
VDD=10V, VGG=-5V

Frequency [MHz]	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
13800	0.081	150.5	10.412	78.2	0.004	-109.4	0.400	-45.0
13900	0.066	144.4	10.869	55.9	0.004	-165.3	0.377	-44.4
14000	0.053	141.5	10.443	46.5	0.009	-163.0	0.359	-44.8
14100	0.052	152.1	10.511	26.7	0.008	-128.8	0.328	-43.6
14200	0.052	163.7	10.387	14.9	0.005	171.8	0.316	-45.2
14300	0.069	177.3	10.078	-2.6	0.005	-123.7	0.299	-43.5
14400	0.090	178.7	9.953	-15.6	0.004	-90.4	0.281	-43.6
14500	0.119	-178.1	9.496	-30.3	0.006	-160.1	0.259	-42.8
14600	0.161	178.0	9.486	-45.6	0.001	-164.1	0.232	-42.5
14700	0.201	173.7	8.887	-59.6	0.001	-104.3	0.213	-37.6

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Package Outline



PIN ASSIGNMENT

- 1 : VDD
- 2 : RF in
- 3 : VGG
- 4 : Pmon
- 5 : RF out
- 6 : VDD

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■ Mounting Instructions for VF Package

1. Screw Mounting

- (1) The flange of package may be attached using screws. Torque conditions are shown in table 1.

Table 1. Recommended and Maximum Torque for Screw Mounting

Package	Recommended screw	Recommended Torque	Maximum Torque
VF	M2.0	10 N-cm (0.9 lb-in)	15 N-cm (1.3 lb-in)

- (2) First, tighten the screws with a torque driver set to 5 N-cm.
- (3) The surface finish of the heat sink should be better than 0.8 μm , and the surface flatness must be better than 10 μm .
- (4) Silicon based heat sink compounds should not be used for the thermal conductive grease. They cause poor grounding of the source flange, contamination and long term degradation of thermal resistance between the FET package and heat sink.

2. Solder Mounting

- (1) Recommended solder are Tin-Lead solder (63Sn/37Pb), Lead-Free solder (Sn-3.0Ag-0.5Cu)*¹ or equivalent.
- (2) For soldering, Tin-Lead solder (63Sn/37Pb) or Lead-Free solder (Sn-3.0Ag-0.5Cu)*¹ shall be used. (*1: The figure displays with weight %. A predominantly tin-rich alloy with 3.0% silver and 0.5% copper.)
- (3) Recommended Flux is Rosin type with chlorine content: 0.2% or less and a low halogen content. After soldering, the flux residue should be removed by appropriate cleaning methods.
- (4) The recommended soldering conditions are as follows:

Partial heating method (soldering iron, spot laser/air)

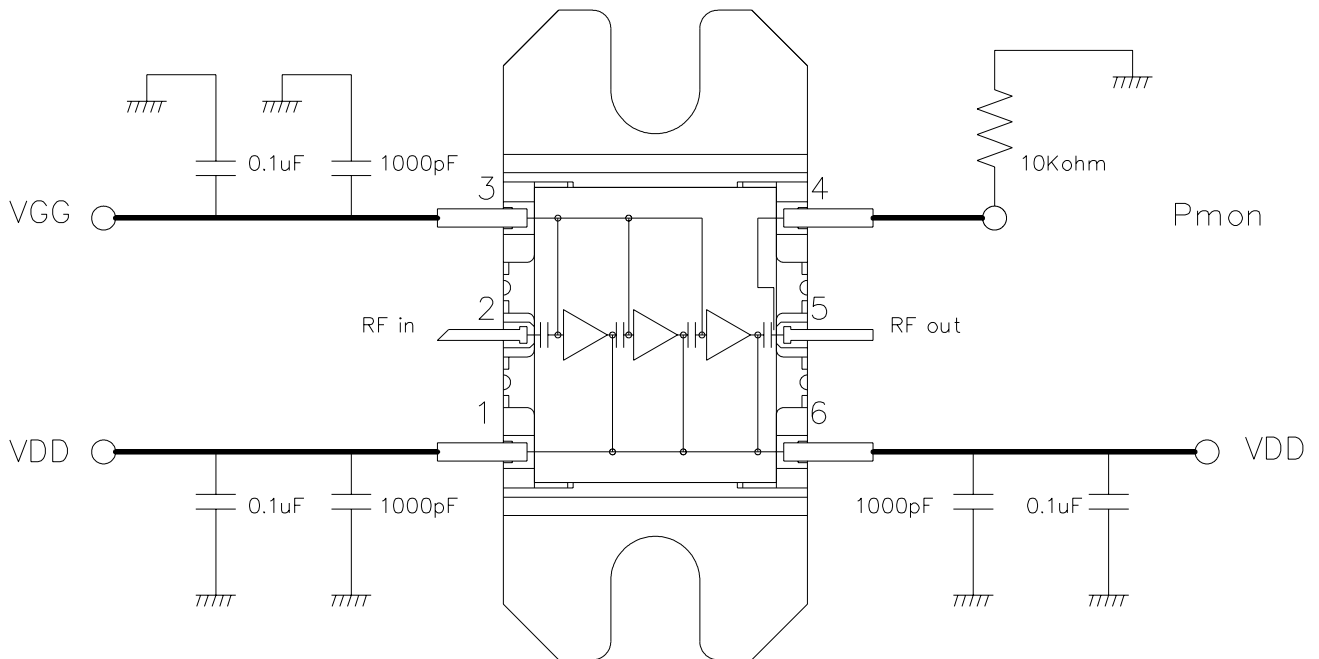
Product terminal temperature: 260 deg-C, max. 10 s./terminal or

400 deg-C, max. 3 s./terminal

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Recommended Bias Circuit and Internal Block Diagram



PIN ASSIGNMENT

- 1 : VDD
- 2 : RF in
- 3 : VGG
- 4 : Pmon
- 5 : RF out
- 6 : VDD

Note 1: The capacitors are recommended on the bias supply line, close to the package, in order to prevent video oscillations which could damage the module.

Note 2: Two pins of VDD are internally connected respectively.

Note 3: The external resistor (10Kohm) on the board is necessary to monitor the output power.

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