NEC

MOS INTEGRATED CIRCUIT
μPD75402A

4 BIT SINGLE-CHIP MICROCOMPUTER

The μPD75402A is a CMOS single-chip microcomputer which uses the 75X series architecture. It is used as a slave microcomputer suitable for control of key input, LED display, or remote controller signal transmission.

The μPD75P402 is also available for system development evaluation and small-volume production. It contains one-time PROM instead of mask ROM used in the μPD75402A.

The following user's manual describes the details of the functions of the μPD75402A. Be sure to read it before designing an application system.

μPD75402A User's Manual: IEU-644

FEATURES

- High-speed operation with a minimum instruction execution time of 0.95 μs (when the microcomputer operates at 4.19 MHz)
- Low voltage and low-speed instruction execution time of 15.3 μs (when the microcomputer operates at 4.19 MHz)
- Memory mapping by on-chip peripheral hardware
- NEC standard serial bus interface (SBI)
- 8-bit basic interval timer (watchdog timer applicable)
- Interrupt function
  - Three vectored interrupts (one external and two internal interrupts)
  - One external test input
- Clock output function (remote controller output applicable)
- Capable of specifying the incorporation of 16 pull-up resistors by software

APPLICATIONS

FAX, PPC, printer, VCR, remote control commander, and suchlike

ORDERING INFORMATION

Part number	Package	Quality grade
μPD75402AC-×××	28-pin plastic DIP (600 mil)	Standard
μPD75402ACT-×××	28-pin plastic shrink DIP (400 mil)	Standard
μPD75402AGB-×××-3B4	44-pin plastic QFP (10 × 10 mm)	Standard

Remark ××× indicates the ROM code number.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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Date Published November 1993 P
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Major changes in this revision are indicated by stars (★) in the margins.

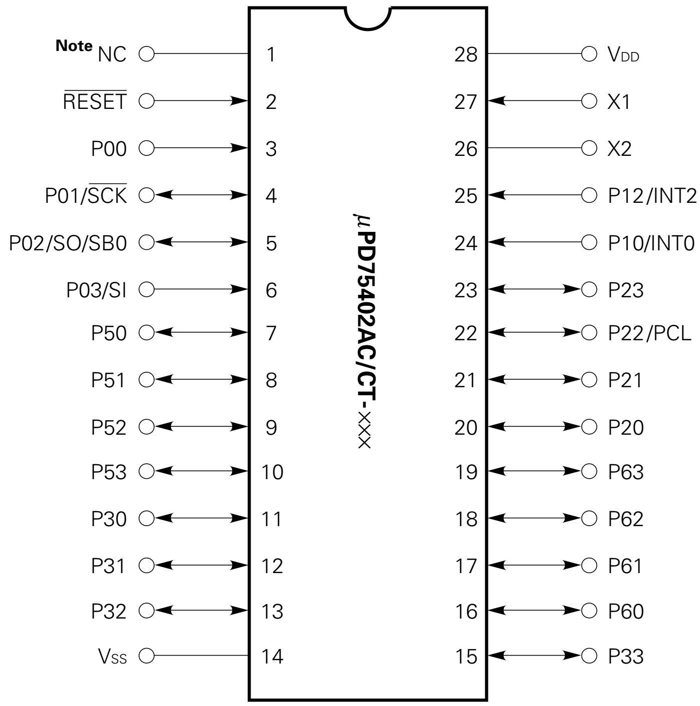
FUNCTIONAL OVERVIEW

Item		Function
Number of basic instructions		37
Minimum instruction execution time		• 0.95, 1.91, or 15.3 μs (when operating at 4.19 MHz) • Switchable among three speeds
Built-in memory	ROM	1920 × 8 bits
	RAM	64 × 4 bits
General register		4 bits × 4 or 8 bits × 2 (memory mapping)
I/O line		• CMOS input ports : 6 lines • CMOS I/O ports : 12 lines (8 lines can drive the LED directly.) • N-ch open-drain I/O ports : 4 lines (All lines can drive the LED directly.)
Pull-up resistor		• Capable of controlling the incorporation of 16 pull-up resistors by software • Capable of controlling the incorporation of 4 pull-up resistors by mask option
Clock output		• 1.05 MHz, 524 kHz, or 65.5 kHz (when operating at 4.19 MHz) • Applicable to remote controller output
Timer/counter		8-bit basic interval timer (watchdog timer applicable)
Serial interface		• 8 bits • Two transfer modes (three-wire synchronous mode and SBI mode)
Vectored interrupt		One external and two internal interrupts
Test input		One external input (See **Chapter 6** for details.)
Standby		STOP/HALT mode
Instruction set		• Bit manipulation instructions (set, clear, test, and Boolean operation) • 1-byte relative branch instructions • 4-bit operation instructions (add, Boolean operation, and compare) • 4- and 8-bit transfer instructions
Package		• 28-pin plastic DIP (600 mil) • 28-pin plastic shrink DIP (400 mil) • 44-pin plastic QFP (10 × 10 mm)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

28-pin plastic DIP (600 mil), 28-pin plastic shrink DIP (400 mil)

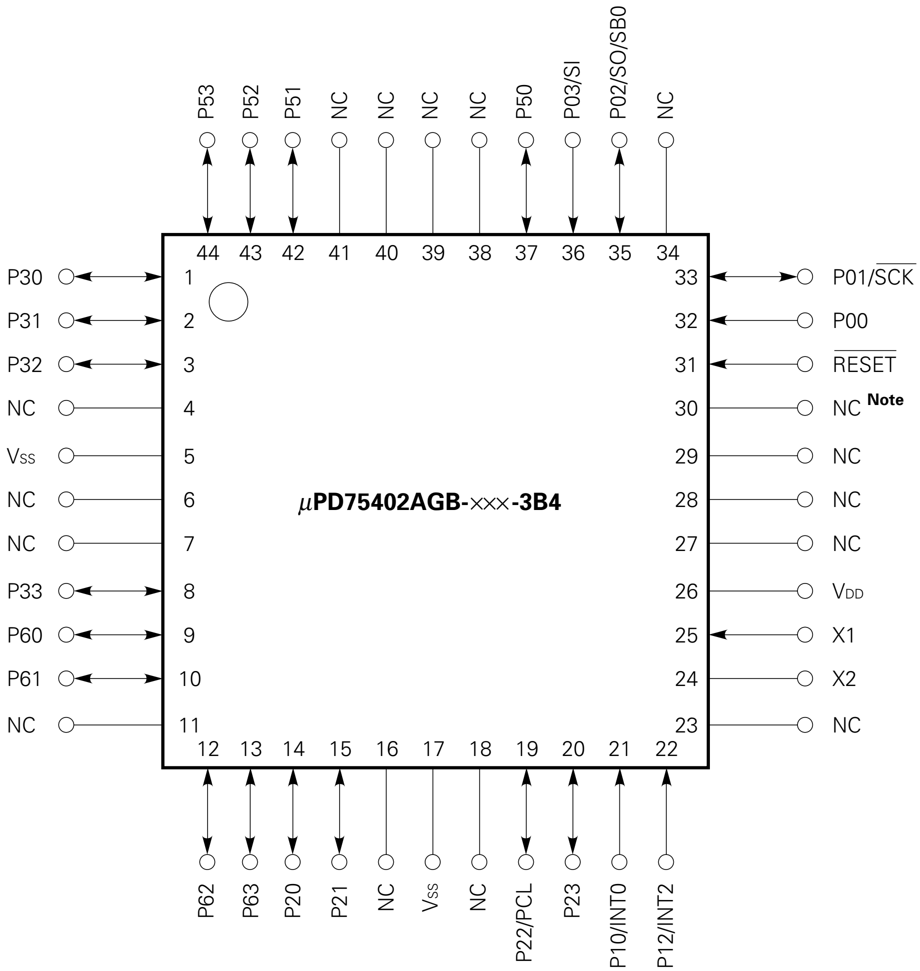


P00 - P03	:	Port 0
P10 and P12	:	Port 1
P20 - P23	:	Port 2
P30 - P33	:	Port 3
P50 - P53	:	Port 5
P60 - P63	:	Port 6

$\overline{SCK}$	:	Serial clock I/O
SO/SB0	:	Serial output/input-output
SI	:	Serial input
PCL	:	Clock output
INT0	:	External vectored interrupt input
INT2	:	External test input
X1 and X2	:	Oscillating pins
$\overline{RESET}$	:	Reset input
V_{DD}	:	Power supply
V_{SS}	:	Ground
NC	:	No connection

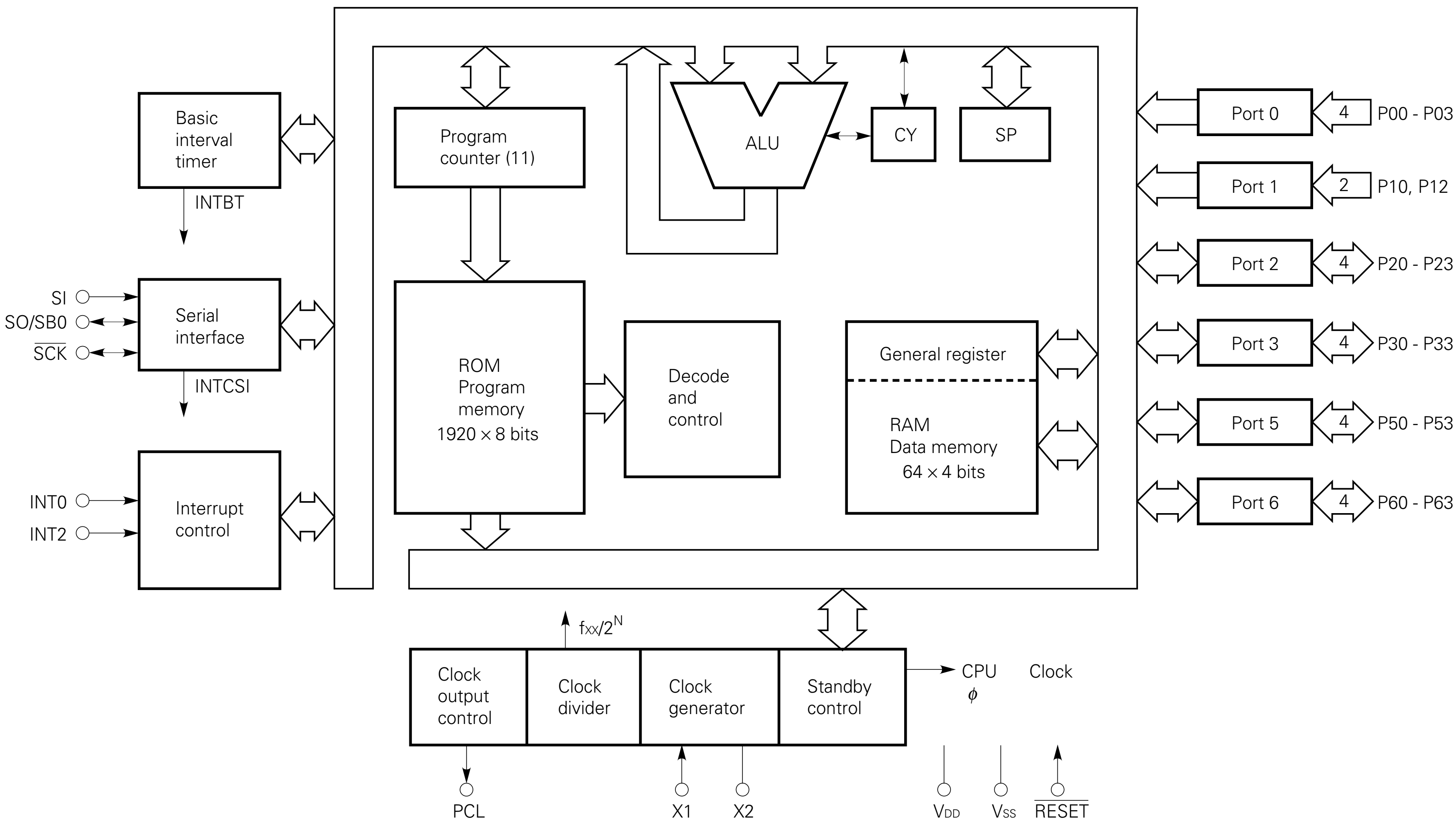
Note When the μPD75402A shares the printed circuit board with the μPD75P402, connect the NC pin directly to the V_{SS} pin.

44-pin plastic QFP (10 × 10 mm)



Note When the μPD75402A shares the printed circuit board with the μPD75P402, connect the NC pin (pin 30) directly to the V_{SS} pin.

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS

Pin	I/O	Dual-function pin	Function
P00	Input	–	4-bit input port (port 0) P01 to P03 allow the connection of built-in pull-up resistors to be specified in units of three bits by software.
P01	I/O	$\overline{SCK}$	
P02	I/O	SO/SB0	
P03	Input	SI	
P10	Input	INT0	2-bit input port (port 1) P10 connects with the built-in noise eliminator using a sampling clock. P12 connects with the built-in noise eliminator using an analog delay. P12 allows the connection of built-in pull-up resistor to be specified by software.
P12		INT2	
P20	I/O	–	4-bit I/O port (port 2) Allow I/O specification in units of four bits. Allow the connection of built-in pull-up resistors to be specified in units of four bits by software.
P21		–	
P22		PCL	
P23		–	
P30 - P33	I/O	–	Programmable 4-bit I/O port (port 3) Allow I/O specification bit by bit. Allow the connection of built-in pull-up resistors to be specified in units of four bits by software. Can directly drive LED.
P50 - P53	I/O	–	4-bit N-ch open-drain I/O port (port 5) Allow I/O specification in units of four bits. Allow the connection of built-in pull-up resistors to be specified bit by bit by mask option. Can directly drive LED.
P60 - P63	I/O	–	4-bit I/O port (port 6) Allow I/O specification in units of four bits. Allow the connection of built-in pull-up resistors to be specified in units of four bits by software. Can directly drive LED.

Remarks 1. The μPD75402A cannot perform 8-bit I/O with two ports as a pair.

2. See Chapter 8 for each pin status during resetting.

3.2 NON-PORT PINS

Pin	I/O	Dual-function pin	Function
INT0	Input	P10	Edge detection vectored interrupt request input pin (A detected edge can be selected by the mode register.) Connects with the built-in noise eliminator using a sampling clock.
INT2	Input	P12	Edge detection external test input pin (A rising edge is detected.)
SI	Input	P03	Serial data input pin
SO	I/O	P02/SB0	Serial data output pin
$\overline{SCK}$	I/O	P01	Serial clock I/O pin
SB0	I/O	P02/SO	Serial bus I/O pin
PCL	I/O	P22	Clock output pin
X1, X2	Input	–	Pin for connection to a crystal/ceramic resonator for system clock generation. An external clock is applied to X1, and its reverse phase to X2.
$\overline{RESET}$	Input	–	System reset input pin, which connects with the built-in noise eliminator using an analog delay.
V_{DD}	–	–	Positive power supply pin
V_{SS}	–	–	Ground potential pin
NC Note	–	–	No connection

Remark See Chapter 8 for each pin status during resetting.

Note Connect the NC pin directly to the V_{SS} pin when the μPD75402A shares the printed circuit board with the μPD75P402.

3.3 PIN INPUT/OUTPUT CIRCUITS

The I/O circuits of the μPD75402A are roughly shown on the next and subsequent pages.

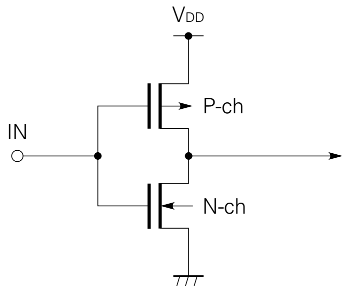
Table 3-1 I/O Circuit Type of Pin

Pin	I/O type	Pin	I/O type
P00	Ⓑ	P20, P21, and P23	E-B
P01/$\overline{SCK}$	Ⓕ-A	P22/PCL	
P02/SO/SB0	Ⓕ-B	P30 - P33	E-B
P03/SI	Ⓑ-C	P50 - P53	M
P10/INT0	Ⓑ	P60 - P63	E-B
P12/INT2	Ⓑ-C	$\overline{RESET}$	Ⓑ

Remark The types in circles have a Schmitt-triggered input.

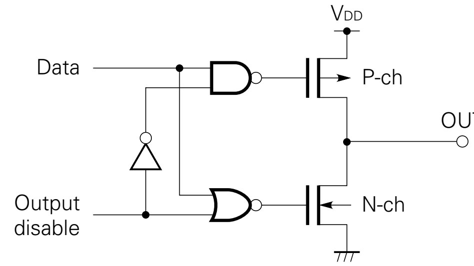
(1/2)

Type A (For type E-B)



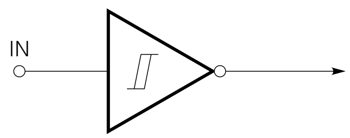
CMOS input buffer

Type D (For type E-B, F-A)



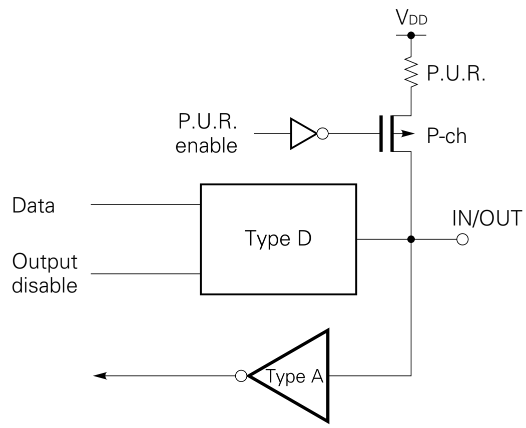
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type B



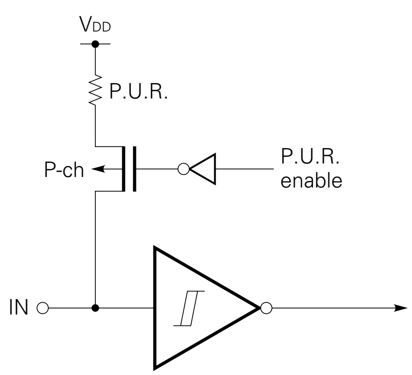
Schmitt trigger input with hysteresis

Type E-B



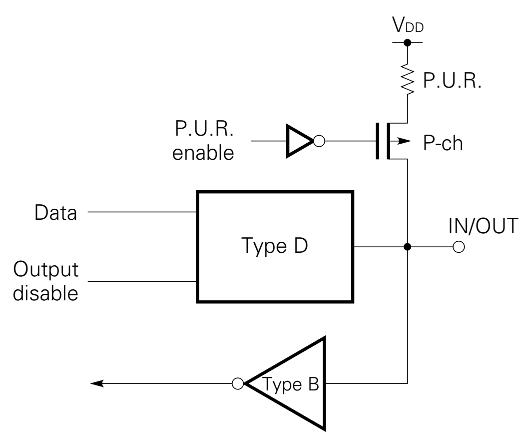
P.U.R.: Pull-Up Resistor

Type B-C



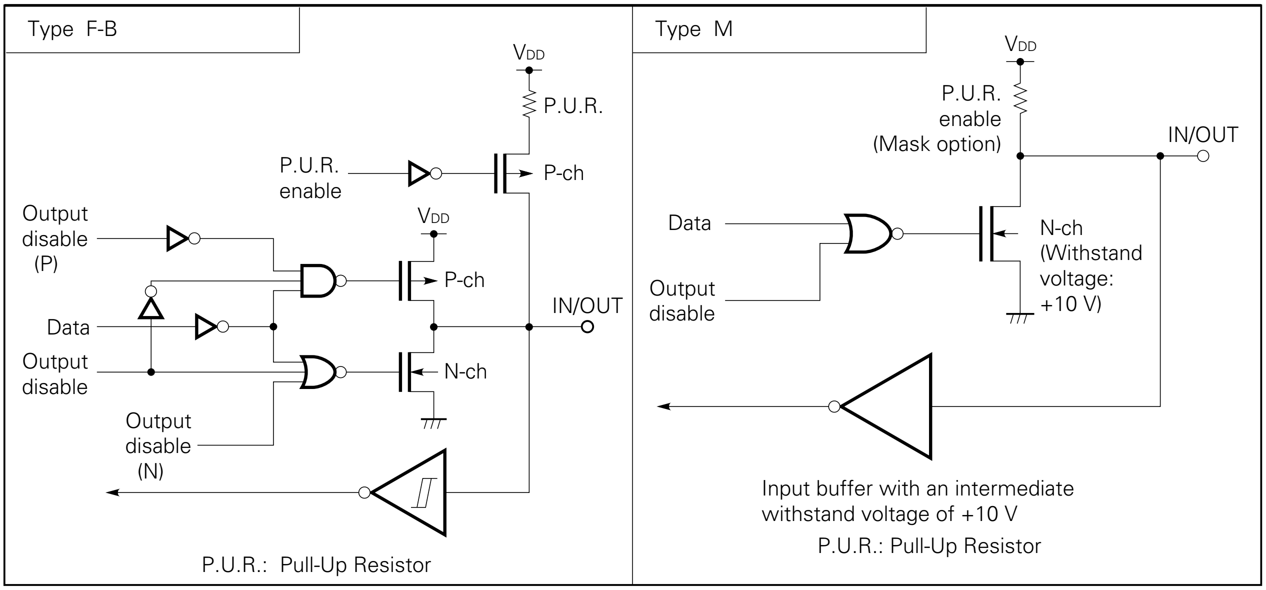
P.U.R.: Pull-Up Resistor

Type F-A



P.U.R.: Pull-Up Resistor

(2/2)



3.4 SELECTION OF A MASK OPTION

The following mask options are provided for pins:

P50 - P53	① Pull-up resistors connected (Either can be specified bit by bit.)	② No pull-up resistors connected

3.5 HANDLING UNUSED PINS

Pin	Recommended connection method
P00	Connected to the V_{SS} pin
P01 - P03 P10, P12	• When a pull-up resistor is contained Connected to the V_{DD} pin • When a pull-up resistor is not contained Connected to the V_{SS} or V_{DD} pin
P20 - P23 P30 - P33 P50 - P53 P60 - P63	• When a pull-up resistor is contained Input mode : Connected to the V_{DD} pin Output mode : Open • When a pull-up resistor is not contained Input mode : Connected to the V_{SS} or V_{DD} pin Output mode : Open
NC	Open or directly connected to the V_{SS} pin[Note]

Note When the μPD75402A shares the printed circuit board with the μPD75P402, connect the NC pin directly to the V_{SS} pin.

3.6 NOTES ON USING THE P00 AND $\overline{\text{RESET}}$ PINS

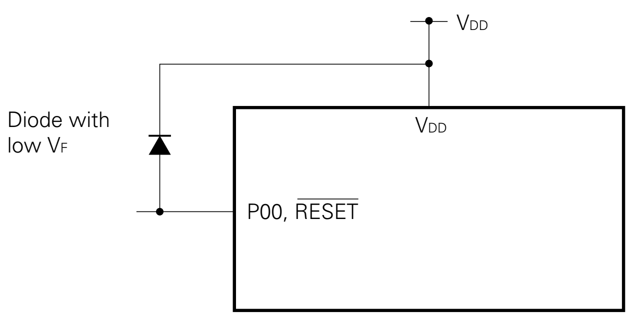
The P00 and $\overline{\text{RESET}}$ pins have the test mode selecting function for testing the internal operation of the μPD75402A (IC test), besides the functions shown in **Sections 3.1 and 3.2**.

Applying a voltage exceeding V_{DD} to the P00 and/or $\overline{\text{RESET}}$ pin causes the μPD75402A to enter the test mode. When noise exceeding V_{DD} comes in during normal operation, the device is switched to the test mode.

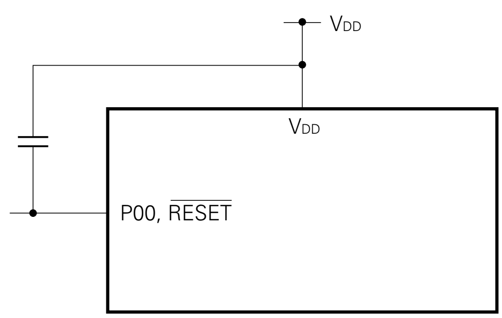
For example, when the wiring from the P00 or $\overline{\text{RESET}}$ pin is too long, noise voltage induced on the wiring is applied to the pin, driving the voltage at the pin above V_{DD}, which may cause malfunction.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- **Connect a diode with low V_F (0.3 V or lower) between the pin and V_{DD}.**



- **Connect a capacitor between the pin and V_{DD}.**



4. MEMORY CONFIGURATION

- Program memory (ROM): 1920 × 8 bits (000H to 77FH)
  - 000H and 001H: Vector table which contains the program start address after reset
  - 002H to 009H : Vector table which contains the program start addresses when interrupts occur
- Data memory
  - Data area : 64 × 4 bits (000H to 03FH)
  - Peripheral hardware area: 128 × 4 bits (F80H to FFFH)

Fig. 4-1 Program Memory Map

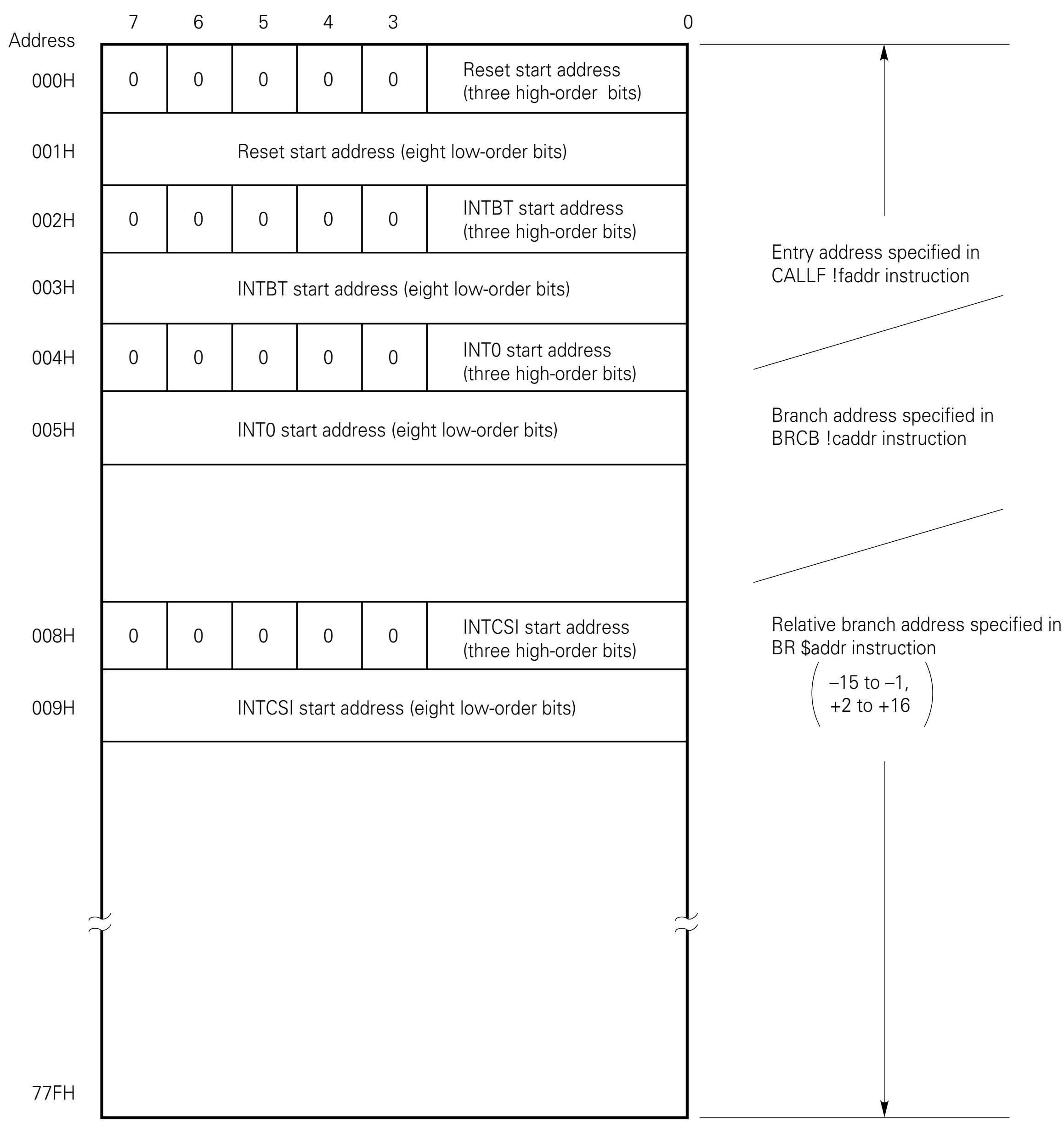
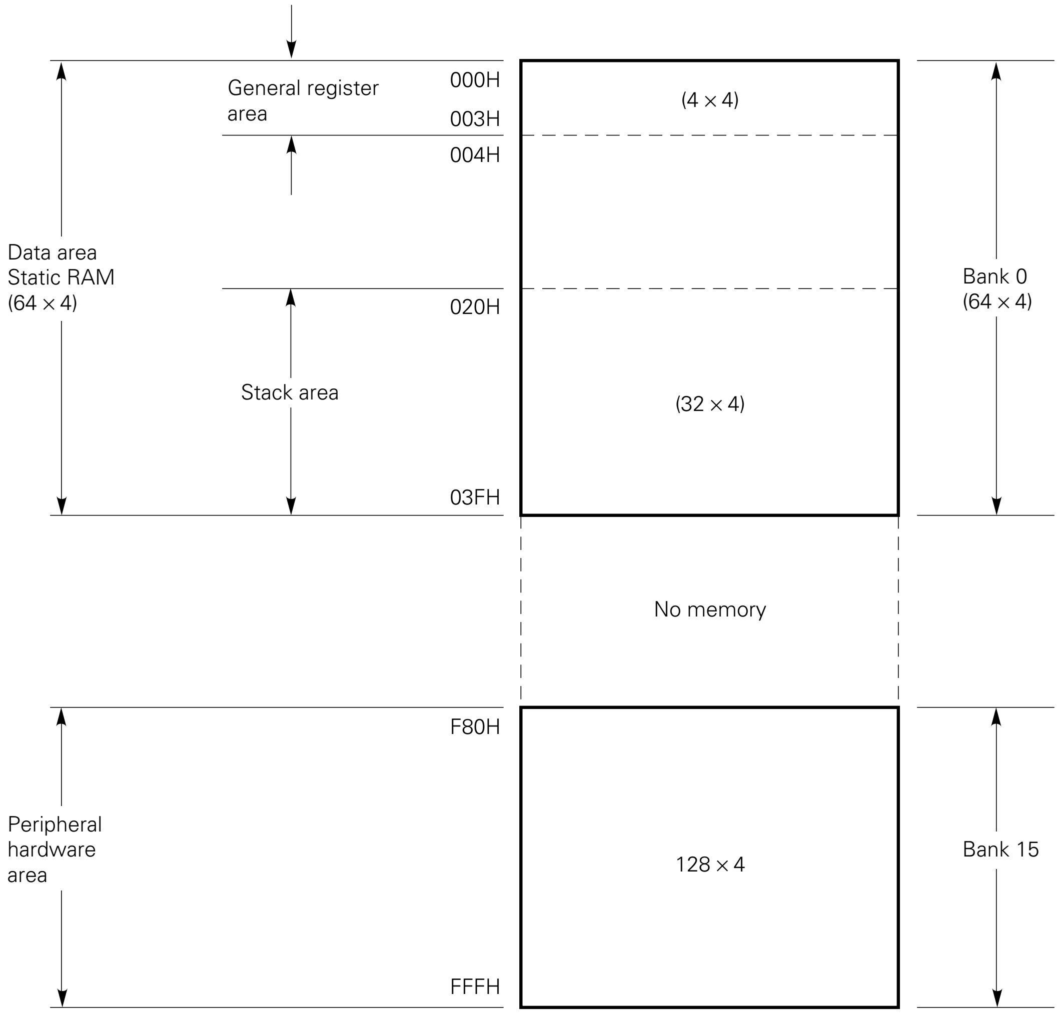


Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

The μPD75402A has the following three types of I/O port:

- 6 CMOS input pins (PORT0 and PORT1)
- 12 CMOS I/O pins (PORT2, PORT3, and PORT6)
- 4 N-ch open-drain I/O pins (PORT5)

Total: 22 pins

Table 5-1 Functions of Ports

Port name	Function	Operation and feature	Remarks
PORT0 PORT1	4-bit Input	Allows read and test at any time regardless of the operation modes of dual function pins.	Also used for SO/SB0, SI, $\overline{\text{SCK}}$, INT0, and INT2.
PORT3 **Note**	4-bit I/O	Allows input or output mode setting bit by bit.	————
PORT2 PORT6 **Note**		Allows input or output mode setting in units of 4 bits.	Port 2 is also used for PCL.
PORT5 **Note**	4-bit I/O (N-ch open-drain I/O with a withstand voltage of 10 V)	Allows input or output mode setting in units of 4 bits.	This port can incorporate a pull-up resistor as a mask option bit by bit.

Note PORT3, PORT5, and PORT6 can directly drive the LED.

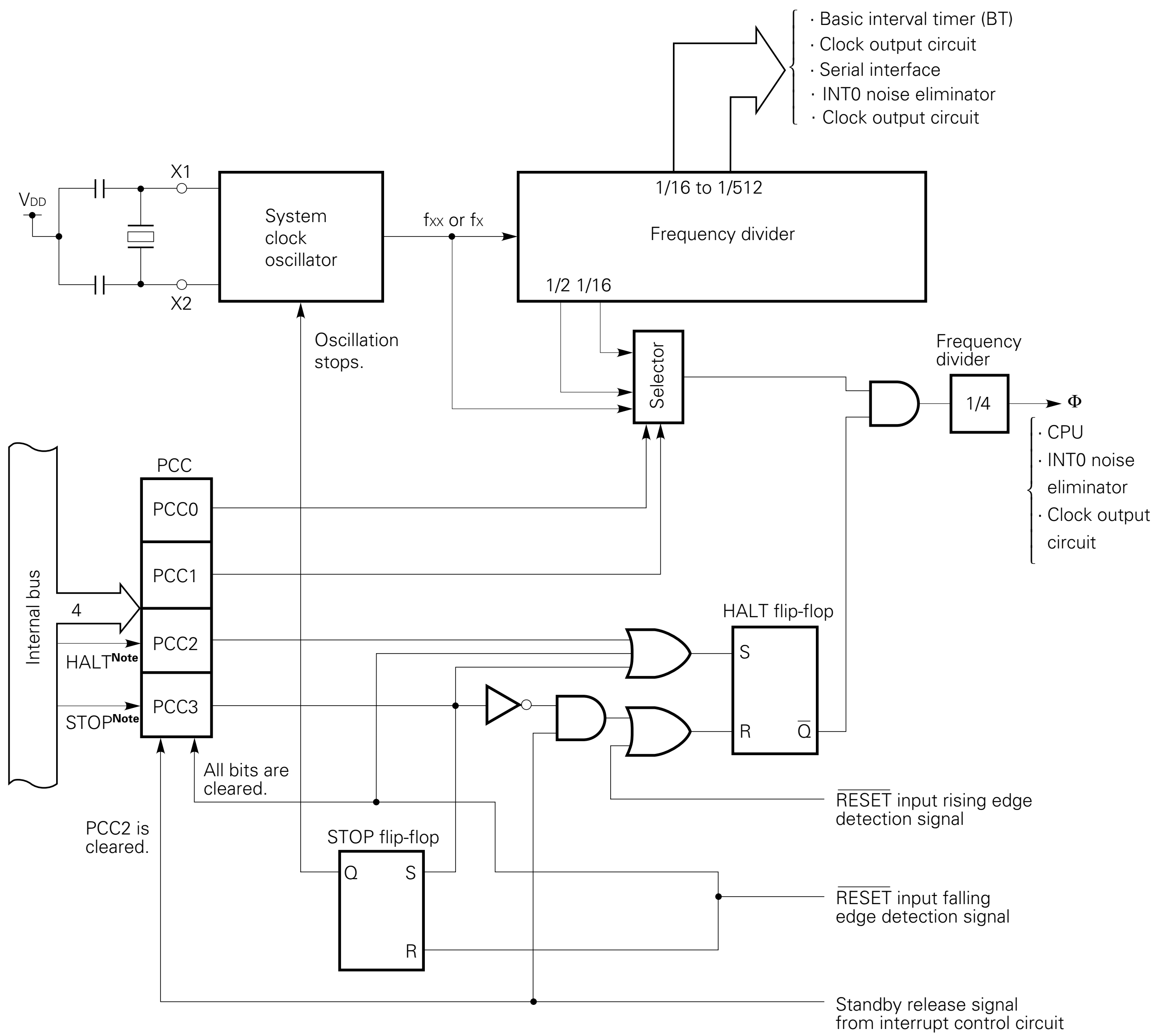
5.2 CLOCK GENERATOR

Operation of the clock generator is specified by the processor clock control register (PCC).

The instruction execution time is variable.

- 0.95 μs, 1.91 μs, 15.3 μs (when fxx is 4.19 MHz.)

★ **Fig. 5-1 Block Diagram of the Clock Generator**



Note Instruction execution

Remarks **1.** fxx : System clock frequency

2. fx : External clock frequency

3. PCC : Processor clock control register

4. 1 clock cycle (tCY) of Φ is 1 machine cycle of an instruction. For tCY, see "AC Characteristics" in **Chapter 10.**

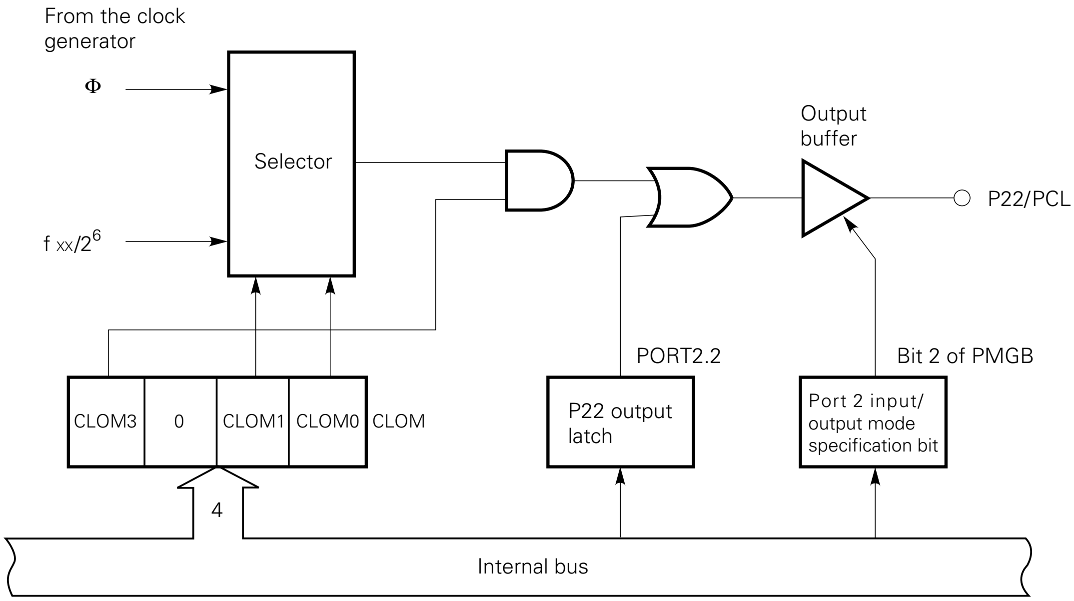
5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit, which outputs clock pulses from pin P22/PCL, is used for supplying clock pulses for peripheral LSIs or for remote control output.

- Clock output (PCL): 1.05 MHz, 524 kHz, 65.5 kHz (when f_{XX} is 4.19 MHz)

Fig. 5-2 shows the configuration of the clock output circuit.

Fig. 5-2 Configuration of the Clock Output Circuit



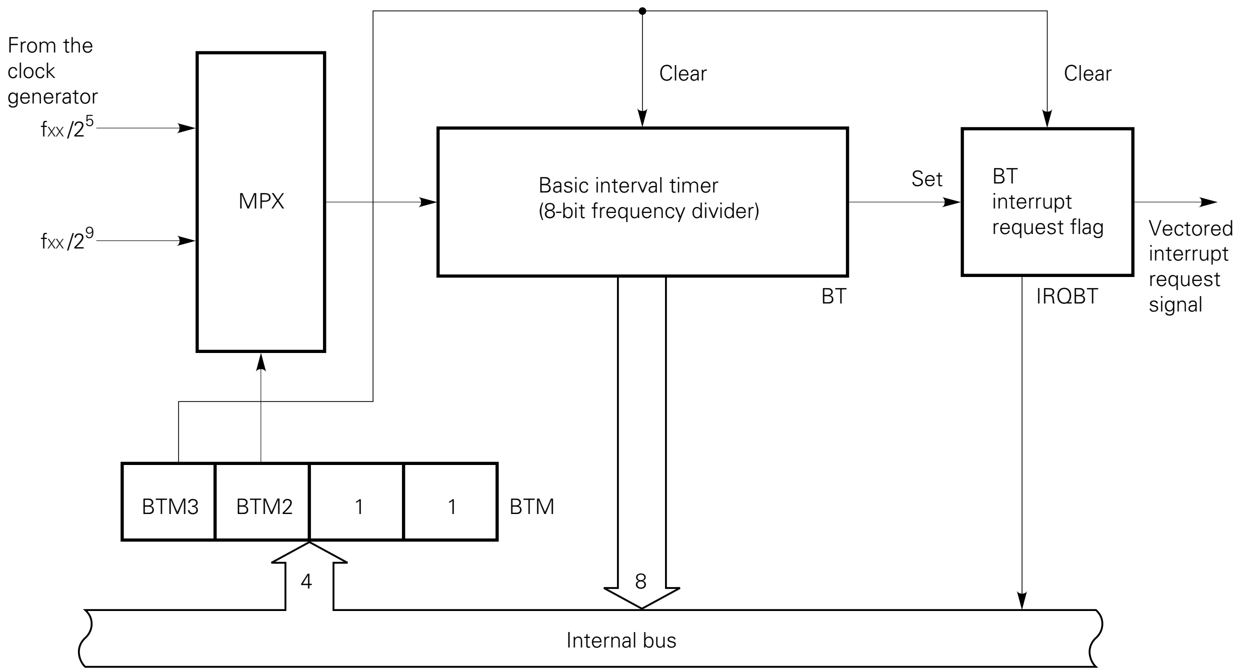
Remark The clock output circuit is designed not to output high-frequency pulses when clock output is switched between the enable and disable states.

5.4 BASIC INTERVAL TIMER

The basic interval timer provides the following functions:

- Interval timer operation that generates a reference time interrupt
- Can be used as a watchdog timer for detecting program crashes
- Reading the count value

Fig. 5-3 Configuration of the Basic Interval Timer



5.5 SERIAL INTERFACE

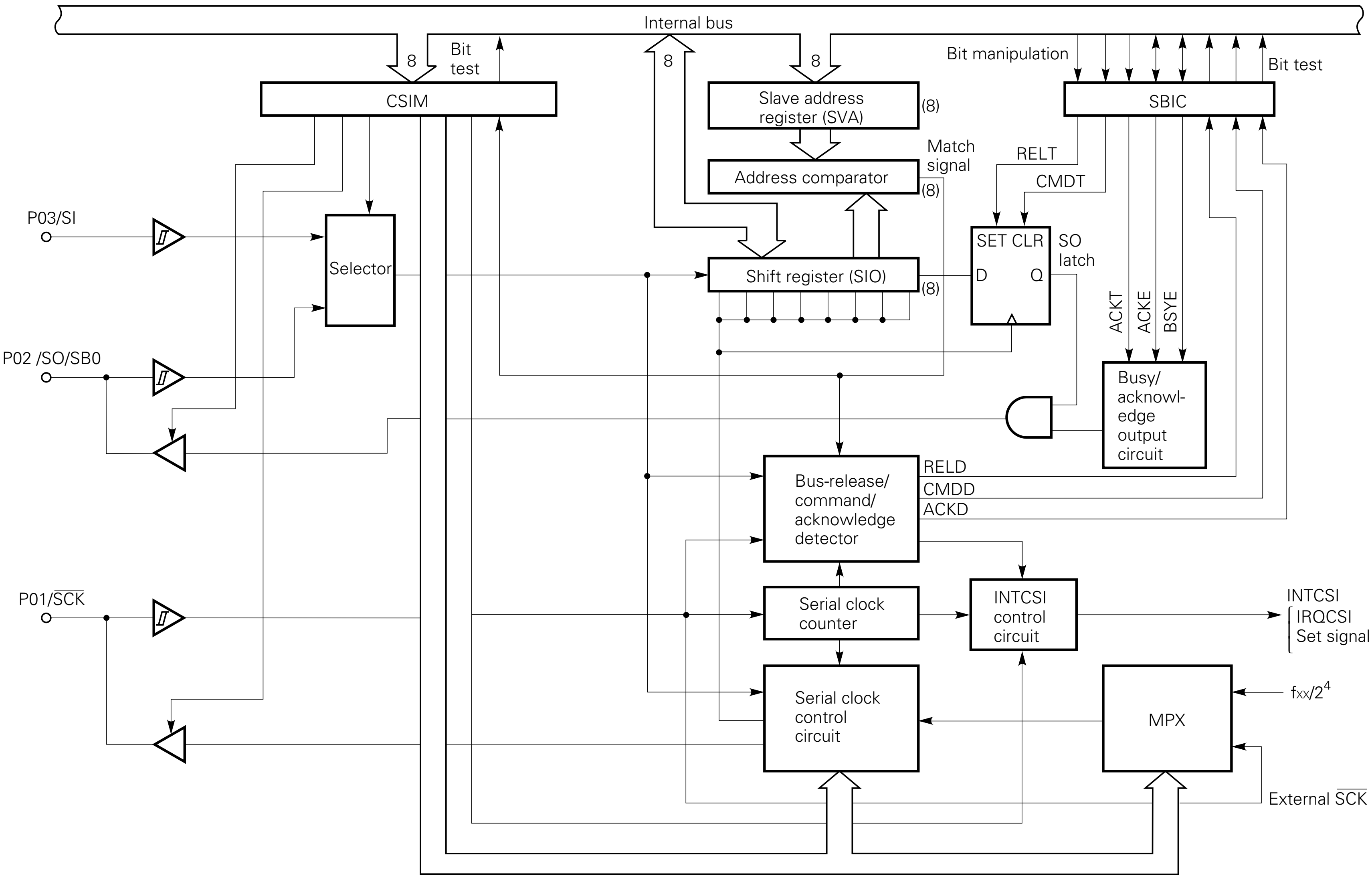
The serial interface has the following modes:

- Three-wire serial I/O mode (MSB is transferred first.)
- SBI mode (MSB is transferred first.)

The three-wire serial I/O mode enables connections to be made with the 75X series, 78K series, and many other types of peripheral I/O devices.

The SBI mode enables communication with two or more devices.

Fig. 5-4 Block Diagram of the Serial Interface



6. INTERRUPT FUNCTION

The μPD75402A has three interrupt sources and each of them has the interrupt vector table.

The μPD75402A is also provided with one edge-sensitive testable input signal.

When a vectored interrupt request is issued, the PC and PSW are saved in the stack, and the contents of the vector table which corresponds to the issued vectored interrupt are set in the PC as a start address. The program branches to the interrupt service routine. These operations are performed automatically by the hardware.

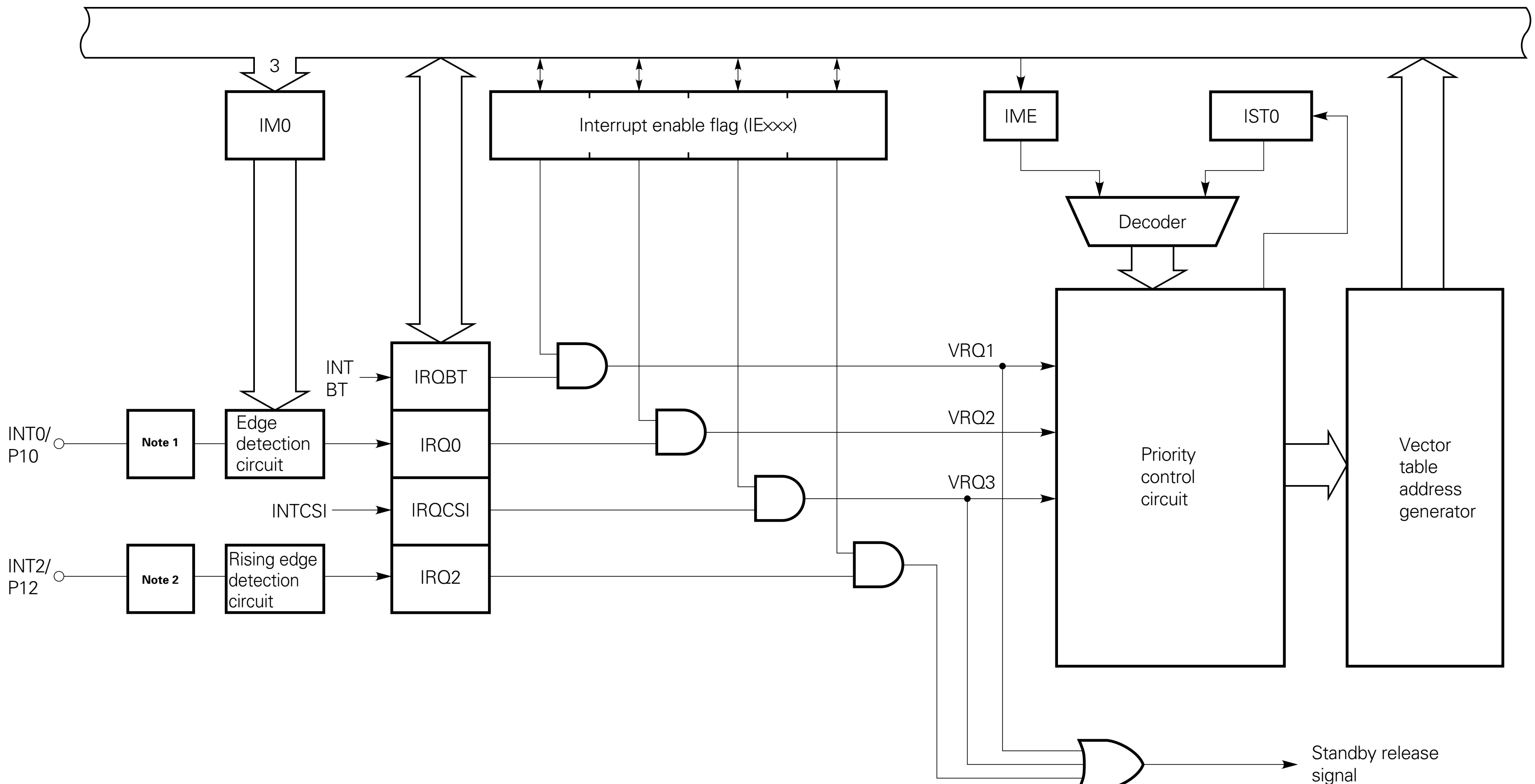
The flag is set by detecting the edge of the testable input signal, but a vectored interrupt request is not issued.

During execution of the interrupt service routine, the μPD75402A does not accept the other interrupt requests. Unlike the other 75××× series, the μPD75402A cannot handle multiple interrupts.

The interrupt control circuit of the μPD75402A has the following functions:

- Vectored interrupt function under hardware control which can determine whether to accept an interrupt by an interrupt enable flag (IE×××) and an interrupt master enable flag (IME).
- Any interrupt start address can be set.
- Test function of an interrupt request flag (IRQ×××) (Software can confirm that an interrupt occurs.)
- Release of the standby (HALT) mode (An interrupt to be released by an interrupt enable flag can be selected from interrupts other than INT0.)

Fig. 6-1 Block Diagram of Interrupt Control Circuit



Notes 1. Noise eliminator using the sampling clock

2. Noise eliminator using analog delay

7. STANDBY FUNCTION

To reduce the power consumption when the program is in the wait state, the μPD75402A has two standby modes, STOP and HALT.

Table 7-1 Operation Statuses in the Standby Mode

		STOP mode	HALT mode
Instruction to be used to set mode		STOP instruction	HALT instruction
Operation status	Clock generator	Oscillation stops.	Only the CPU clock (Φ) stops, but oscillation continues.
	Basic interval timer	Operation stops.	Operates. (IRQBT is set at every reference time interval.)
	Serial interface	Operable only when the external $\overline{SCK}$ input is selected for the serial clock.	Operable
	Clock output circuit	Operation stops.	Clocks other than CPU clock (Φ) can be output.
	External interrupt	INT2 pin is usable. INT0 pin cannot be used.	INT2 pin is usable. INT0 pin cannot be used.
	CPU	Operation stops.	
Release signal		$\overline{RESET}$ input	$\overline{RESET}$ input or interrupt request signals enabled by the interrupt enable flags

8. RESET FUNCTION

When a low level signal is input to the $\overline{RESET}$ input pin, the state changes to the system reset. Table 8-1 shows the statuses of the hardware.

When the $\overline{RESET}$ signal rises from the low level to the high level, the reset state is released. The three low-order bits of the reset vector table whose address is 000H is set in bits 10 to 8 of the program counter (PC) and the contents of the reset vector table whose address is 001H is set in bits 7 to 0 of the PC. The program branches to that address and starts execution, i.e., the reset start address is programmable.

Initialize contents of registers in a program if necessary.

The $\overline{RESET}$ pin connects to the Schmitt-trigger circuit whose threshold level has hysteresis in the chip. This pin is also connected to the noise eliminator using an analog delay to eliminate narrow noise and prevent errors caused by noise. (See **Fig. 8-1**.)

For the power-on reset operation, be sure to allow sufficient time for oscillation to settle between power on and acceptance of the reset signal (see Fig. 8-2).

Fig. 8-1 Acceptance of the Reset Signal

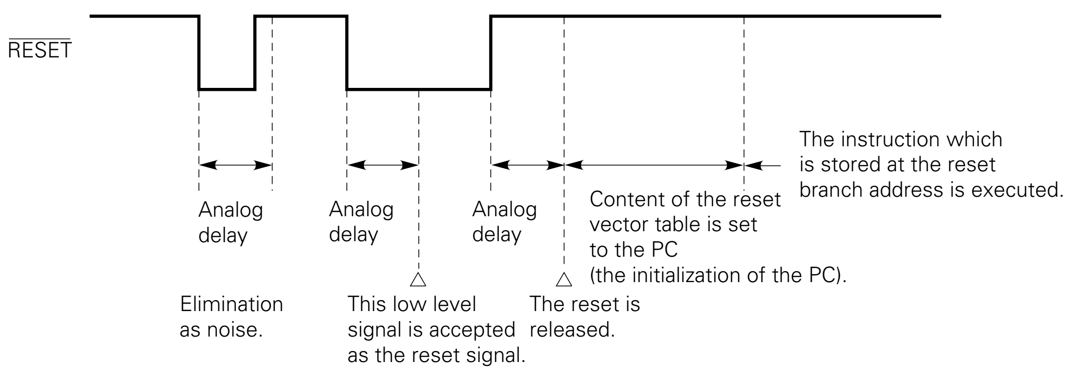


Fig. 8-2 Power-On Reset Operation

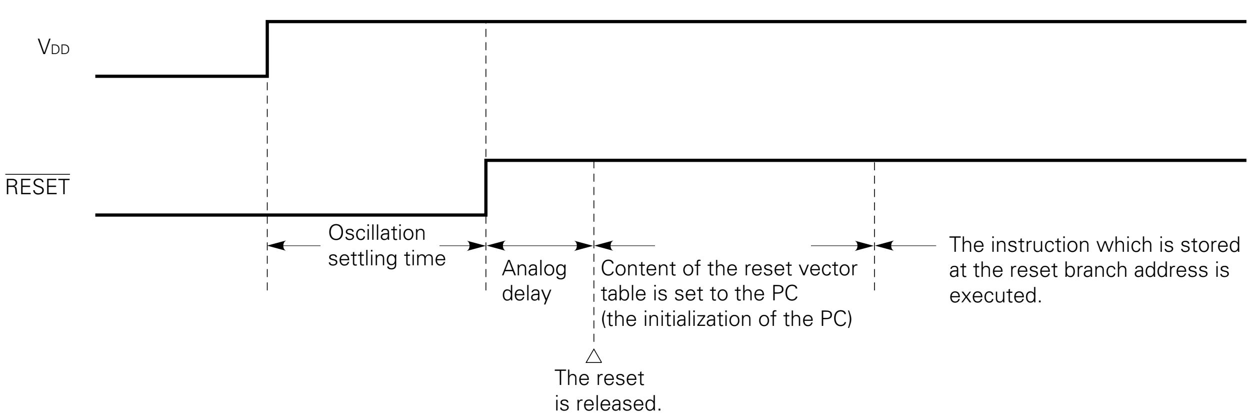


Table 8-1 Hardware Statuses after Reset Operations

Hardware		RESET input in standby mode	RESET input during operations
Program counter (PC)		Set the three low-order bits of address 000H in program memory in PC bits 10 to 8 and set the contents of address 001H in PC bits 7 to 0.	Set the three low-order bits of address 000H in program memory in PC bits 10 to 8 and set the contents of address 001H in PC bits 7 to 0.
PSW	Carry flag (CY)	Retained	Undefined
	Skip flag (SK0 - SK2)	0	0
	Interrupt status flag (IST0)	0	0
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Retained Note	Undefined
General register (X, A, H, L)		Retained	Undefined
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Serial interface	Shift register (SIO)	Retained	Undefined
	Operation mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Retained	Undefined
Clock generator and clock output circuit	Processor clock control register (PCC)	0	0
	Clock output mode register (CLOM)	0	0
Interrupt	Interrupt request flag (IRQ×××)	Reset (0)	Reset (0)
	Interrupt enable flag (IE×××)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0 mode register (IM0)	0	0
Digital I/O port	Output buffer	Off	Off
	Output latch	Cleared (0)	Cleared (0)
	I/O mode register (PMGA, PMGB)	0	0
	Pull-up resistor specification register (POGA)	0	0
States of pins	P00 - P03, P10, P12, P20 - P23, P30 - P33, P60 - P63	Used as inputs	Used as inputs
	P50 - P53	• High level when pull-up resistor is built in • High impedance when open drain is used in the internal circuit	• High level when pull-up resistor is built in • High impedance when open drain is used in the internal circuit

Note Data in the data memory whose addresses are 38H to 3DH is not defined when the standby mode is released by the RESET input signal.

9. INSTRUCTION SET

(1) Representation format and description method of operands

An operand is described in the operand field of each instruction according to the description method corresponding to the operand representation format of the instruction (refer to "RA75X Assembler Package User's Manual, Language" (EEU-1363) for details). When two or more elements are described in the description method field, select one of them. Upper-case letters, a number sign (#), and at mark (@), an exclamation mark (!), and a dollar sign ($) are keywords, so they can be used without alteration.

Specify an appropriate numeric value or label for immediate data.

The symbols of registers and flags can be used as labels instead of mem, fmem, and bit (refer to the "μPD75402A User's Manual" (IEU-644) for details). Some labels, however, cannot be specified in fmem.

Representation format	Description method
reg reg1	X, A, H, L X, H, L
rp	XA, HL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem bit	8-bit immediate data or label Note 2-bit immediate data or label
fmem	FB0H - FBFH/FF0H - FFFH immediate data or label
addr caddr faddr	11-bit immediate data or label 11-bit immediate data or label 11-bit immediate data or label
PORTn IE×××	PORT0 - PORT3, PORT5, PORT6 IEBT, IECSI, IE0, IE2

Note Only an even address can be written in mem when 8-bit data is processed.

(2) Legend

A : A register, 4-bit accumulator
H : H register, 4-bit accumulator
L : L register, 4-bit accumulator
X : X register, 4-bit accumulator
XA : Register pair (XA), 8-bit accumulator
HL : Register pair (HL)
PC : Program counter
SP : Stack pointer
CY : Carry flag, bit accumulator
PSW : Program status word
PORTn: Port n (n = 0 to 3, 5, 6)
IME : Interrupt master enable flag
IE××× : Interrupt enable flag
PCC : Processor clock control register
. : Address/bit delimiter
(××) : Contents addressed by ××
××H : Hexadecimal data

(3) Explanation of the symbols in the addressing area field

*1	MB = 0	Data memory addressing
*2	MB = 0 (00H - 3FH) MB = 15 (80H - FFH)	
*3	MB = 15, fmem = FB0H - FBFH or FF0H - FFFH	
*4	addr = 000H - 77FH	Program memory addressing
*5	addr = (Current PC) – 15 to (Current PC) – 1 or (Current PC) + 16 to (Current PC) + 2	
*6	caddr = 000H - 77FH	
*7	faddr = 000H - 77FH	

Remarks 1. MB indicates an accessible memory bank.

2. *4 to *7 indicate each addressable area.

(4) Explanation of the machine cycle field

S indicates the number of machine cycles required for a skip instruction to perform skipping. The following shows the values of S.

- When the next instruction is not skipped, S is 0.
- When the next instruction is skipped, S is 1.

A machine cycle is equal to one cycle (= t_{CY}) of CPU clock Φ. A PCC setting determines the machine cycle. It can be set to one of three different periods.

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer instruction	MOV	A, #n4	1	1	A ← n4		String A
		XA, #n8	2	2	XA ← n8		String A
		HL, #n8	2	2	HL ← n8		String B
		A, @HL	1	1	A ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		A, mem	2	2	A ← (mem)	*2	
		XA, mem	2	2	XA ← (mem)	*2	
		mem, A	2	2	(mem) ← A	*2	
		mem, XA	2	2	(mem) ← XA	*2	
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*2	
		XA, mem	2	2	XA ↔ (mem)	*2	
		A, reg1	1	1	A ↔ reg1		
	MOVT	XA, @PCXA	1	3	XA ← $(PC_{10-8} + XA)_{ROM}$		
Arithmetic/ logical instruction	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
	AND	A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, @HL	1	1	A ← A ⊻ (HL)	*1	
Accumulator manipulation instruction	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		
Increment/ decrement instruction	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*2	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
Comparison instruction	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
Carry flag manipulation instruction	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycle	Operation	Addressing area	Skip condition
Memory bit manipulation instruction	SET1	mem.bit	2	2	(mem.bit) ← 1	*2	
		fmem.bit	2	2	(fmem.bit) ← 1	*3	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*2	
		fmem.bit	2	2	(fmem.bit) ← 0	*3	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*2	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*3	(fmem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*2	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*3	(fmem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*3	(fmem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*3	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*3	
	XOR1	CY, fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*3	
Branch instruction	BR	addr	–	–	PC_{10-0} ← addr (The assembler selects an appropriate instruction from the BRCB !caddr and BR $addr instructions.)	*4	
		$addr	1	2	PC_{10-0} ← addr	*5	
	BRCB	!caddr	2	2	PC_{10-0} ← caddr	*6	
Subroutine stack control instruction	CALLF	!faddr	2	2	(SP – 4)(SP – 1)(SP – 2) ← 0, PC_{10-0} (SP – 3) ← 0000 PC_{10-0} ← faddr, SP ← SP – 4	*7	
	RET		1	3	PC_{10-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4		
	RETS		1	3 + S	PC_{10-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4, then skip unconditionally		Unconditionally
	RETI		1	3	PC_{10-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1)(SP – 2) ← rp, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
Interrupt control instruction	EI		2	2	IME (IPS.3) ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IE×××	2	2	IE××× ← 0		
Input/output instruction	IN	A, PORTn	2	2	A ← PORTn (n = 0 - 3, 5, 6)		
	OUT	PORTn, A	2	2	PORT n ← A (n = 2, 3, 5, 6)		
CPU control instruction	HALT		2	2	Set HALT mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP mode (PCC.3 ← 1)		
	NOP		1	1	No operation		

10. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions			Rated value	Unit
Supply voltage	V_{DD}				–0.3 to +7.0	V
Input voltage	V_{I1}	Ports other than port 5			–0.3 to V_{DD} + 0.3	V
	V_{I2}	Port 5	Built-in pull-up resistor		–0.3 to V_{DD} + 0.3	V
			Open drain		–0.3 to +11.0	V
Output voltage	V_O				–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Each pin			–15	mA
		Total of all output pins			–30	mA
Low-level output current	I_{OL} **Note**	One pin of port 0, 3, 5, or 6		Peak value	30	mA
				rms	15	mA
		One pin of port 2		Peak value	20	mA
				rms	10	mA
		Total of all pins of ports 0, 3, and 5 (excl. P33)		Peak value	100	mA
				rms	60	mA
		Total of all pins of ports 2, 6, and P33		Peak value	100	mA
				rms	60	mA
Operating temperature	T_{opt}				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

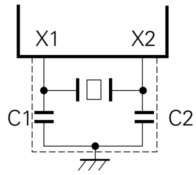
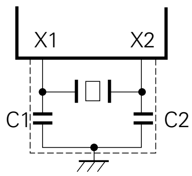
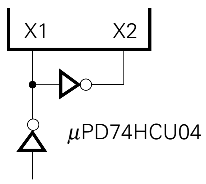
Note Calculate rms with [rms] = [peak value] $\times\sqrt{\text{duty}}$.

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	f = 1 MHz 0 V for pins other than pins to be measured			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

CHARACTERISTICS OF THE OSCILLATION CIRCUIT (T_a = –40 °C to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constant	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator		Oscillator frequency (f_{XX}) Note 1	V_{DD} = oscillation voltage range	2.0		5.0 Note 3	MHz
		Oscillation settling time Note 2	After V_{DD} reaches MIN. of the oscillation voltage range			4	ms
Crystal		Oscillator frequency (f_{XX}) Note 1		2.0	4.19	5.0 Note 3	MHz
		Oscillation settling time Note 2	V_{DD} = 4.5 to 6.0 V			10	ms
External clock		X1 input frequency (f_X) Note 1		2.0		5.0 Note 3	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		250	ns

Notes 1. The oscillator frequency and X1 input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} is applied or after the STOP mode is released.

★ **3.** When 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time. When PCC = 0011, one machine cycle falls short of 0.95 μs, the minimum value for the standard.

★ **Caution When the clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.**

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{SS}. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

RECOMMENDED CERAMIC RESONATORS

Manufacturer	Part number Note	Frequency [MHz]	Capacitance of externally-connected capacitors [pF]		Oscillation voltage range [V]	
			C1	C2	Min.	Max.
Murata Mfg. Co., Ltd.	CSA×××MG093	2.00 to 2.44	30	30	2.7	6.0
	CSA×××MGU	2.45 to 4.91	30	30	2.7	6.0
Kyocera Corp.	KBR-2.0MS	2.0	47	47	3.0	6.0
	KBR-4.19MS	4.19	33	33	3.0	6.0
	KBR-5.0MS	5.0	33	33	3.3	6.0

Note ××× indicates frequency.

DC CHARACTERISTICS (T_a = –40 °C to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	Ports 2, 3, and 6		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	Ports 0 and 1, and $\overline{RESET}$		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	Port 5	Built-in pull-up resistor	$0.7V_{DD}$		V_{DD}	V
			Open drain	$0.7V_{DD}$		10	V
	V_{IH4}	X1 and X2		V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2, 3, 5, and 6		0		$0.3V_{DD}$	V
	V_{IL2}	Ports 0 and 1, and $\overline{RESET}$		0		$0.2V_{DD}$	V
	V_{IL3}	X1 and X2		0		0.4	V
High-level output voltage	V_{OH}	Ports 0, 2, 3, and 6	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			I_{OH} = –100 μA	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}	Ports 3, 5, and 6	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.6	2.0	V
		Ports 0, 2, 3, 5, and 6	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0 (Open drain)	Pull-up resistor : 1 kΩ or more V_{DD} = 4.5 to 6.0 V			$0.2V_{DD}$	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Other than X1 and X2			3	μA
	I_{LIH2}		X1 and X2			20	μA
	I_{LIH3}	V_{IN} = 10 V	Port 5 (open drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Other than X1 and X2			– 3	μA
	I_{LIL2}		X1 and X2			– 20	μA
High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}	Other than port 5			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Port 5 (open drain)			20	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				– 3	μA
Built-in pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, and 6 (excl. P00 and P10) V_{IN} = 0 V	V_{DD} = 5.0 V ± 10 %	15	40	80	kΩ
			V_{DD} = 3.0 V ± 10 %	30		300	kΩ
	R_{L2}	Port 5 V_{OUT} = V_{DD} – 2.0 V	V_{DD} = 5.0 V ± 10 %	15	40	70	kΩ
			V_{DD} = 3.0 V ± 10 %	10		60	kΩ
Power supply current Note 1	I_{DD1}	4.19 MHz crystal resonance C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10 % Note 2		2.5	8	mA
			V_{DD} = 3.0 V ±10 % Note 3		0.5	1.5	mA
	I_{DD2}		HALT mode, V_{DD} = 5.0 V ±10 %		500	1500	μA
			HALT mode, V_{DD} = 3.0 V ±10 %		150	450	μA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ±10%		0.5	20	μA
			V_{DD} = 3.0 V ±10 %		0.1	10	μA
			V_{DD} = 3.0 V ±10 %, T_a = 25 °C		0.1	5	μA

Notes 1. This current excludes the current which flows through the built-in pull-up resistors.

2. Value when the processor clock control resistor (PCC) is set to 0011 and the μPD75402A is operated in the high-speed mode

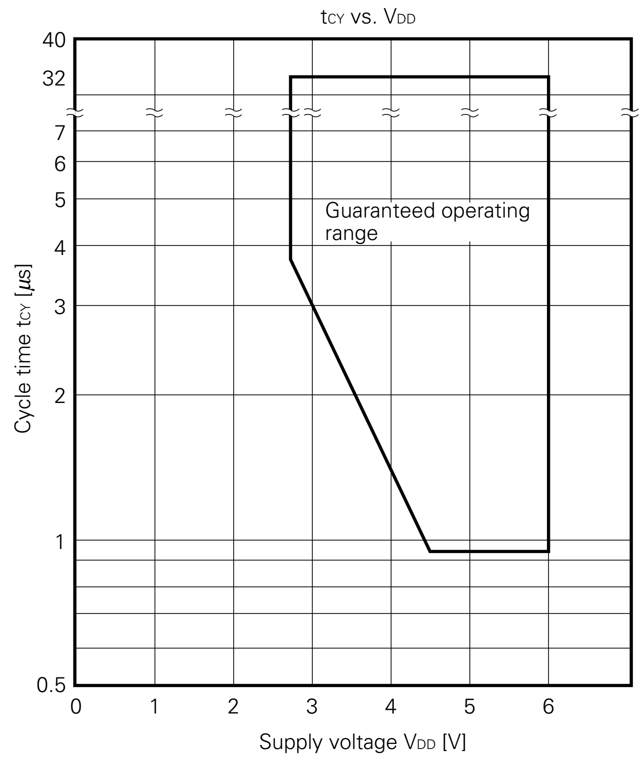
3. Value when the PCC is set to 0000 and the μPD75402A is operated in the low-speed mode

AC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU clock cycle time (minimum instruction execution time = 1 machine cycle) **Note 1**	t_{CY}	V_{DD} = 4.5 to 6.0 V	0.95		32	μs
			3.8		32	μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INT0	**Note 2**			μs
		INT2	10			μs
RESET low-level width	t_{RSL}		10			μs

Notes 1. CPU clock (Φ) cycle time (minimum instruction execution time) depends on the connected resonator frequency and the setting of the processor clock control register (PCC).
The figure on the right side shows the cycle time t_{CY} characteristics for the supply voltage V_{DD}.

2. This value is 2t_{CY} or 128/f_{XX} according to the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

THREE-WIRE SERIAL I/O MODE ($\overline{SCK}$ ··· INTERNAL CLOCK OUTPUT):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2 - 50$			ns
	t_{KH1}			$t_{KCY1}/2 - 150$			ns
SI setup time (referred to $\overline{SCK}$↑)	t_{SIK1}			150			ns
SI hold time (referred to $\overline{SCK}$↑)	t_{KSI1}			400			ns
Delay from $\overline{SCK}$↓ to SO output	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

THREE-WIRE SERIAL I/O MODE ($\overline{SCK}$ ··· EXTERNAL CLOCK INPUT):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI setup time (referred to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (referred to $\overline{SCK}$↑)	t_{KSI2}			400			ns
Delay from $\overline{SCK}$↓ to SO output	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns

Note R_L and C_L are the resistance and capacitance of the SO output line load respectively.

SBI MODE ($\overline{SCK}$ ··· INTERNAL CLOCK OUTPUT (MASTER)):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 150$			ns
SB0 setup time (referred to $\overline{SCK}$↑)	t_{SIK3}			150			ns
SB0 hold time (referred to $\overline{SCK}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
Delay from $\overline{SCK}$↓ to SB0 output	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
Delay from $\overline{SCK}$↑ to SB0↓	t_{KSB}			t_{KCY3}			ns
Delay from SB0↓ to $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0 low-level width	t_{SBL}			t_{KCY3}			ns
SB0 high-level width	t_{SBH}			t_{KCY3}			ns

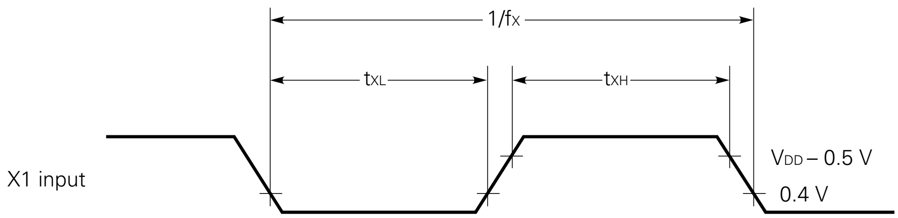
SBI MODE ($\overline{SCK}$ ··· EXTERNAL CLOCK INPUT (SLAVE)):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0 setup time (referred to $\overline{SCK}$↑)	t_{SIK4}			100			ns
SB0 hold time (referred to $\overline{SCK}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
Delay from $\overline{SCK}$↓ to SB0 output	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF **Note**	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
Delay from $\overline{SCK}$↑ to SB0↓	t_{KSB}			t_{KCY4}			ns
Delay from SB0↓ to $\overline{SCK}$↓	t_{SBK}			t_{KCY4}			ns
SB0 low-level width	t_{SBL}			t_{KCY4}			ns
SB0 high-level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L are the resistance and capacitance of the SB0 output line load respectively.

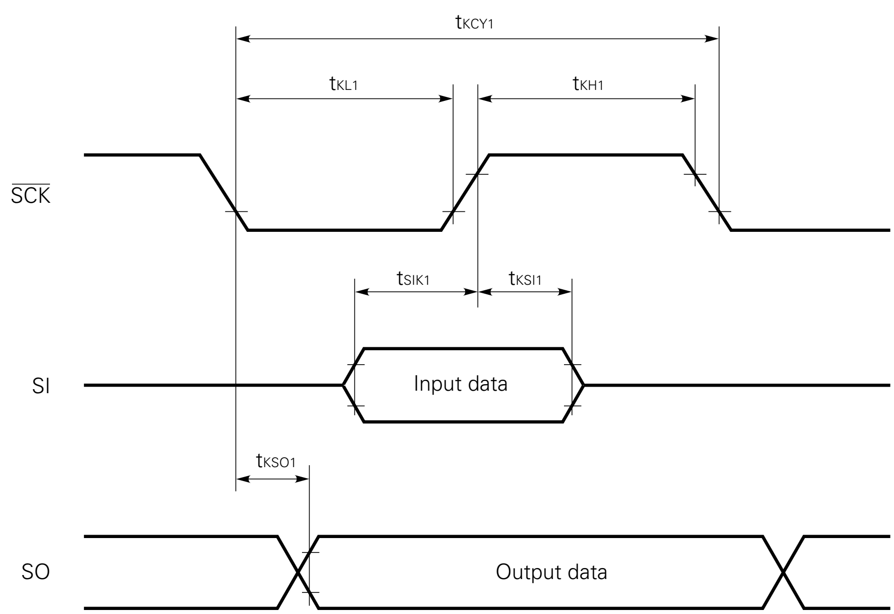
AC Timing Measurement Points (Excluding X1 Input)

Clock Timing



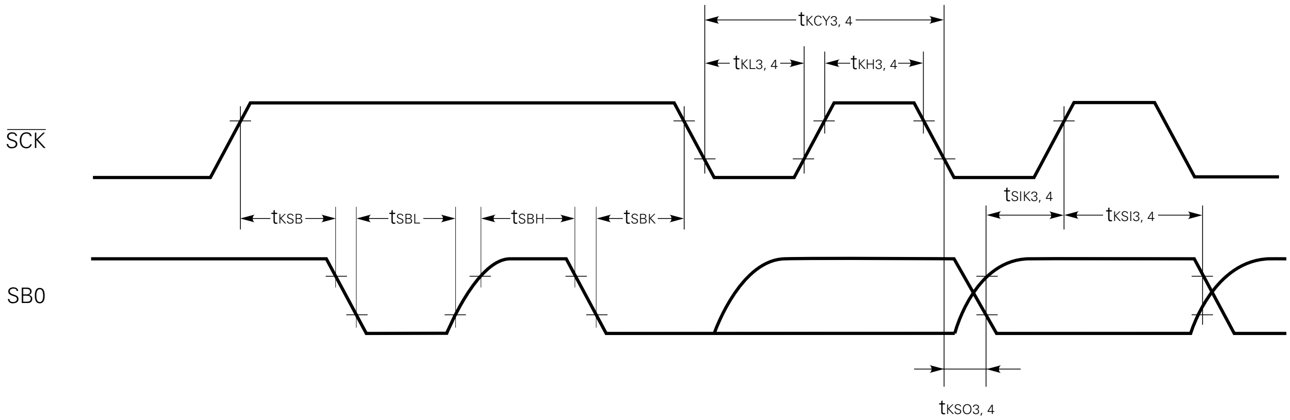
Serial Transfer Timing

Three-wire serial I/O mode:

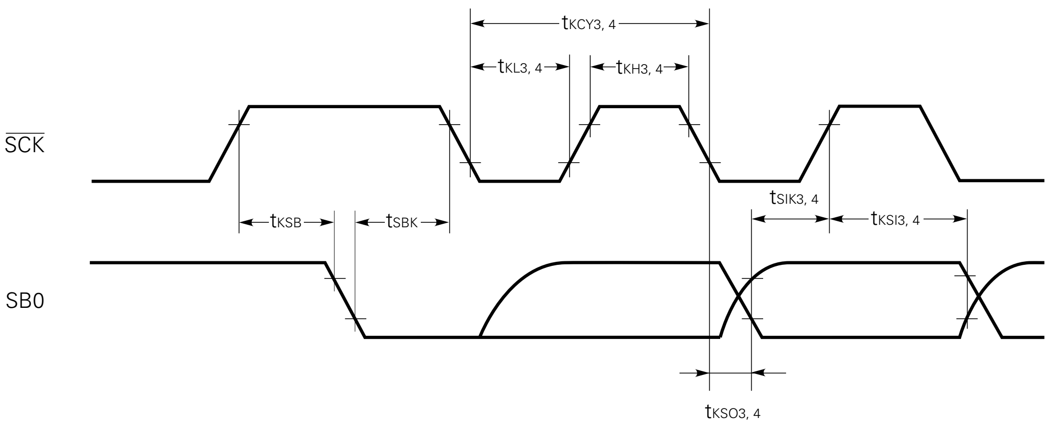


Serial Transfer Timing

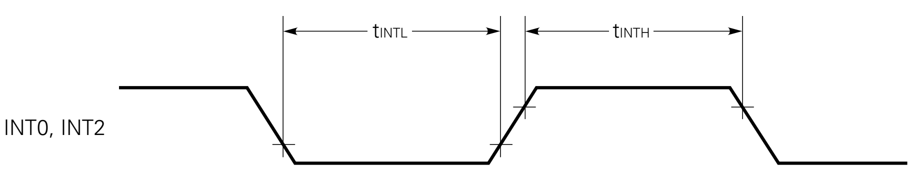
Bus release signal transfer:



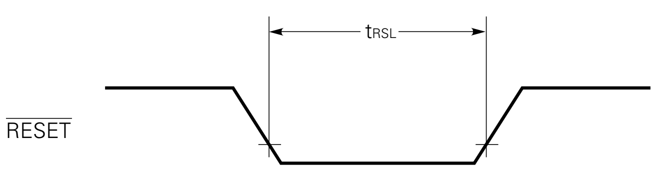
Command signal transfer:



Internal Input Timing



RESET Input Timing

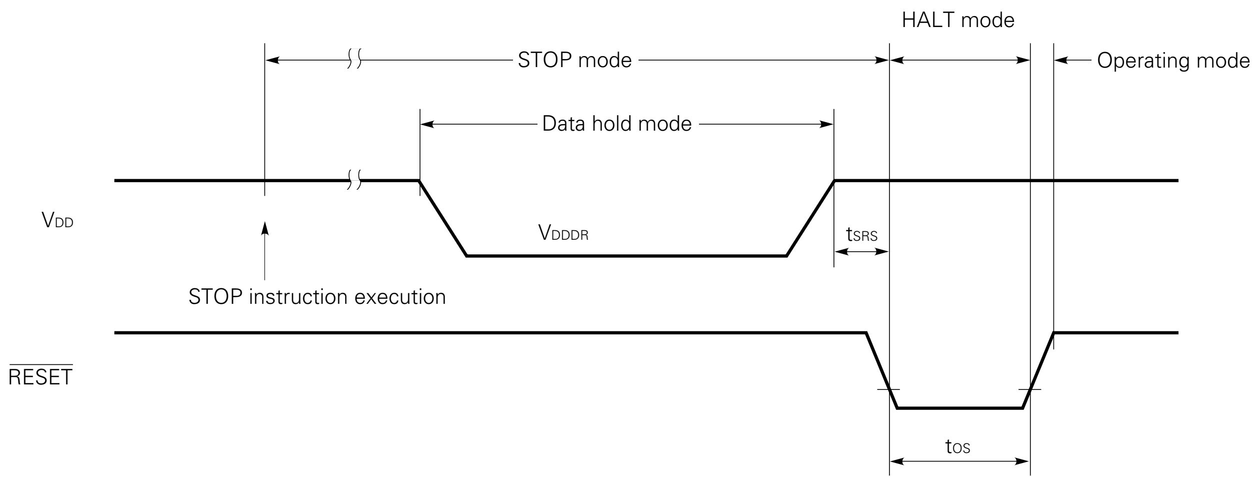


DATA HOLD CHARACTERISTICS AT LOW SUPPLY VOLTAGE IN DATA MEMORY STOP MODE

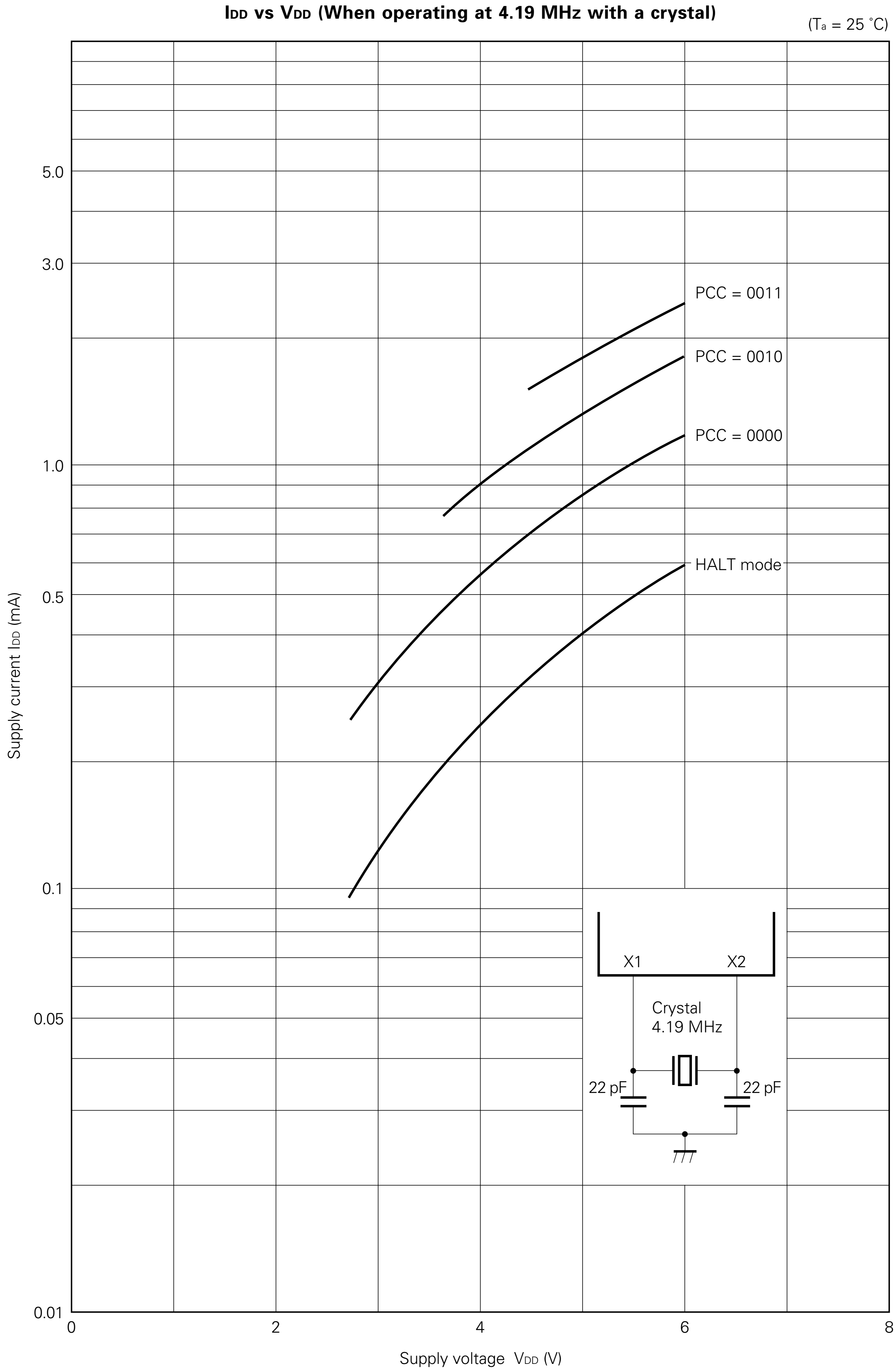
(T_a = –40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data hold supply voltage	V_{DDDR}		2.0		6.0	V
Data hold supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
$\overline{RESET}$ setup time	t_{SRS}		0			μs
Oscillation settling time	t_{OS}	After V_{DD} reaches the oscillation voltage range when the ceramic resonator is connected			4	ms
		After V_{DD} reaches the oscillation voltage range when the crystal is connected			10	ms

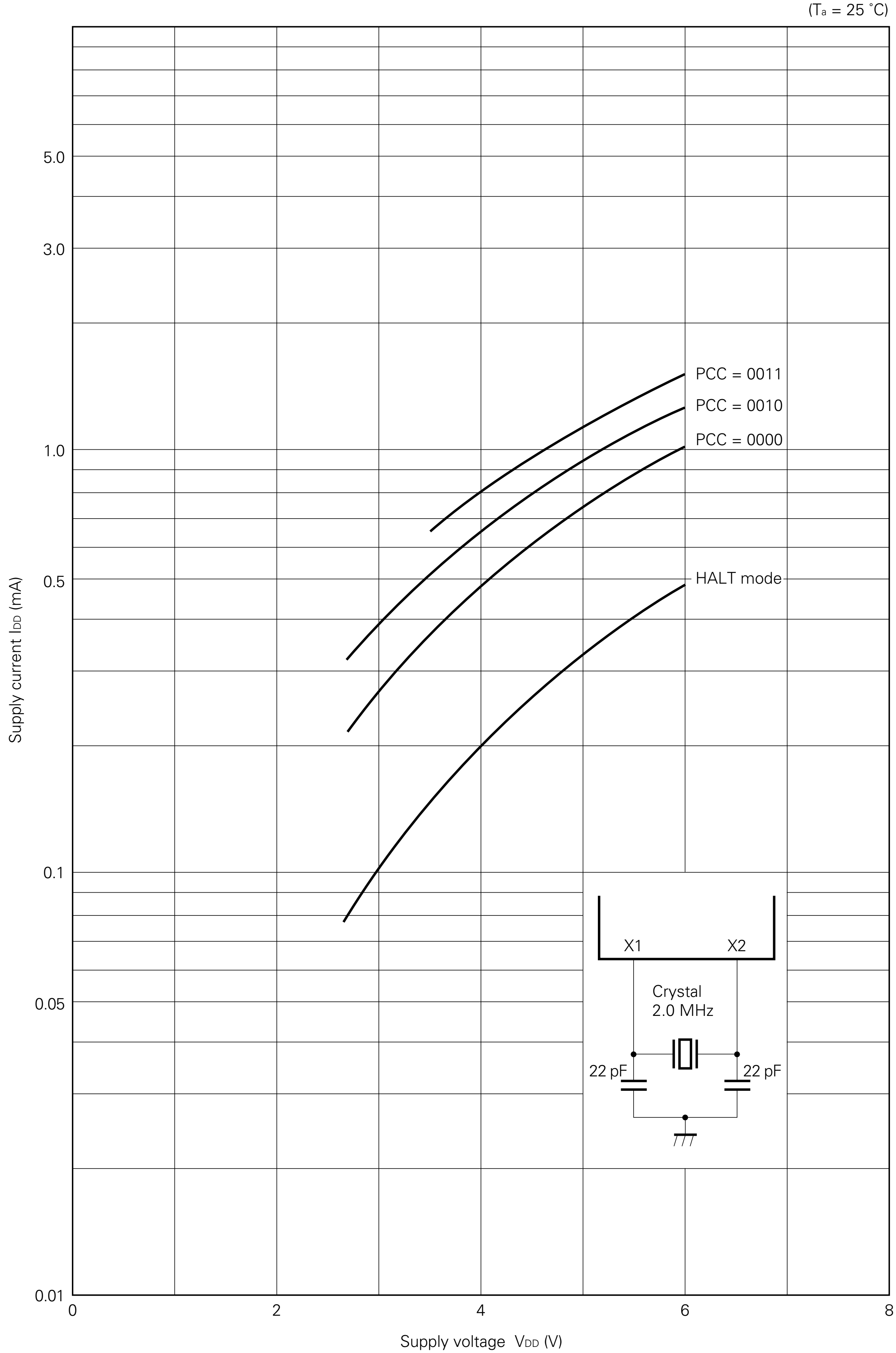
Data Hold Timing (STOP Mode Release by $\overline{RESET}$)



★ ## 11. CHARACTERISTIC CURVES (FOR REFERENCE)

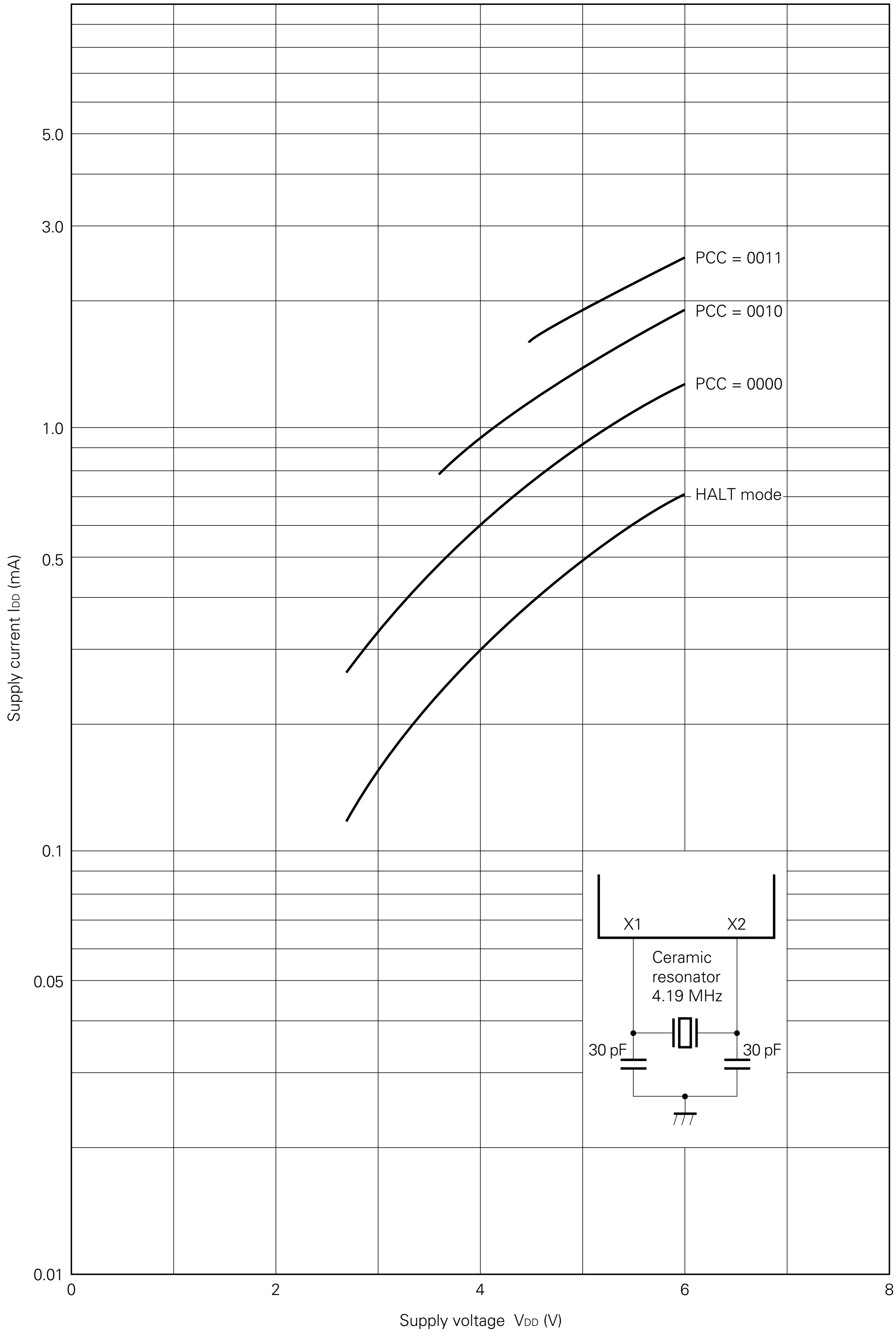


I_{DD} vs V_{DD} (When operating at 2.0 MHz with a crystal)

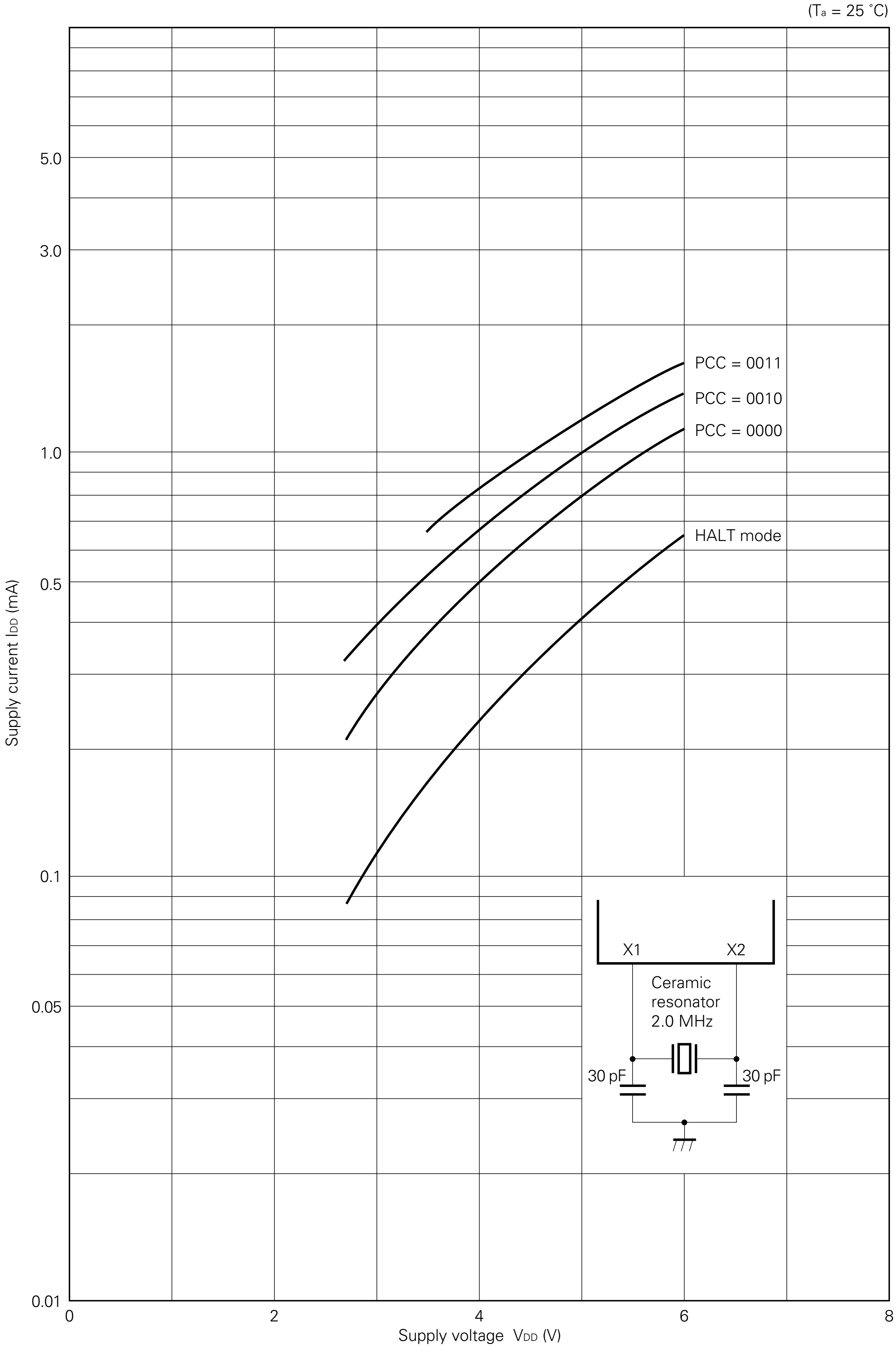


I_{DD} vs V_{DD} (When operating at 4.19 MHz with a ceramic resonator)

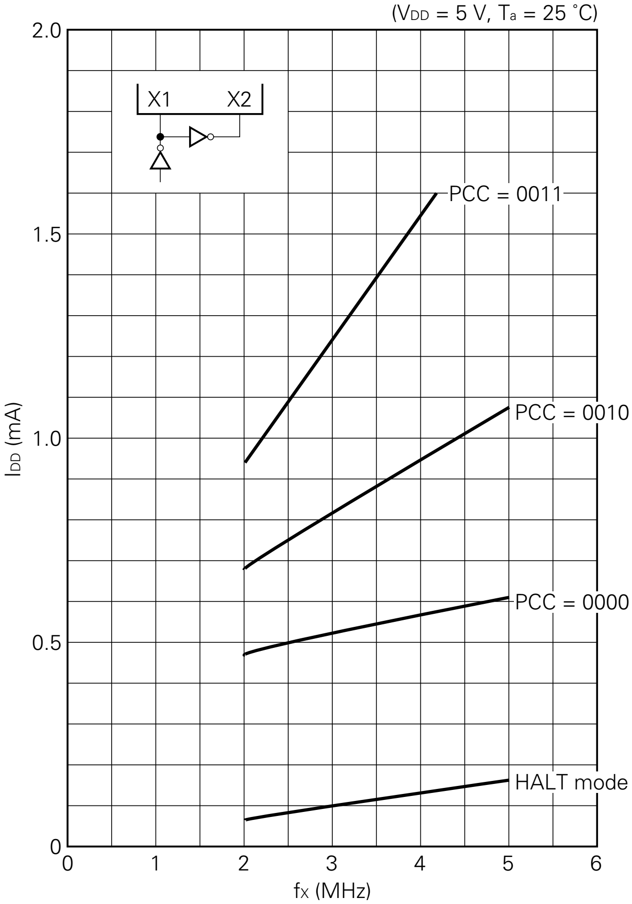
(T_a = 25 °C)



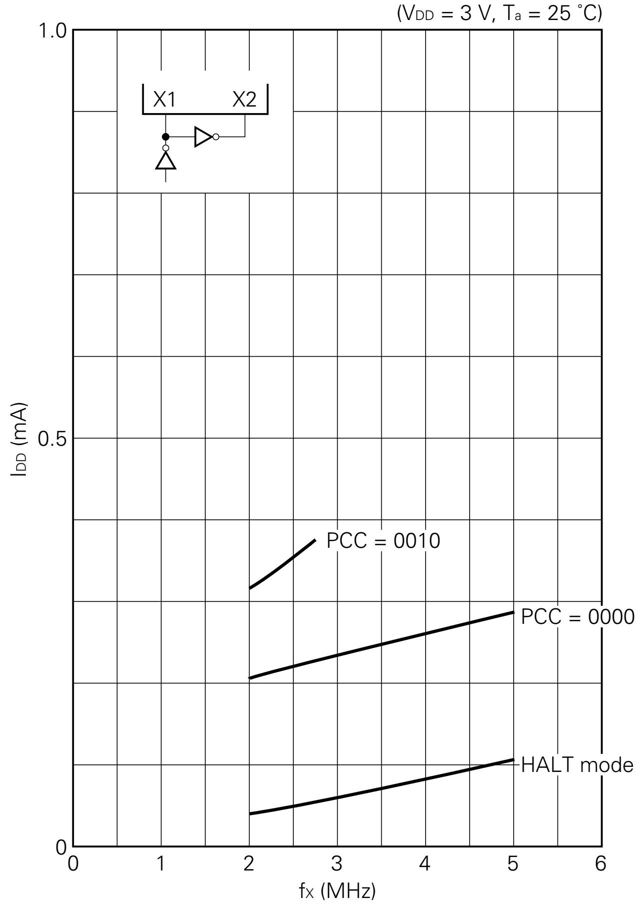
I_{DD} vs V_{DD} (When operating at 2.0 MHz with a ceramic resonator)



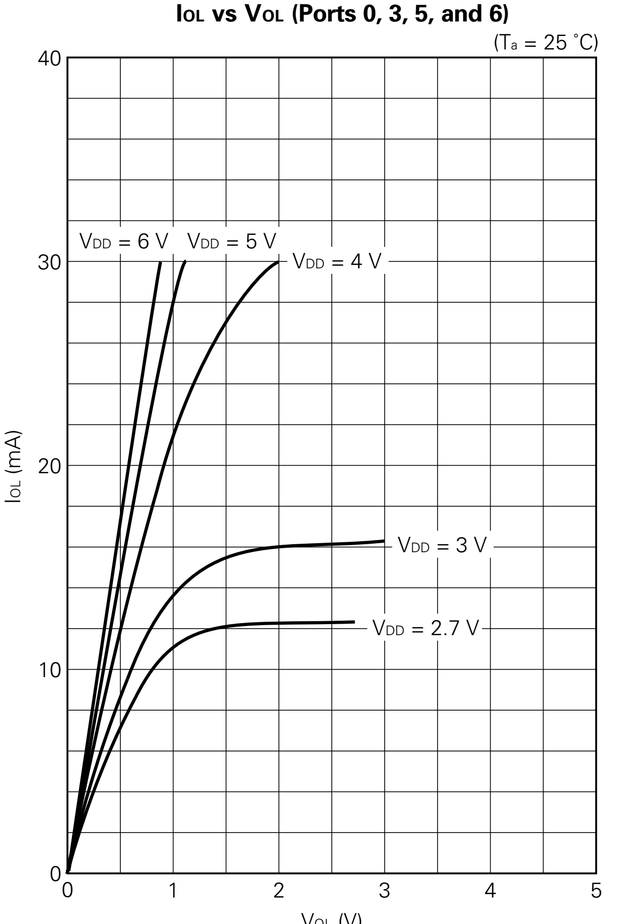
I_{DD} vs f_X



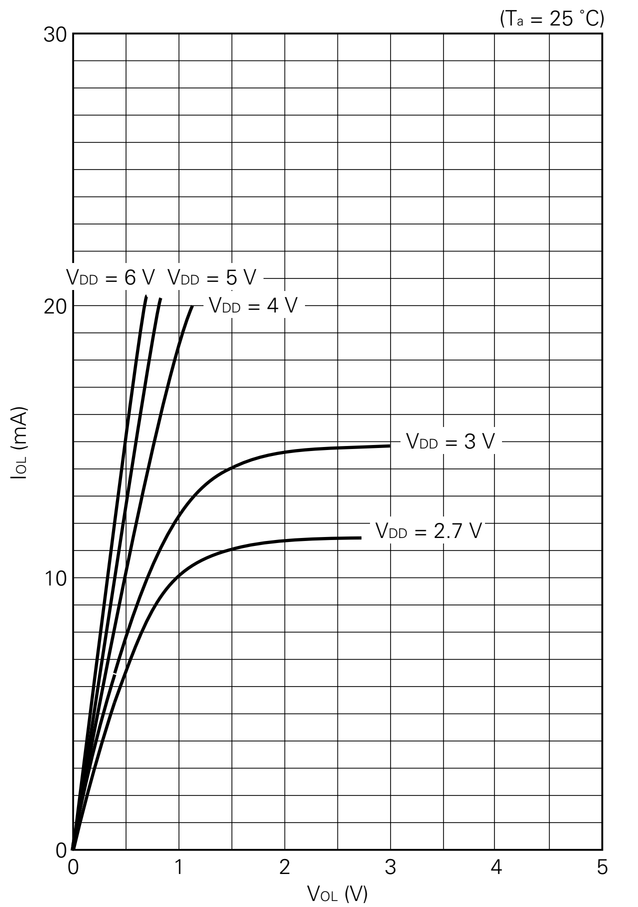
I_{DD} vs f_X



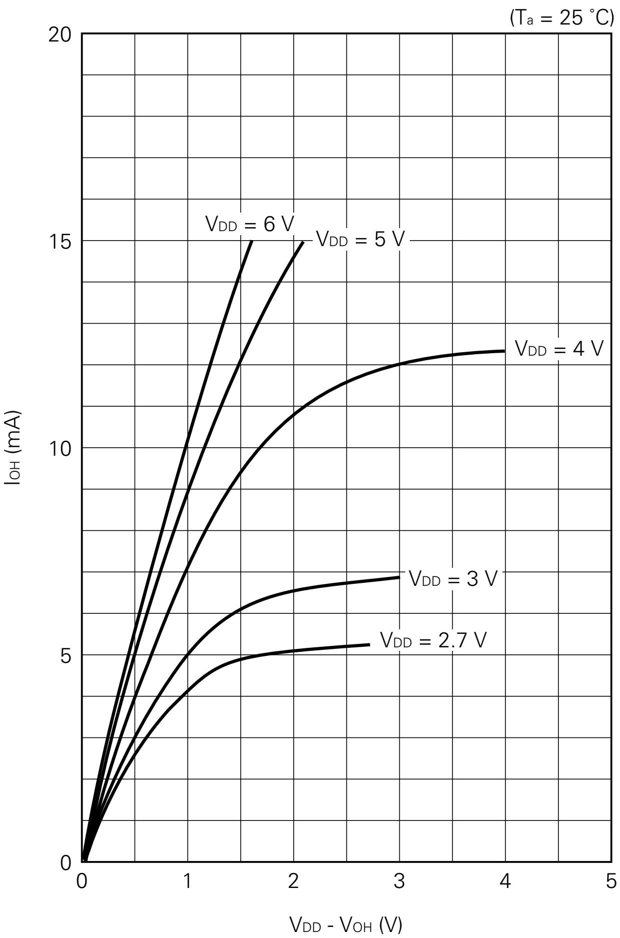
I_{OL} vs V_{OL} (Ports 0, 3, 5, and 6)



I_{OL} vs V_{OL} (Port 2)

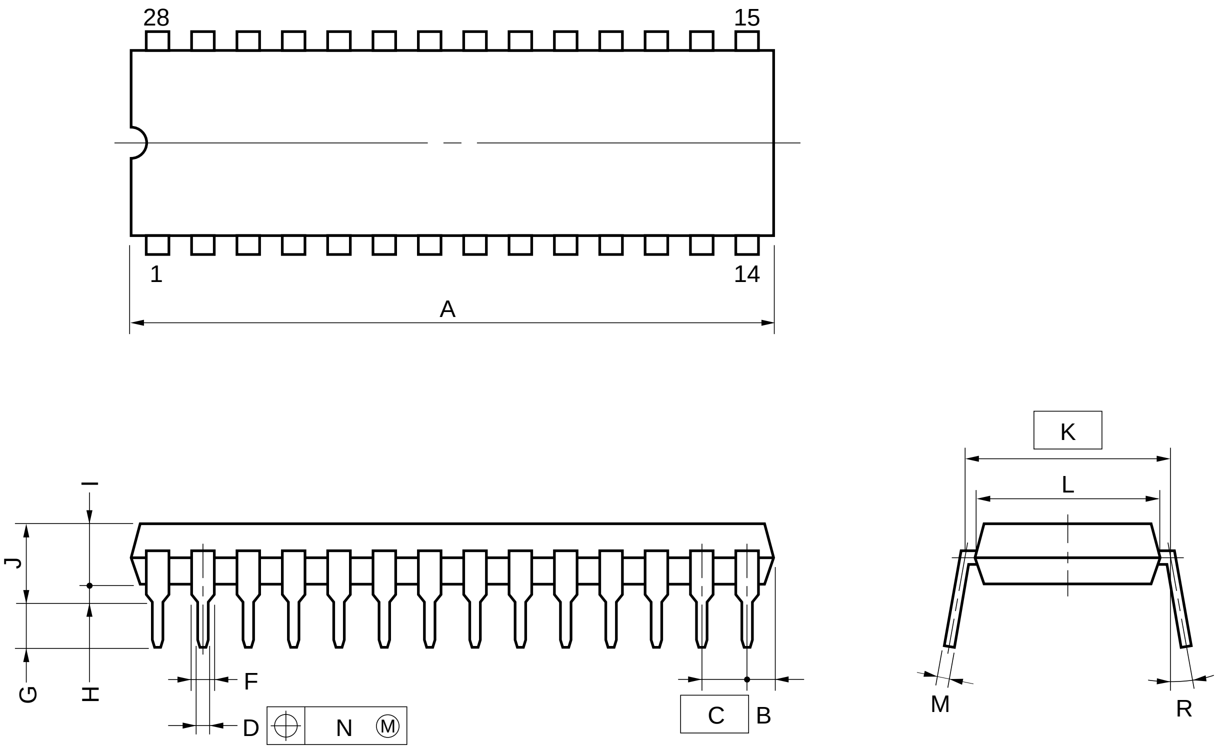


I_{OH} vs V_{OH} (Ports 0, 2, 3, and 6)



12. PACKAGE DIMENSIONS

28 PIN PLASTIC DIP (600 mil)



NOTES

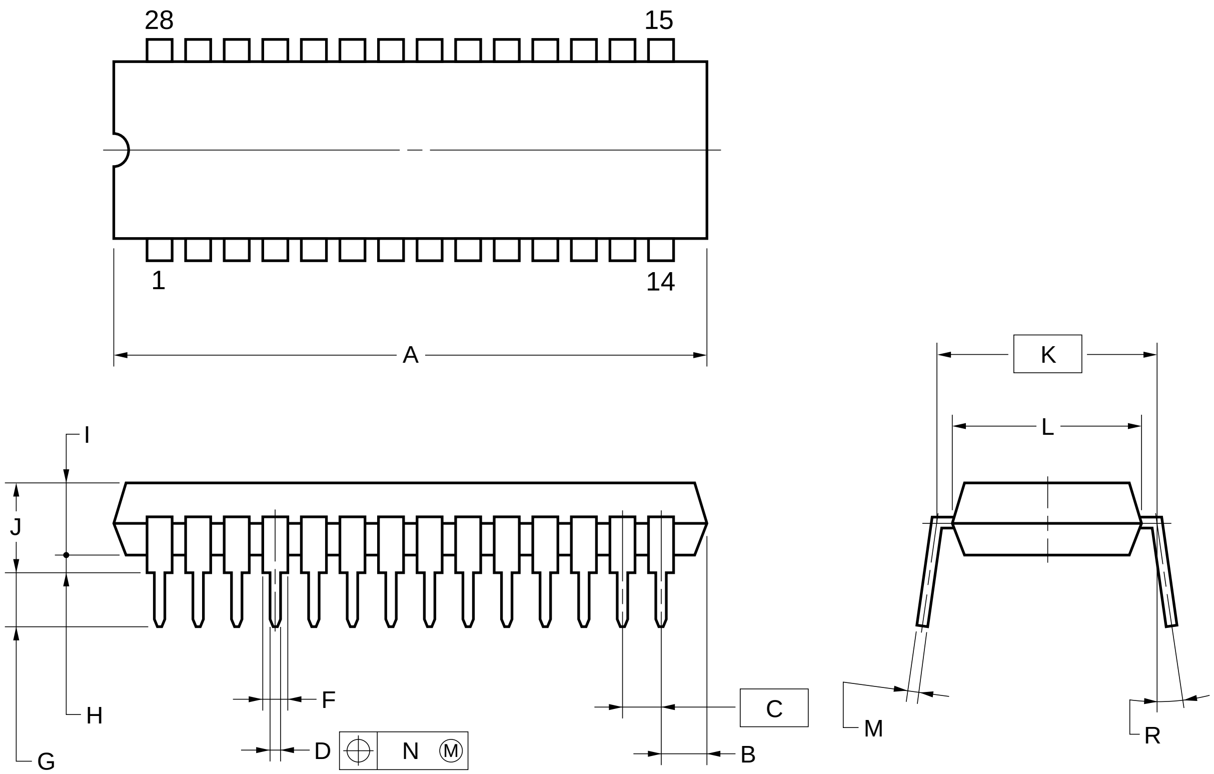
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	38.10 MAX.	1.500 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6±0.3	0.142±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
R	0 ~ 15°	0 ~ 15°

P28C-100-600A1-1

28PIN PLASTIC SHRINK DIP (400 mil)



NOTES

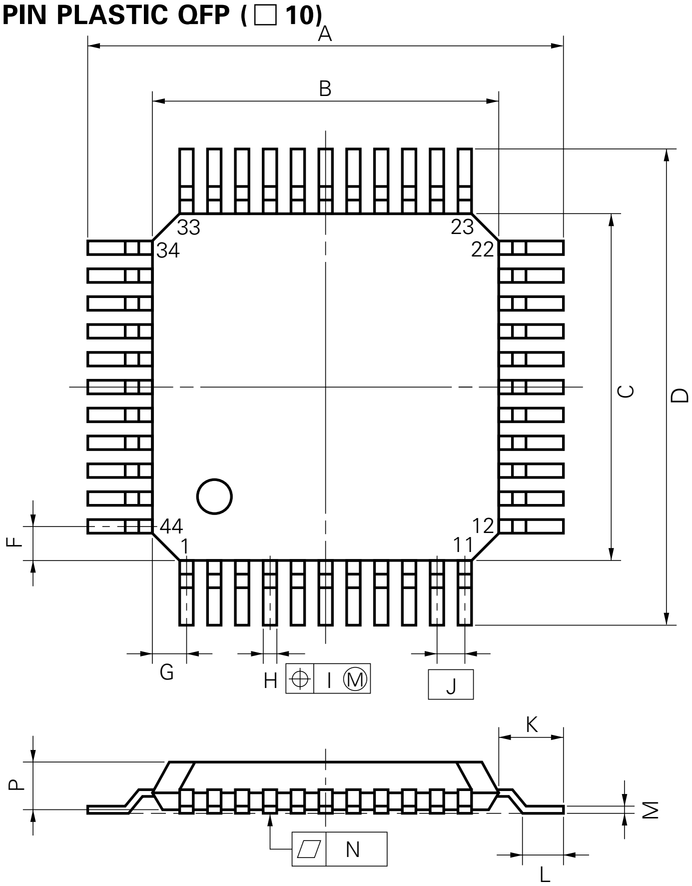
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

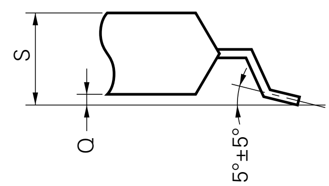
ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P28C-70-400A-1

★ 44 PIN PLASTIC QFP (□10)



Detail of lead end



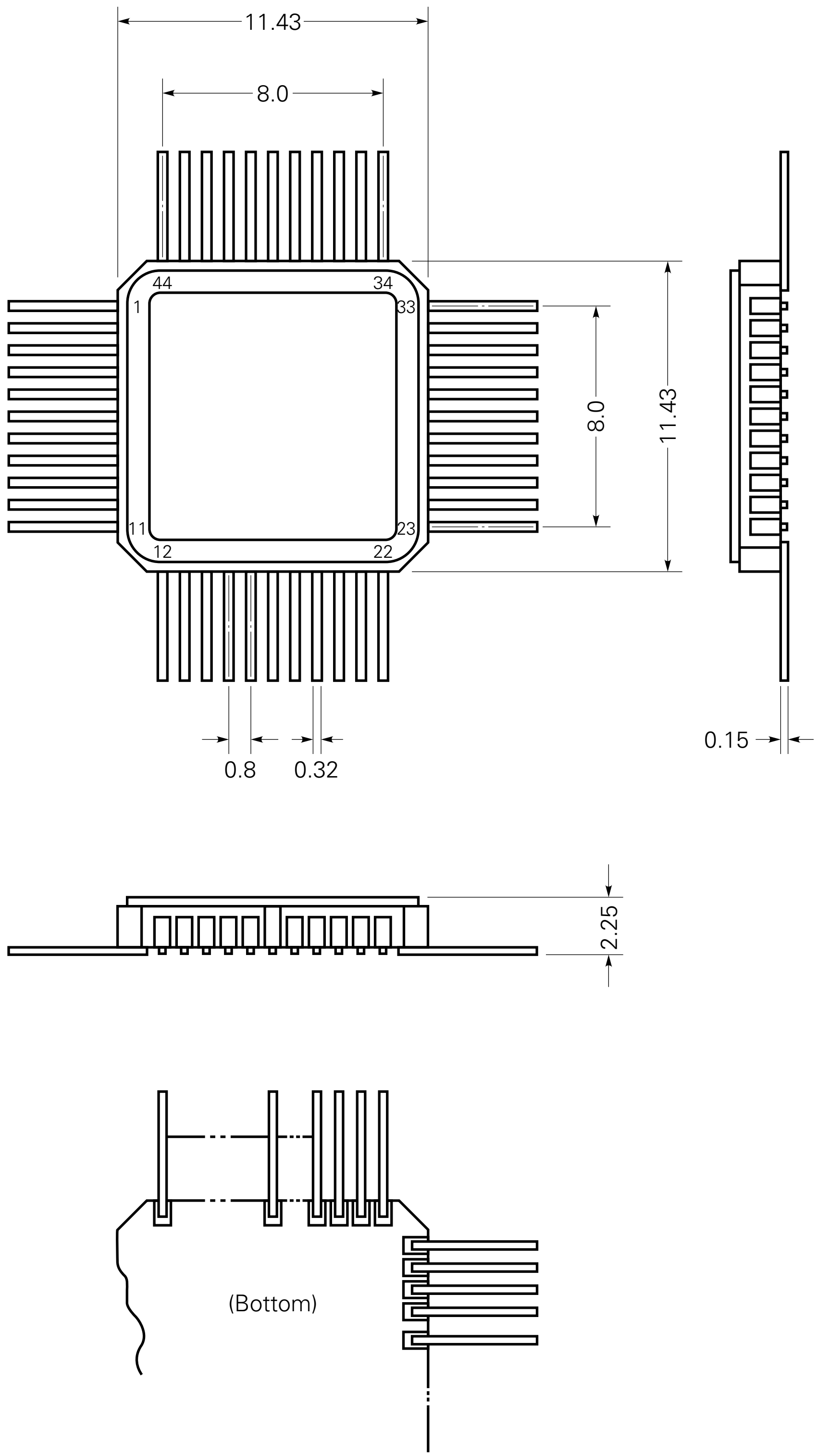
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P44GB-80-3B4-2

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

PACKAGE DIMENSIONS OF THE 44-PIN CERAMIC QFP FOR ES (REF. DWG.) (UNIT: mm)



Cautions 1. Find the location of pin 1 by checking the location of pin 17, which is connected to the metal cap.

2. The metal cap is connected to pin 17. The electrical level of the metal cap is V_{SS} (GND).

3. The lead length has not been specified because leads are cut without any detailed specifications.

13. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering the μPD75402A.

For the details of the recommended soldering conditions refer to our document "SMD Surface Mount Technology Manual" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 13-1 Soldering Conditions for Surface-Mount Devices

μPD75402AGB-×××-3B4: 44-pin plastic QFP (10 × 10 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 ˚C Reflow time: 30 seconds or less (at 210 ˚C or more) Number of reflow processes: 1	IR30-00-1
VPS	Peak package's surface temperature: 215 ˚C Reflow time: 40 seconds or less (at 200 ˚C or more) Number of reflow processes: 1	VP15-00-1
Wave soldering	Temperature in the soldering vessel: 260 ˚C or less Flow time: 10 seconds or less Number of soldering processes: 1 Pre-heating temperature: 120 ˚C max. (package surface temperature)	WS60-00-1
Partial heating method	Terminal temperature: 300 ˚C or less Flow time: 3 seconds or less (for each side of device)	–

Caution Do not apply more than a single process at once, except for "Partial heating method."

Table 13-2 Soldering Conditions for Inserted Devices

μPD75402AC-××× : 28-pin plastic DIP (600 mil)
μPD75402ACT-××× : 28-pin plastic shrink DIP (400 mil)

Soldering process	Soldering conditions
Wave soldering (only for leads)	Temperature in the soldering vessel: 260 °C or less Flow time: 10 seconds or less
Partial heating method	Terminal temperature: 260 °C or less Flow time: 10 seconds or less

Caution In wave soldering, apply solder only to the lead section. Care must be taken that jet solder does not contact the main body of the package.

Notice

Other versions of the products are available. For these versions, the recommended reflow soldering conditions have been mitigated as follows:
Higher peak temperature (235 °C), two-stage, and longer exposure limit.
Contact an NEC representative for details.

APPENDIX A FUNCTIONAL COMPARISON AMONG μPD75402A, μPD75402, AND μPD75P402

<table>
<tr><th colspan="2">Model</th><th>μPD75402A</th><th colspan="2">μPD75402</th><th>μPD75P402</th></tr>
<tr><td colspan="2">ROM (bytes)</td><td colspan="3">1920 (masked ROM)</td><td>1920 (PROM)</td></tr>
<tr><td colspan="2">RAM (× 4 bits)</td><td colspan="4">64</td></tr>
<tr><td colspan="2">Instruction cycle</td><td>0.95 μs, 1.91 μs, 15.3 μs
(when operating at 4.19 MHz)</td><td colspan="2">1.91 μs, 15.3 μs
(when operating at 4.19 MHz)</td><td>0.95 μs, 1.91 μs, 15.3 μs
(when operating at 4.19 MHz)</td></tr>
<tr><td rowspan="3">I/O ports</td><td>Input</td><td rowspan="3">22</td><td>6</td><td colspan="2" rowspan="2">16
(Pull-up resistors can be connected by software.)</td></tr>
<tr><td>I/O</td><td>12</td></tr>
<tr><td>N-ch I/O</td><td colspan="2">4
(Pull-up resistors can be connected by mask option.)</td><td>4 (No pull-up resistors can be connected.)</td></tr>
<tr><td colspan="2">Timer</td><td colspan="4">• Basic interval timer</td></tr>
<tr><td colspan="2">Serial interface</td><td colspan="4">• NEC standard serial bus interface
• Three-wire synchronous serial interface</td></tr>
<tr><td colspan="2">Vectored interrupt</td><td colspan="4">One external and two internal interrupts</td></tr>
<tr><td colspan="2">Test input</td><td colspan="4">One external input</td></tr>
<tr><td colspan="2">Supply voltage</td><td colspan="3">2.7 to 6.0 V</td><td>5 V ±10 %</td></tr>
<tr><td colspan="2">Operating temperature</td><td colspan="3">–40 to +85 °C</td><td>–10 to +70 °C</td></tr>
<tr><td colspan="2">Package</td><td colspan="4">• 28-pin plastic DIP
• 28-pin plastic shrink DIP
• 44-pin plastic QFP</td></tr>
</table>

APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided for developing systems including the μPD75402A:

Hardware	IE-75000-R Note 1 IE-75001-R	In-circuit emulator for the 75X series
	IE-75000-R-EM Note 2	Emulation board for the IE-75000-R and IE-75001-R
	EP-75402C-R	Emulation probe for the μPD75402AC and μPD75402ACT
	EP-75402GB-R EV-9200G-44	Emulation probe for the μPD75402AGB. A 44-pin conversion socket, the EV-9200G-44, is attached to the probe.
	PG-1500	PROM programmer
	PA-75P402CT	PROM programmer adapter for the μPD75P402C and μPD75P402CT. Connected to the PG-1500.
	PA-75P402GB	PROM programmer adapter for the μPD75P402GB. Connected to the PG-1500.
Software	IE control program	Host machine • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A Note 3) • IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

Notes 1. Maintenance service only

2. Not contained in the IE-75001-R

3. These software cannot use the task swap function, which is available in MS-DOS Ver. 5.00 and Ver. 5.00A.

Remark Refer to "75X Series Selection Guide" (IF-1027) for development tools manufactured by third parties.

APPENDIX C RELATED DOCUMENTS ★

Documents related to the device

Document name	Document No.
User's manual	IEU-644
Application note	IEA-638
75X series selection guide	IF-1027

Documents related to development tools

	Document name		Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1416
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75402C-R User's Manual		EEU-701
	EP-75402GB-R User's Manual		EEU-702
	PG-1500 User's Manual		EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-1346
		Language	EEU-1363
	PG-1500 Controller User's Manual		EEU-1291

Other related documents

Document name	Document No.
Package Manual	IEI-1213
SMD Surface Mount Technology Manual	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEI-1203
Electrostatic Discharge (ESD) Test	IEI-1201
Guide to Quality Assurance for Semiconductor Devices	MEI-1202

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

[MEMO]

[MEMO]