DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD75516(A)

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75516(A) is a product in the 75X series (of 4-bit single-chip microcomputers). The 75X series has an architecture which is comparable to that of 8-bit microcomputers.

The μPD75516(A) possesses high class processing capacities as a 4-bit single-chip microcomputer with built-in A/D converter and serial interface, including the capability to process data in lengths of 1, 4 and 8 bits in addition to its high speed operation.

Functions are described in detail in the following User'S Manual, which should be read when carrying out design work.

μPD75516 User's Manual: IEM-5049

FEATURES

- Higher reliability than μPD75516
- A large number of I/O Lines: 64 lines (Internal pull-up/pull- down resistor specifiable: 47)
- Built-in 8-bit serial interface: 2 channels
  Built-in NEC standard serial bus interface (SBI)
- Built-in 8-bit AD converter: 8 channels
- High speed operation and a instruction execution time variation function which is effective for saving power.
  - 0.95 μs/1.91 μs/15.3 μs (at 4.19 MHz operation), 122 μs (at 32.768 kHz operation)
- Program memory (ROM) capacity: 16256 × 8 bits
- Data memory (RAM) capacity: 512 × 4 bits
- Powerful timer function: 4 channels
  - 8-bit timer/event counter
  - Watch timer
  - 8-bit basic interval timer
  - Timer/pulse generator: 14-bit PWM output capability
- Ultra low power consumption watch operation is possible (5 μA TYP.: During operation at 3 V)
- Devices with built-in PROM are available (μPD75P516)

USES

Automotive electrical equipment, etc.

The information in this document is subject to change without notice.

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Date Published October 1993 P
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μPD75516GF(A)-×××-3B9	80-pin plastic QFP (14 × 20 mm)	Special

Remarks "×××" means the specified ROM code.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

DIFFERENCES BETWEEN μPD75516(A) AND μPD75516

Item \ Product Name		μPD75516(A)	μPD75516
Quality grade		Special	Standard
Electrical specification	Absolute maximum rating	Differ in high-level output current and low-level output current.	
	DC characteristic	Differ in low-level output voltage.	
	A/D converter characteristic	Differ in ambient temperature range and absolute accuracy.	

LIST OF μPD75516(A) FUNCTIONS

Item			Function
On-chip memory		ROM	16256 × 8 bits
		RAM	512 × 4 bits
General registers			(4 bits × 8 or 8 bits × 4) × 4 banks
Instruction cycle			• 0.95 μs/1.91 μs/15.3 μs (Main system clock : at 4.19 MHz operation) • 122 μs (Subsystem clock : at 32.768 kHz operation)
Input/output ports	Total		64
	CMOS input		16 (dual function and analog input as INT, SIO, PPO, software pull-up capability: 7)
	CMOS input/output		28 • Software pull-up capability : 16 • Mask option pull-down capability: 4
	N-ch open-drain input/output		20 (10 V withstand voltage, mask option pull-up capability: 20)
A/D converter			8-bit resolution × 8 channels (successive approximation type) • Operating voltage: V_{DD} = 3.5 to 6.0 V
Timer/counters			4 channels { • Timer/event counter • Basic interval timer • Timer/pulse generator (14-bit PWM output capability) • Watch timer
Serial Interface			2 channels { • NEC standard serial bus interface (SBI)/3-wire SIO: 1 channel • Normal clocked serial interface (3-wire SIO): 1 channel
Vectored interrupts			External: 3, internal: 4
Test inputs			External: 1, internal: 1
Instruction set			• Bit data set/reset/test/Boolean operations • 4-bit data transfer, operation, increment/ decrement, compare • 8-bit data transfer, operation, increment/ decrement, compare
System clock oscillator			• Ceramic/crystal oscillator for main system clock oscillation: 4.19 MHz • Crystal oscillator for subsystem clock oscillation: 32.768 kHz
Operating power supply			VDD = 2.7 to 6.0 V
Package			80-pin plastic QFP (14 × 20 mm)

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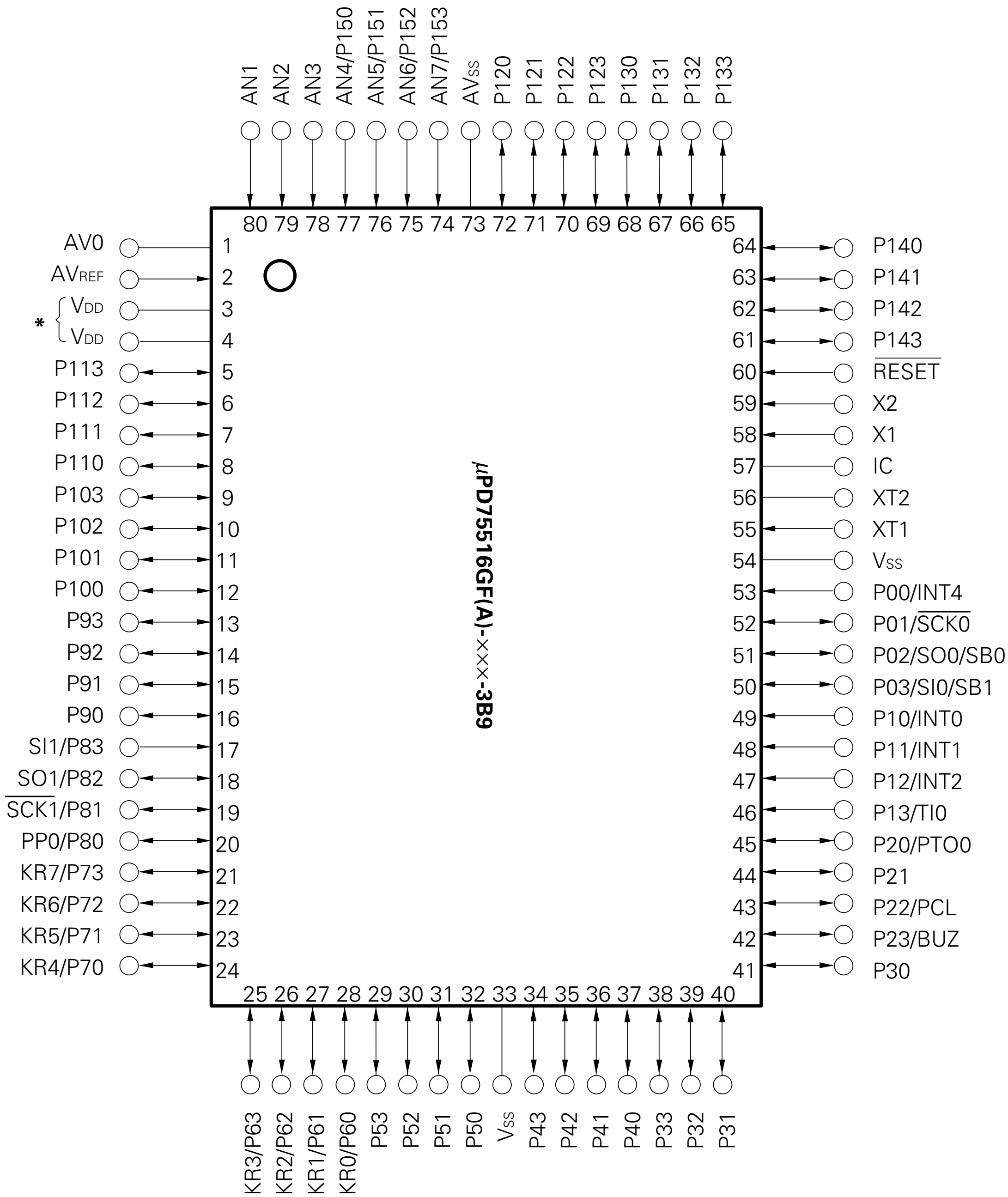
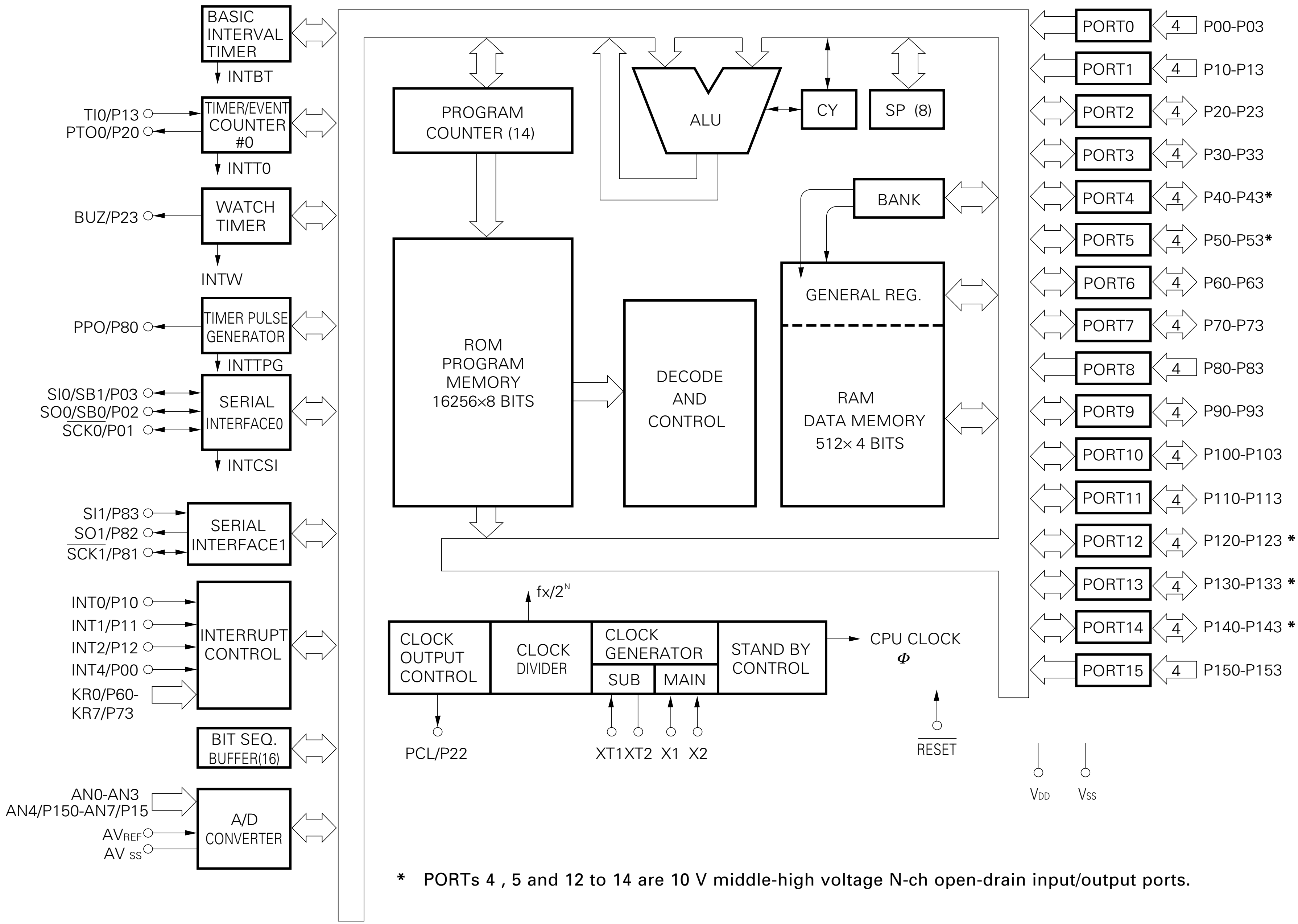
1. PIN CONFIGURATION



IC: Internally Connected (Connect to V_{SS}.)

* Be sure to supply power to both V_{DD} pins.

2. BLOCK DIAGRAM



* PORTs 4 , 5 and 12 to 14 are 10 V middle-high voltage N-ch open-drain input/output ports.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Dual-Function Pin	Function	8-Bit I/O	After Reset	Input/Output Circuit Type*
P00	Input	INT4	4-bit input port (PORT0). Internal pull-up resistor can be specified in 3-bit units by software for P01 to P03.	×	Input	Ⓑ
P01		$\overline{\text{SCK0}}$				Ⓕ – A
P02		SO0/SB0				Ⓕ – B
P03		SI0/SB1				Ⓜ – C
P10	Input	INT0	Noise removing function available	×	Input	Ⓑ – C
P11		INT1				
P12		INT2	4-bit input port (PORT1). Internal pull-up resistor can be specified in 4-bit units by software.			
P13		TI0				
P20	Input/ output	PTO0	4-bit input/ output port (PORT2). Internal pull-up resistor can be specified in 4-bit units by software.	×	Input	E – B
P21		—				
P22		PCL				
P23		BUZ				
P30	Input/ output	—	Programmable 4-bit input/ output port (PORT3). Input/ output specifiable in 1-bit units. Internal pull-up resistor can be specified in 4-bit units by software.	×	Input	E – C
P31		—				
P32		—				
P33		—				
P40 to P43	Input/ output	—	N-ch open-drain 4-bit input/output port (PORT4). Pull-up resistor can be incorporated in 1-bit units (mask option). 10 V withstand voltage with open-drain.	○	High level (when a pull-up resistor is incorporated) or high impedance	M
P50 to P53	Input/ output	—	N-ch open-drain 4-bit input/ output port (PORT5). Pull-up resistor can be incorporated in 1-bit units (mask option). 10 V withstand voltage with open-drain.		High level (when a pull-up resistor is incorporated) or high impedance	M
P60	Input/ output	KR0	Programmable 4-bit input/output port (PORT6). Input/output specifiable in 1-bit units. Internal pull-up resistor can be specified in 4-bit units by software.	○	Input	Ⓕ – C
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/ output	KR4	4-bit input/output port (PORT7). Internal pull-up resistor can be specified in 4-bit units by software.		Input	Ⓕ – A
P71		KR5				
P72		KR6				
P73		KR7				

* Schmitt trigger inputs are circled.

3.1 PORT PINS (2/2)

Pin Name	I/O	Dual-Function Pin	Function	8-Bit I/O	After Reset	Input / Output Circuit Type *
P80	Input	PPO	4-bit input port (PORT8).	×	Input	E
P81		$\overline{SCK1}$				Ⓕ
P82		SO1				E
P83		SI1				Ⓑ
P90 to P93	Input/ output	——	4-bit input/output port (PORT8) Pull-up resistor can be incorporated in 1-bit units (mask option).	×	Low level (when a pull down resistor is incorporated) or high impedance	V
P100 to P103	Input/ output	——	4-bit input/output port (PORT10).	×	Input	E
P110 to P113	Input/ output	——	4-bit input/output port (PORT11).		Input	E
P120 to P123	Input/ output	——	N-ch open-drain 4-bit input/ output port (PORT12). Pull-up resistor can be incorporated in 1-bit units (mask option). 10 V withstand voltage with open-drain.	×	High level (when a pull-up resistor is incorporated) or high impedance	M
P130 to P133	Input/ output	——	N-ch open-drain 4-bit input/ output port (PORT13). Pull-up resistor can be incorporated in 1-bit units (mask option). 10 V withstand voltage with open-drain.	×	High level (when a pull-up resistor is incorporated) or high impedance	M
P140 to P143	Input/ output	——	N-ch open-drain 4-bit input/ output port (PORT14). Pull-up resistor can be incorporated in 1-bit units (mask option). 10 V withstand voltage with open-drain.	×	High level (when a pull-up resistor is incorporated) or high impedance	M
P150 to P153	Input	AN4 to AN7	4-bit input/output port (PORT15).	×	Input	Y-A

* Schmitt trigger inputs are circled.

3.2 NON-PORT PINS

Pin Name	I/O	Dual-Function Pin	Function	After Reset	Input / Output Circuit Type *
TI0	Input	P13	External event pulse input to the timer/event counter.	—	Ⓑ – C
PTO0	Output	P20	Timer/event counter output .	Input	E – B
PCL	Output	P22	Clock output.	Input	E – B
BUZ	Output	P23	Fixed frequency output (for buzzer or system clock trimming).	Input	E – B
$\overline{SCK0}$	Input/ output	P01	Serial clock input/output .	Input	Ⓕ – A
SO0/SB0	Input/ output	P02	Serial data output. Serial bus input/output.	Input	Ⓕ – B
SI0/SB1	Input/ output	P03	Serial data input pin. Serial bus input/output.	Input	Ⓜ – C
INT4	Input	P00	Edge-detected vectored interrupt input (valid for detection of rising and falling edges).	—	Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input (detected edge selection possible). — Clocked	—	Ⓑ – C
INT1	Input	P11	Edge-detected vectored interrupt input (detected edge selection possible). — Asynchronous	—	Ⓑ – C
INT2	Input	P12	Edge-detected testable input (rising edge detection). — Asynchronous	—	Ⓑ – C
KR0 to KR3	Input	P60 to P63	Serial falling edge detection testable input.	Input	Ⓕ – C
KR4 to KR7	Input	P70 to P73	Serial falling edge detection testable input.	Input	Ⓕ – A
$\overline{SCK1}$	Input/ output	P81	Serial clock input/output.	Input	Ⓕ
SO1	Output	P82	Serial data output.	Input	E
SI1	Input	P83	Serial data input.	Input	Ⓑ
AN0 to AN3	Input	—	A/D converter analog input.	—	Y
AN4 to AN7	Input	P150 to P153	A/D converter analog input.	—	Y-A
AV_{REF}	Input	—	A/D converter reference voltage input.	—	Z
AV_{SS}	—	—	A/D converter reference GND potential.	—	—
X1, X2	Input	—	Main system clock oscillation crystal/ceramic connection pin. An external clock is input to X1 and an antiphase clock is input to X2.	—	—
XT1	Input	—	Subsystem clock oscillation crystal connection pin. An external clock is input to XT1 and XT2 is leave open.	—	—
XT2	—	—	Subsystem clock oscillation crystal connection pin. An external clock is input to XT1 and XT2 is leave open.	—	—
$\overline{RESET}$	Input	—	System reset input.	—	Ⓑ
PPO	Output	P80	Timer/pulse generator pulse output	Input	E
IC	—	—	Internally Connected. Connect to V_{SS} directly.	—	—
V_{DD}	—	—	Positive power supply.	—	—
V_{SS}	—	—	GND potential.	—	—

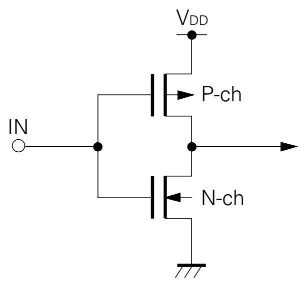
* Schmitt trigger inputs are circled.

3.3 PIN INPUT/OUTPUT CIRCUIT LIST

Use of simplified forms of the input/output circuit for each pin of the μPD75516(A) are shown as follows.

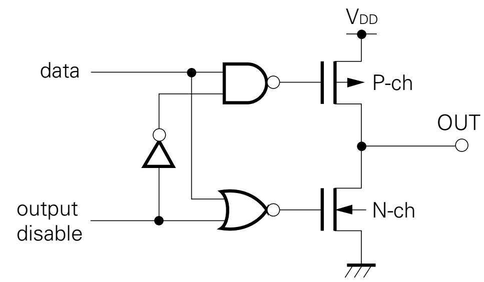
Fig. 3-1 List of Pin Input/Output Circuit (1/3)

TYPE A



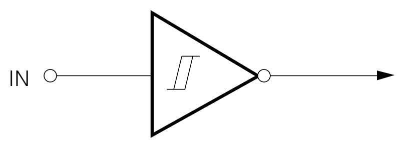
CMOS Standard Input Buffer

TYPE D



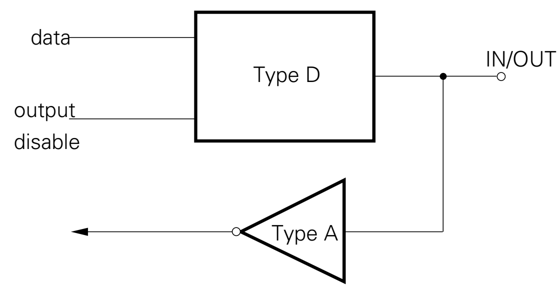
Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

TYPE B



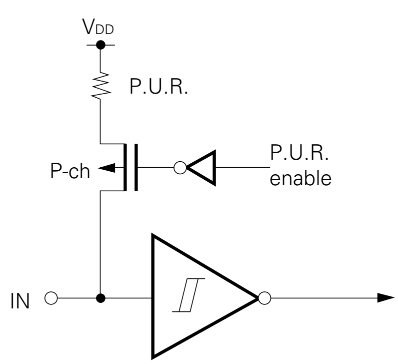
Schmitt-Trigger Input with Hysteresis Characteristic

TYPE E



Input/Output Circuit Consisting of Type D Push-Pull Output and Type A Input Buffer

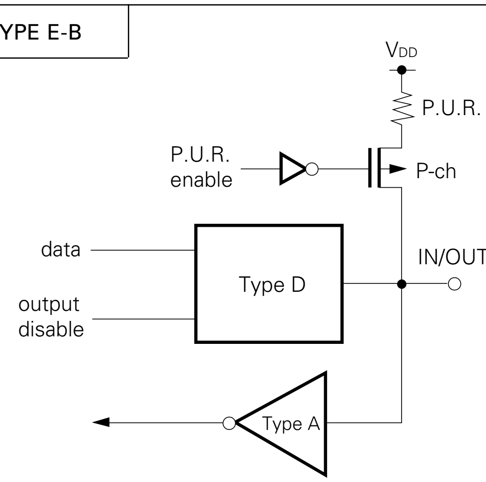
TYPE B-C



P.U.R. : Pull-Up Resistor

Schmitt-Trigger Input with Hysteresis Characteristic

TYPE E-B



P.U.R.:Pull-Up Resistor

Fig. 3-1 List of Pin Input/Output Circuit (2/3)

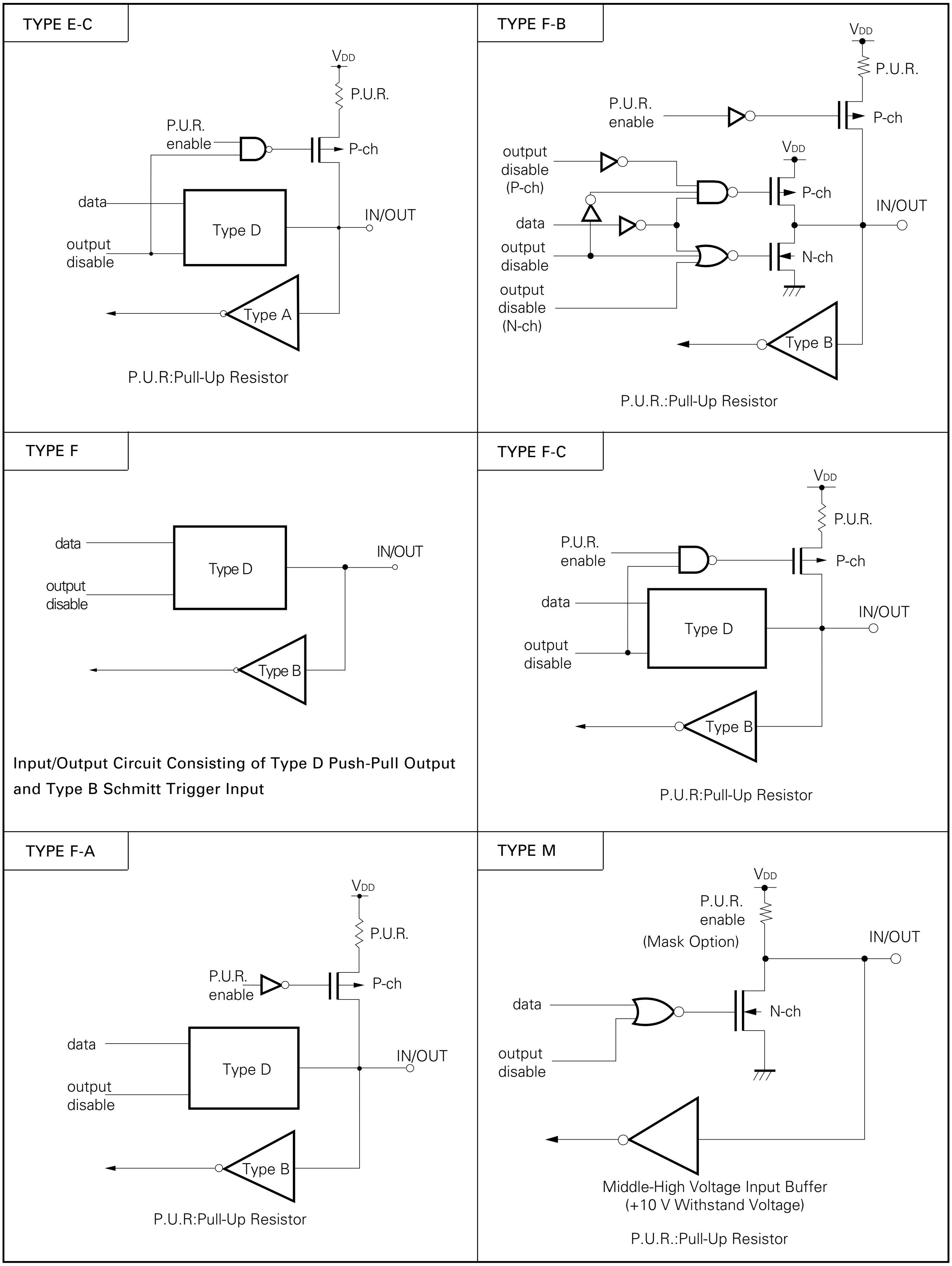
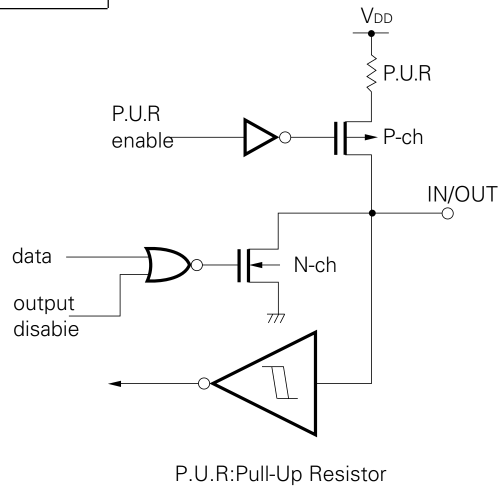
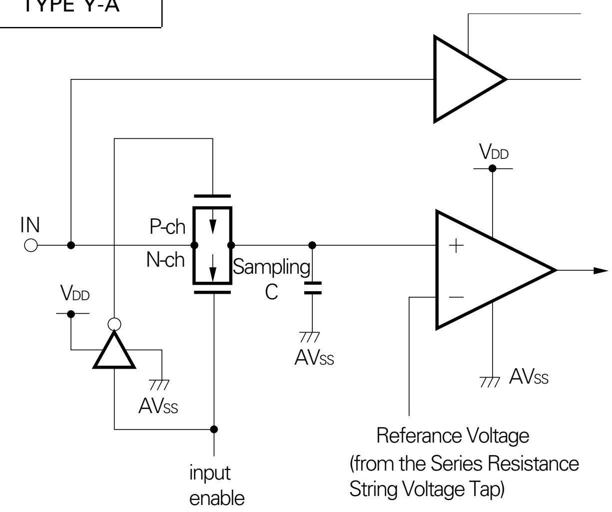


Fig. 3-1 List of Pin Input/Output Circuit (3/3)

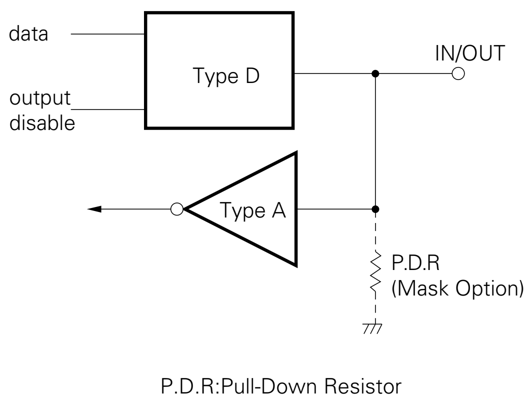
TYPE M-C



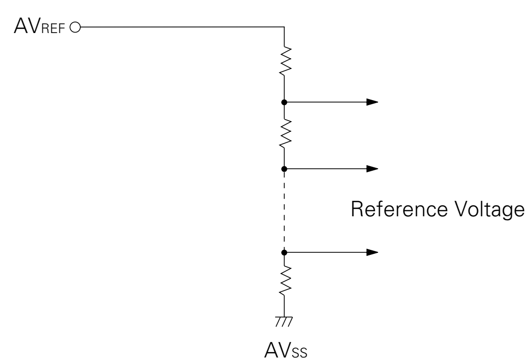
TYPE Y-A



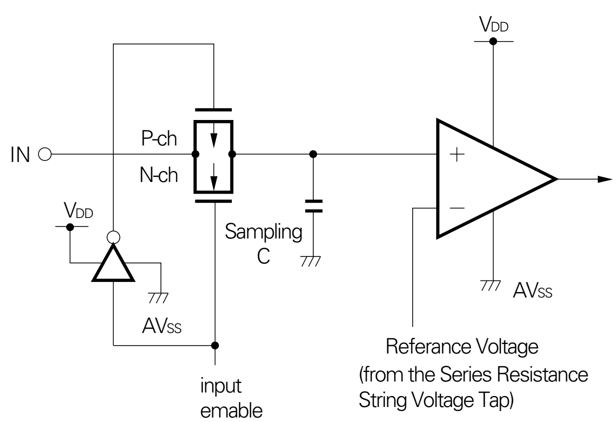
TYPE V



TYPE Z



TYPE Y



3.4 RECOMMENDED CONNECTIONS OF UNUSED PINS

Table 3-1 Recommended Connection of Unused Pins

Pin	Recommended Connection
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK0}$	Connect to V_{SS} or V_{DD}
P02/SO0/SB0	
P03/SI1/SB1	
P10/INT0 to P12/INT2	Connect to V_{SS}
P13/TI0	
P20/PTO0	Input state : Connect to V_{SS} or V_{DD} Ouput state : Leave open
P21	
P22/PCL	
P23/BUZ	
P30 to P33	
P40 to P43	
P50 to P53	
P60/KR0 to P63/KR3	
P70/KR4 to P73/KR7	
P80/PPO	Connect to V_{SS} or V_{DD}
P81/$\overline{SCK1}$	
P82/SO1	
P83/SI1	
P90 to P93	Input state : Connect to V_{SS} or V_{DD} Ouput state : Leave open
P100 to P103	
P110 to P113	
P120 to P123	
P130 to P133	
P140 to P143	
P150/AN4 to P153/AN7	Connect to V_{SS}
AN0 to AN3	
XT1	Connect to V_{SS} or V_{DD}
XT2	Leave open
AV_{REF}	Connect to V_{SS}
AV_{SS}	
IC	Connect directly to V_{SS}

3.5 MASK OPTION SELECTION

The following mask options are available for the pins.

(1) Specification of internal pull-up/pull-down resistor

Table 1-2 Pull-Up/Pull-Down Resistor Selection

Pins	Mask Option	
P40 to P43, P50 to P53, P120 to P123, P130 to P133, P140 to P143	1 With pull-up resistor (specifiable bit-wise)	2 Without pull-up resistor (specifiable bit-wise)
P90 to P93	1 With pull-down resistor (specifiable bit-wise)	2 Without pull-down resistor (specifiable bit-wise)

(2) Specification of internal feedback resistor for subsystem clock oscillation

Table 1-3 Feedback Resistor Selection

Pins	Mask Option	
XT1, XT2	1 With feedback resistor (subsystem clock used)	2 Without feedback resistor (subsystem clock not used)

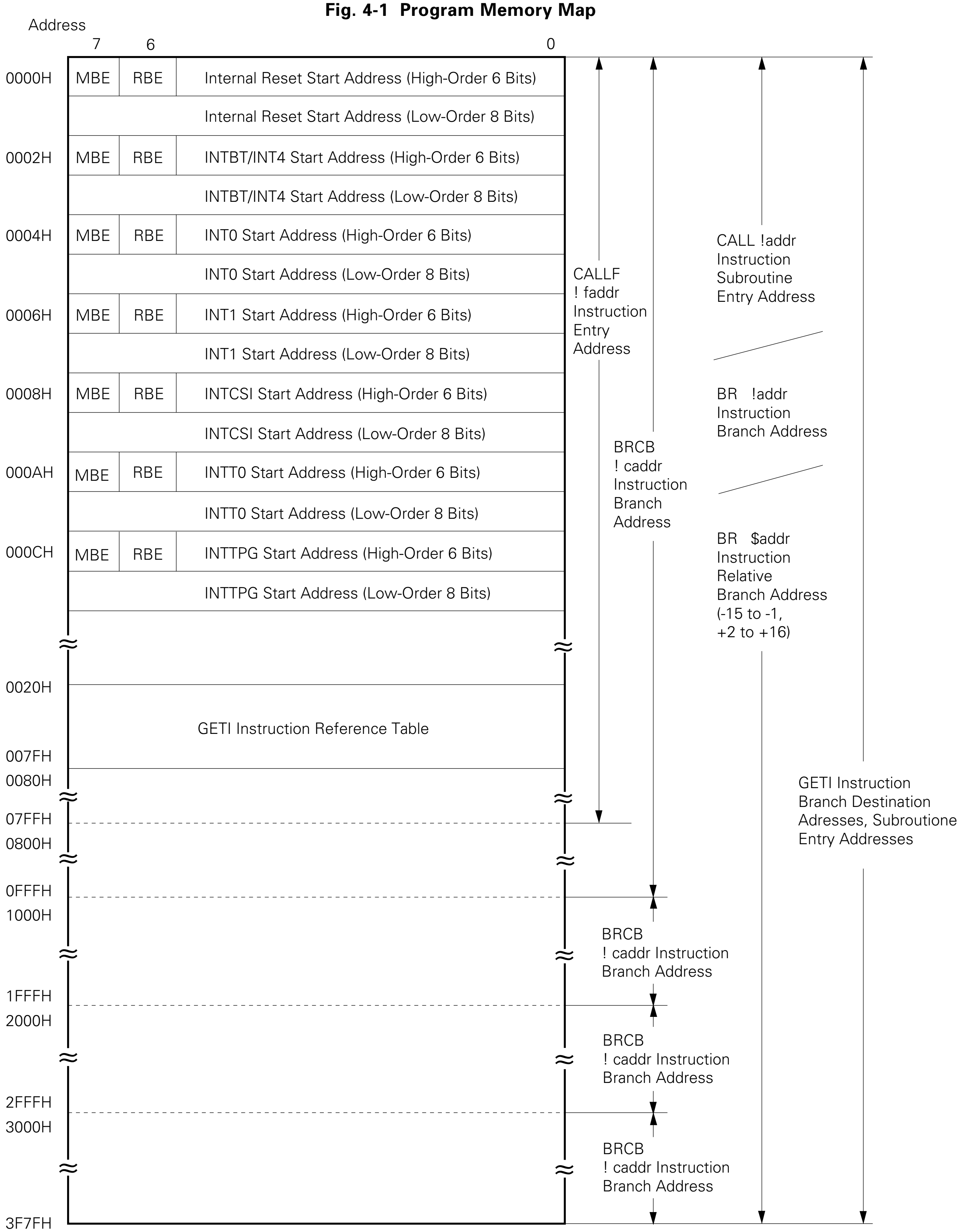
Note **When the subsystem clock is not used, operation is not affected if a feedback resistor is incorporated, but the supply current I_{DD} is increased.**

4. MEMORY CONFIGURATION

- Program memory (ROM) ... 16256 × 8 bits (0000H to 3F7FH)
  - 0000H to 0001H: Vector table in which reset-related program start adress is written.
  - 0002H to 000DH: Vector table in which interrupt-related program start addresses are written.
  - 0020H to 007FH: Table area referenced by the GETI instruction.

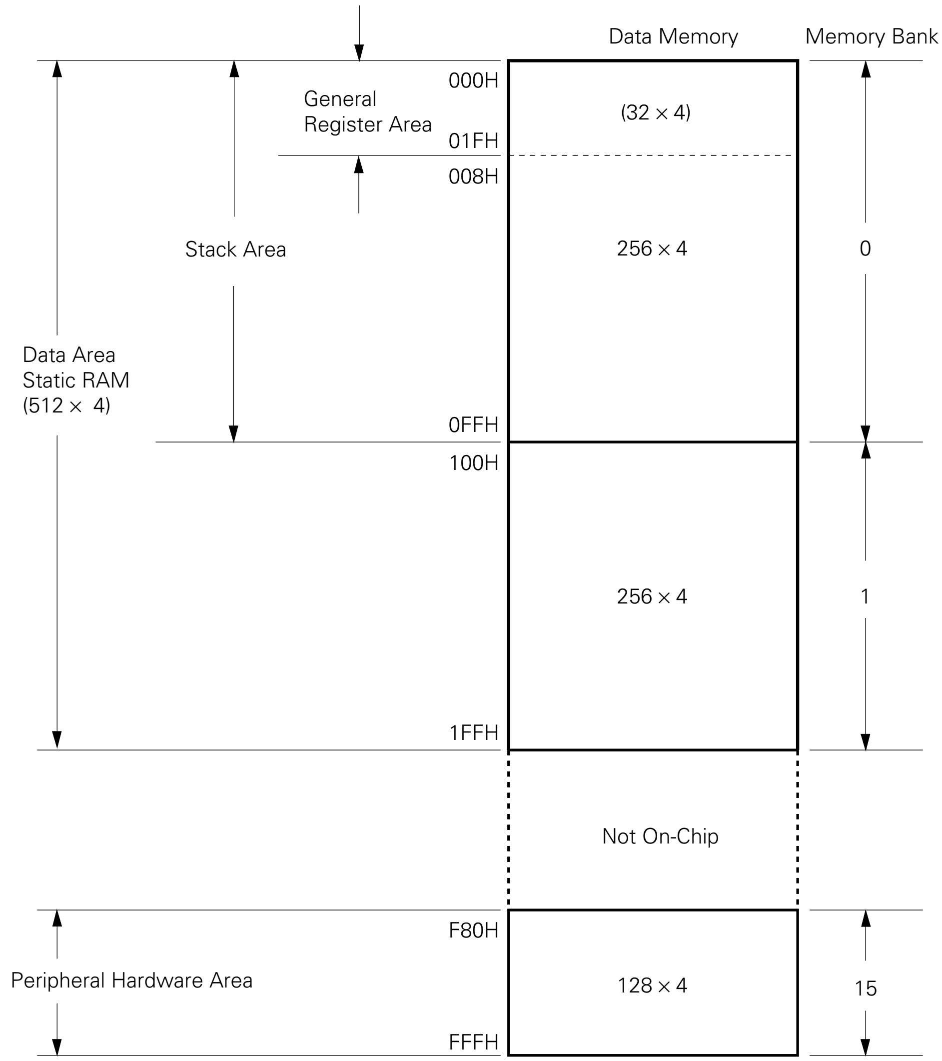
- Data memory
  - Data area ... 512 × 4 bits (000H to 1FFH)
  - Peripheral hardware area ... 128 × 4 bits (F80H to FFFH)

Fig. 4-1 Program Memory Map



Remarks In addition to the above, it is possible to branch to an address with the low-order 8 bits of the PC only changed by means of a BR PCDE or BR PCXA instruction.

Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

There are three kinds of I/O ports, as follows.

- CMOS input (PORT0, 1, 8, 15) : 16
- CMOS input/output (PORT2, 3, 6, 7, 9, 10, 11) : 28
- N-ch open drain (PORT4, 5, 12, 13, 14) : 20

Total 64

Fig. 5-1 Port Functions

<table>
<tr><th>Port (Pin Name)</th><th>Function</th><th colspan="2">Operation/Features</th><th>Remarks</th></tr>
<tr><td>PORT 0</td><td rowspan="2">4-bit input</td><td colspan="2" rowspan="2">Can always be read or tested regardless of the operating mode of the dual function pin.</td><td>Shares the use of the pin with INT4, $\overline{\text{SCK0}}$, SO0/SB0, SI0/SB1.</td></tr>
<tr><td>PORT 1</td><td>Shares the use of the pin with INT0 to INT2 and TI0.</td></tr>
<tr><td>PORT 2</td><td rowspan="2">4-bit input/output</td><td colspan="2">Can be set in the input or output mode as a 4-bit unit.</td><td>Shares the use of the pin with PTO0, PCL, BUZ</td></tr>
<tr><td>PORT 3</td><td colspan="2">Can be set in the input or the output mode in 1/4-bit units</td><td>—</td></tr>
<tr><td>PORT 4</td><td rowspan="2">4-bit input/output (N-ch open-drain 10 V withstand voltage)</td><td rowspan="2">Can be set in input or output mode in 4-bit units</td><td rowspan="2">With ports 4 and 5 as a pair, data can be input and output in 8-bit units.</td><td rowspan="2">With a mask option, the internal pull-up resistance can be specified in 1-bit units.</td></tr>
<tr><td>PORT 5</td></tr>
<tr><td>PORT 6</td><td rowspan="2">4-bit input/output</td><td>Can be set in input or output mode in 1/4-bit units</td><td rowspan="2">With ports 6 and 7 as a pair, data can be input and output in 8-bit units.</td><td>Shares the use of the pin with KR0 to KR3.</td></tr>
<tr><td>PORT 7</td><td>Can be set in input or output mode in 4-bit units</td><td>Shares the use of the pin with KR4 to KR7.</td></tr>
<tr><td>PORT 8</td><td>4-bit input</td><td colspan="2">Can always be read or tested regardless of the operating mode of the dual function pin.</td><td>Shares the use of the pin with PPO, $\overline{\text{SCK1}}$, SO1 and SI1.</td></tr>
<tr><td>PORT 9</td><td>4-bit input/output</td><td colspan="2">Can be set in input or output mode in 4-bit units.</td><td>With a mask option, the internal pull-up resistance can be specified in 1-bit units.</td></tr>
<tr><td>PORT 10</td><td rowspan="2">4-bit input/output</td><td colspan="2" rowspan="2">Can be set in input or output mode in 4-bit units.</td><td rowspan="2">—</td></tr>
<tr><td>PORT 11</td></tr>
<tr><td>PORT 12</td><td rowspan="3">4-bit input/output (N-ch open-drain 10 V withstand voltage)</td><td colspan="2" rowspan="3">Can be set in input or output mode in 4-bit units.</td><td rowspan="3">With a mask option, the internal pull-up resistance can be specified in 1-bit units.</td></tr>
<tr><td>PORT 13</td></tr>
<tr><td>PORT 14</td></tr>
<tr><td>PORT 15</td><td>4-bit input</td><td colspan="2">Can always be read or tested regardless of the operating mode of the dual function pin.</td><td>Shares the use of the pin with AN4 to AN7.</td></tr>
</table>

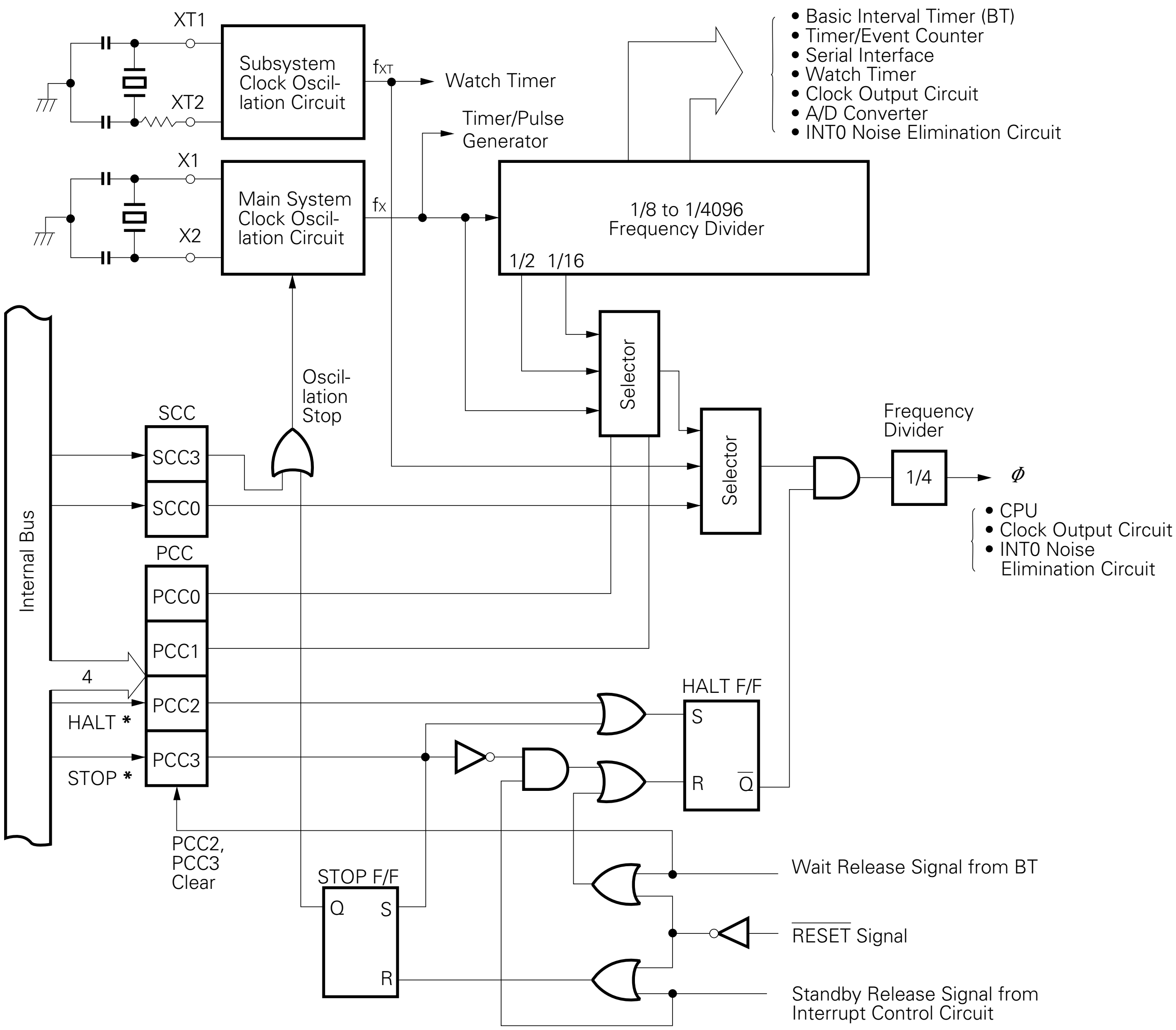
5.2 CLOCK GENERATOR

The operation of the clock generator is determined by the processor clock control register (PCC) and system clock control register (SCC).

There are two kinds of clock, the main system clock and subsystem clock, and the instruction execution time can be changed.

- 0.95 μs/1.91 μs/15.3 μs (4.19 MHz main system clock operation)
- 122 μs (32.768 kHz subsystem clock operation)

Fig. 5-1 Clock Generator Block Diagram



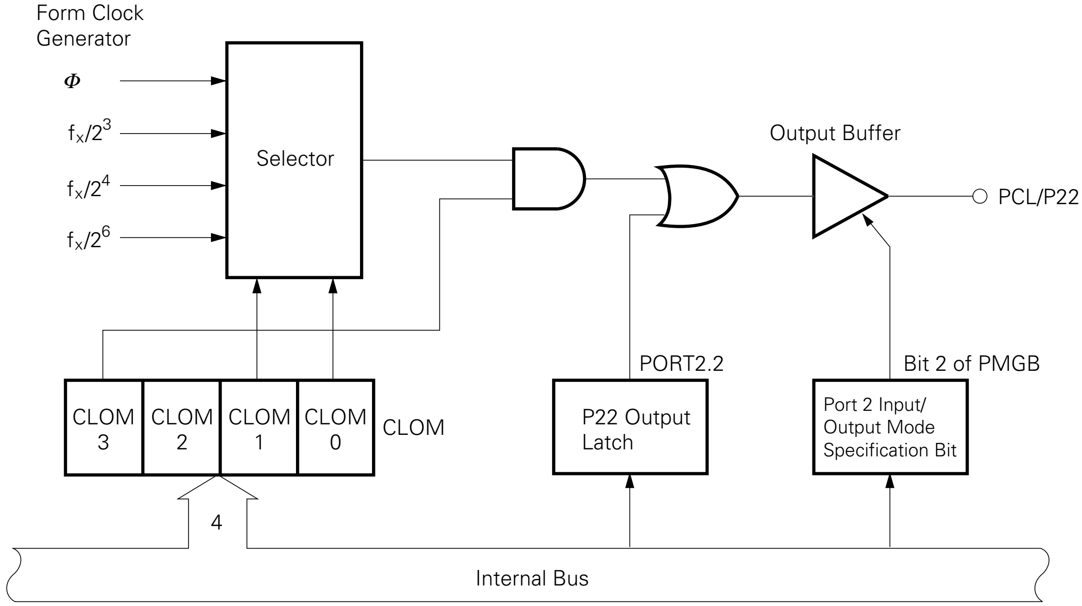
Remarks
1. fX = Main system clock frequency
2. fXT = Subsystem clock frequency
3. Φ = CPU clock
4. PCC: Processor clock control register
5. SCC: System clock control register
6. One Φ clock cycle (tCY) is one machine cycle. See **"AC CHARACTERISTICS"** in **11. "ELECTRICAL SPECIFICATIONS"** for details of tCY.

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit is a circuit which outputs a clock pulse from P22/PCL pin and is used to supply clock pulses to remote control outputs or peripheral LSI's.

- Clock output (PCL) : Φ, 524 kHz, 262 kHz, 65.5 kHz (at 4.19 MHz operation)

Fig. 5-2 Clock Output Circuit Configuration



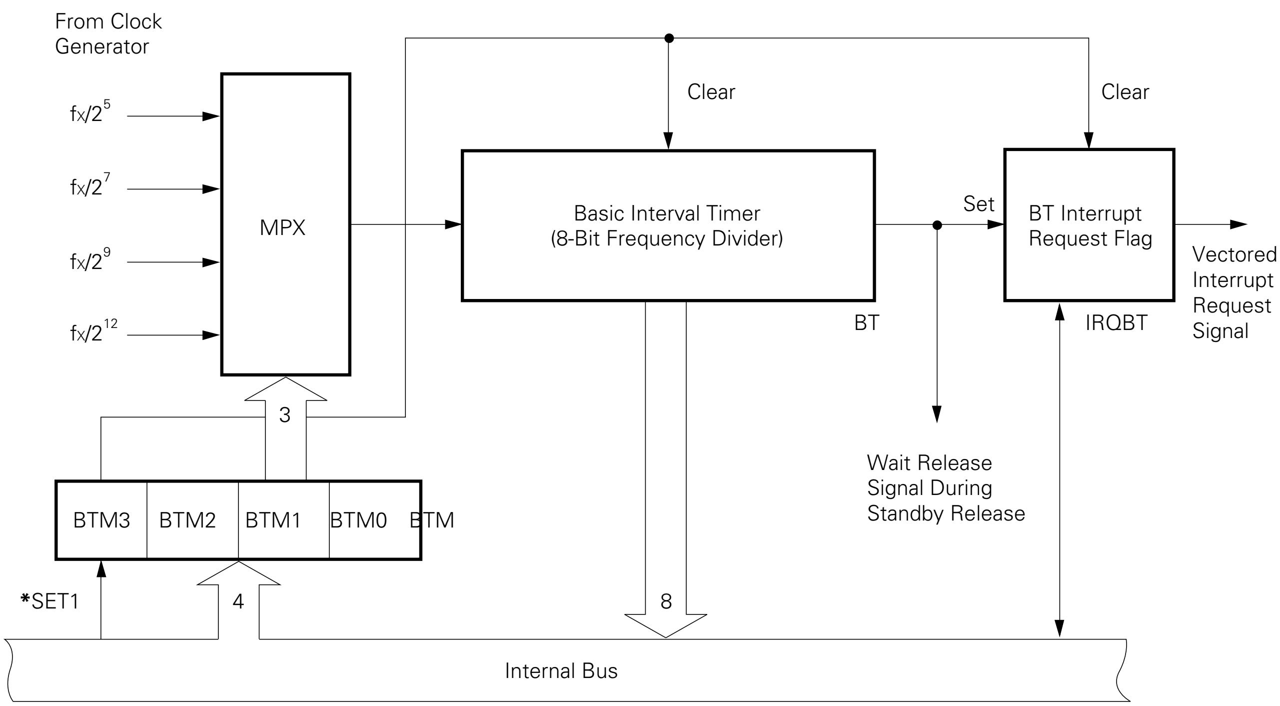
Remarks Consideration is given so that a low amplitude pulse is not output when switching between clock output enable and disable.

5.4 BASIC INTERVAL TIMER

The basic interval timer includes the following functions.

- It operates as an interval timer which generates reference time interrupts.
- It can be applied as a watchdog timer which detects when a program is out of control.
- Selects and counts wait times when the standby mode is released.
- It reads count contents.

Fig. 5-3 Basic Interval Timer Configuration



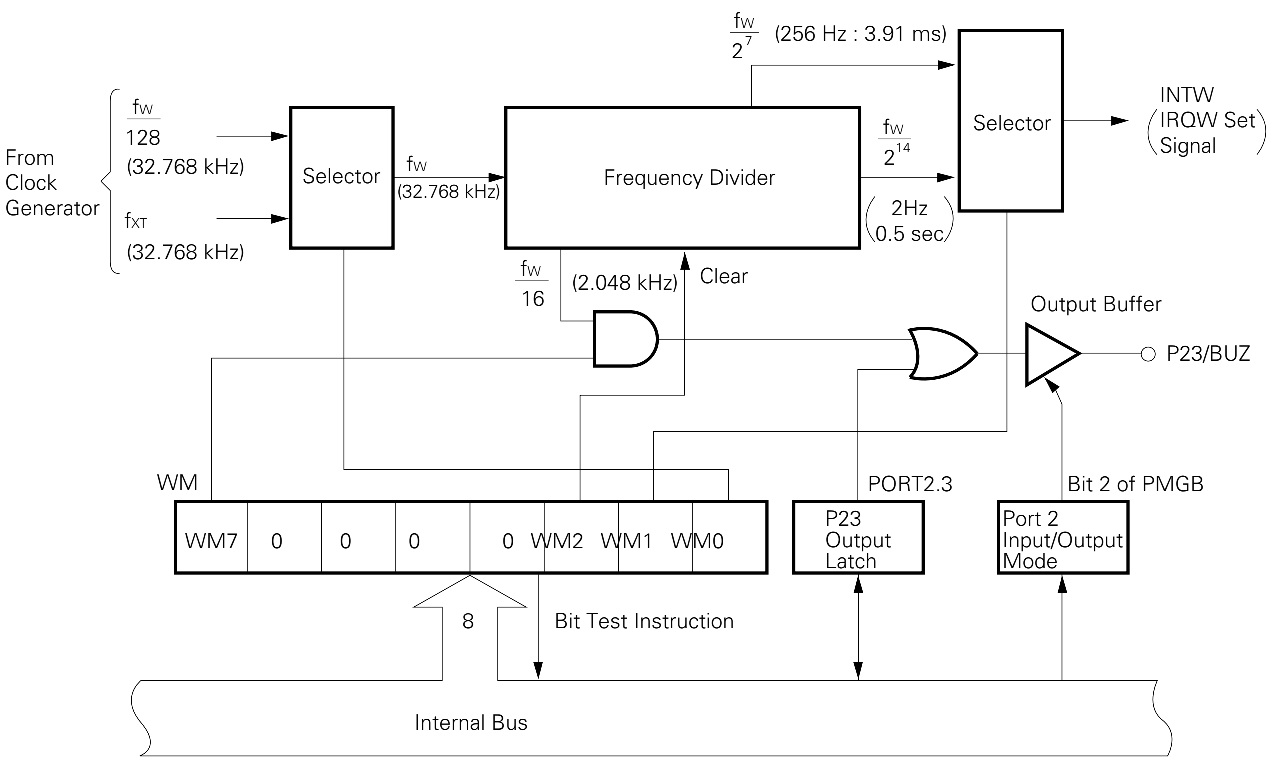
* Instruction execution.

5.5 WATCH TIMER

The μPD75516(A) incorporates a single watch timer channel. The watch timer has the following functions.

- Sets test flags (IRQW) at 0.5-second intervals. The standby mode can be released with IRQW.
- 0.5-sec. time intervals can be created in either the main system clock or the subsystem clock.
- In the fast watch mode, time intervals which are 128 times normal (3.91 ms) can be set, making this function convenient for program debugging and testing.
- A fixed frequency (2.048 kHz) can be output to the P23/BUZ pin for use in generating buzzer sounds and trimming system clock oscillation frequencies.
- The frequency divider can be cleared, so this clock can be started at 0 second.

Fig. 5-4 Watch Timer Block Diagram



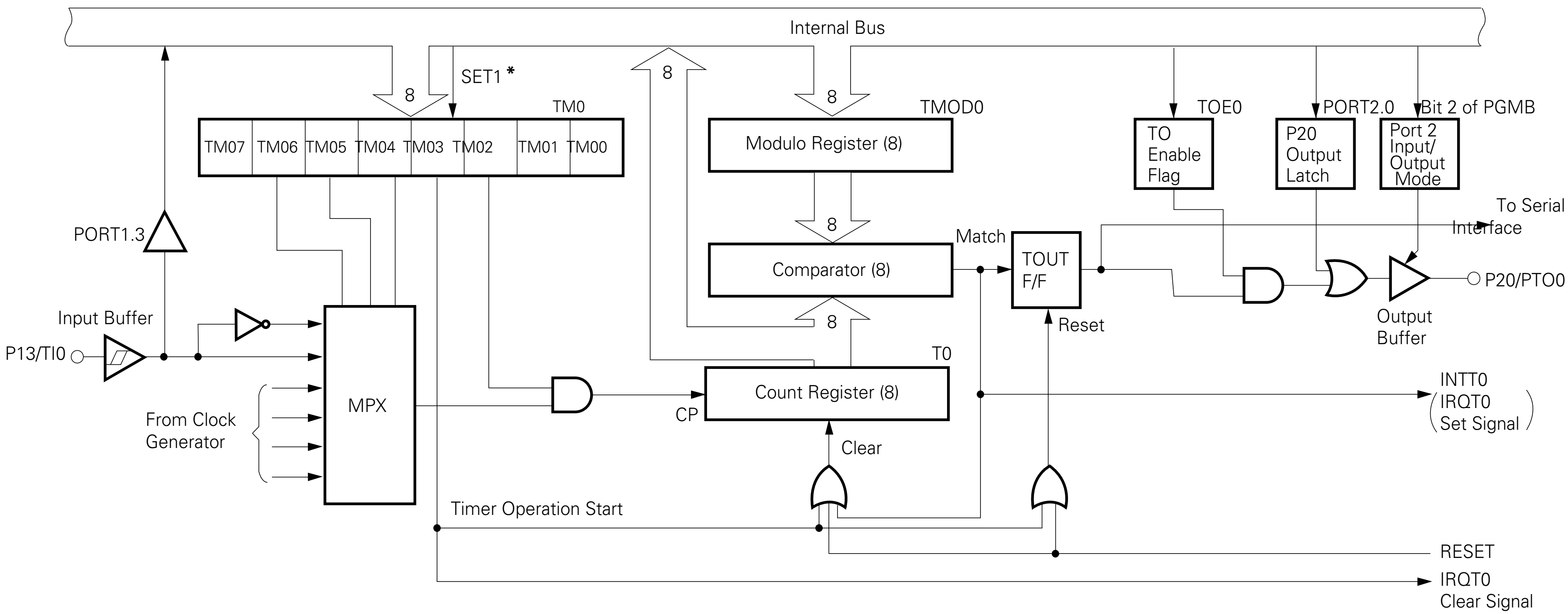
Remarks Values in parentheses are when f_X = 4.194304 MHz and f_{XT} = 32.768 kHz.

5.6 TIMER/EVENT COUNTER

The μPD75516(A) incorporates a single-channel timer/event counter. The timer/event counter has the following functions.

- Operates as a programmable interval timer.
- Outputs square waves in the desired frequency to the PTO0 pin.
- Operates as an event counter.
- Divides the TI0 pin input into N divisions and outputs it to the PTO0 pin (frequency divider operation).
- Supplies a serial shift clock to the serial interface circuit.
- Count status read function.

Fig. 5-5 Timer/Event Counter Block Diagram



* Instruction execution

5.7 TIMER/PULSE GENERATOR

The μPD75516(A) incorporates one channel of timer/pulse generator which can be used as a timer or a pulse generator. The timer/pulse generator has the following functions.

(a) Functions available in the timer mode

- 8-bit interval timer operation (IRQTPG generation) enabling the clock source to be varied at 5 levels
- Square wave output to PPO pin

(b) Functions available in the PWM pulse generate mode

- 14-bit accuracy PWM pulse output to the PPO pin (Used as a digital-to-analog converter and applicable to tuning)
- Interrupt generation of fixed time interval ($\frac{2^{15}}{f_X}$ = 7.81 ms : f_X = 4.19 MHz operation)

If pulse output is not necessary, the PPO pin can be used as a 1-bit output port.

Note If the STOP mode is set while the timer/pulse generator is in operation, miss-operation may result. To prevent that from occurring, preset the timer/pulse generator to the stop state using its mode register.

Fig. 5-6 Block Diagram of Timer/Pulse Generator (Timer Mode)

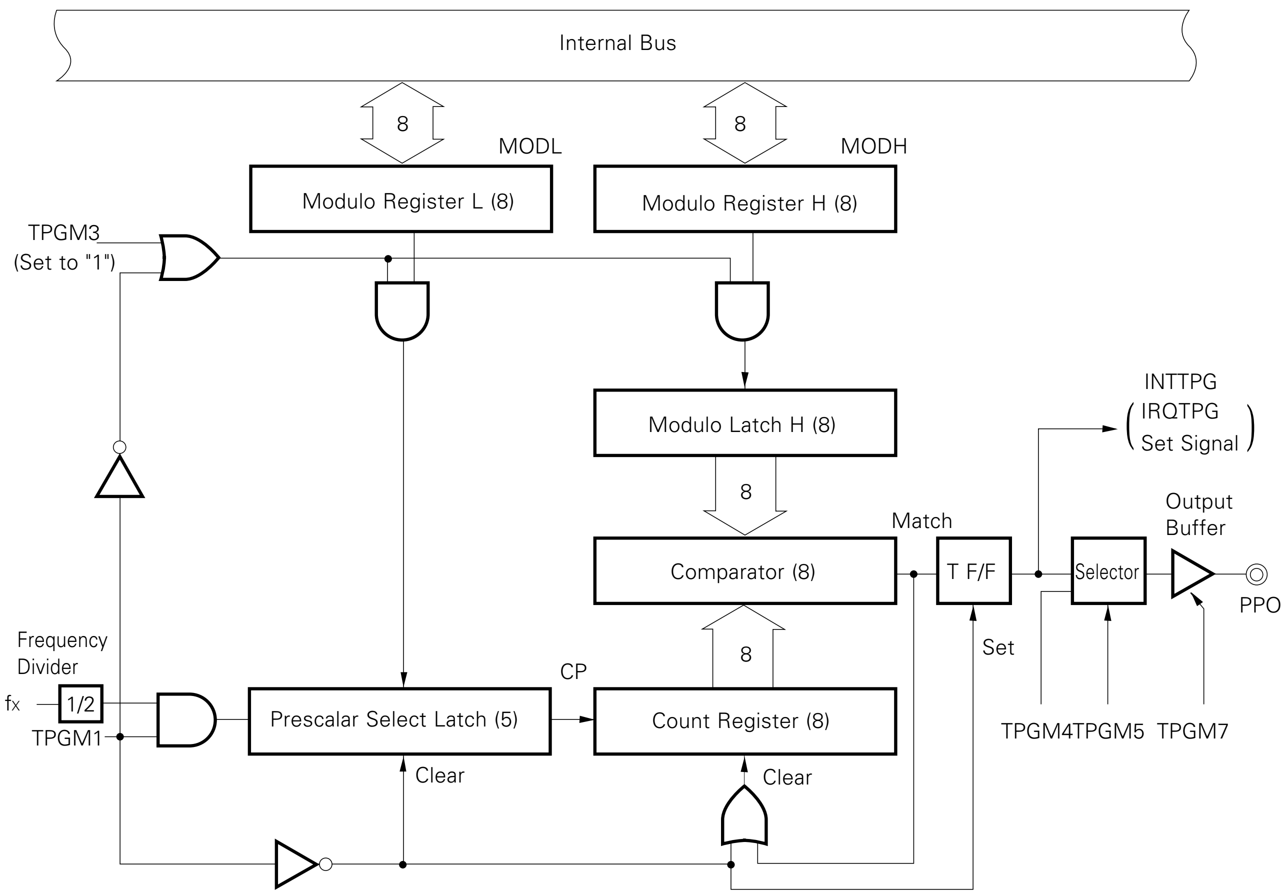
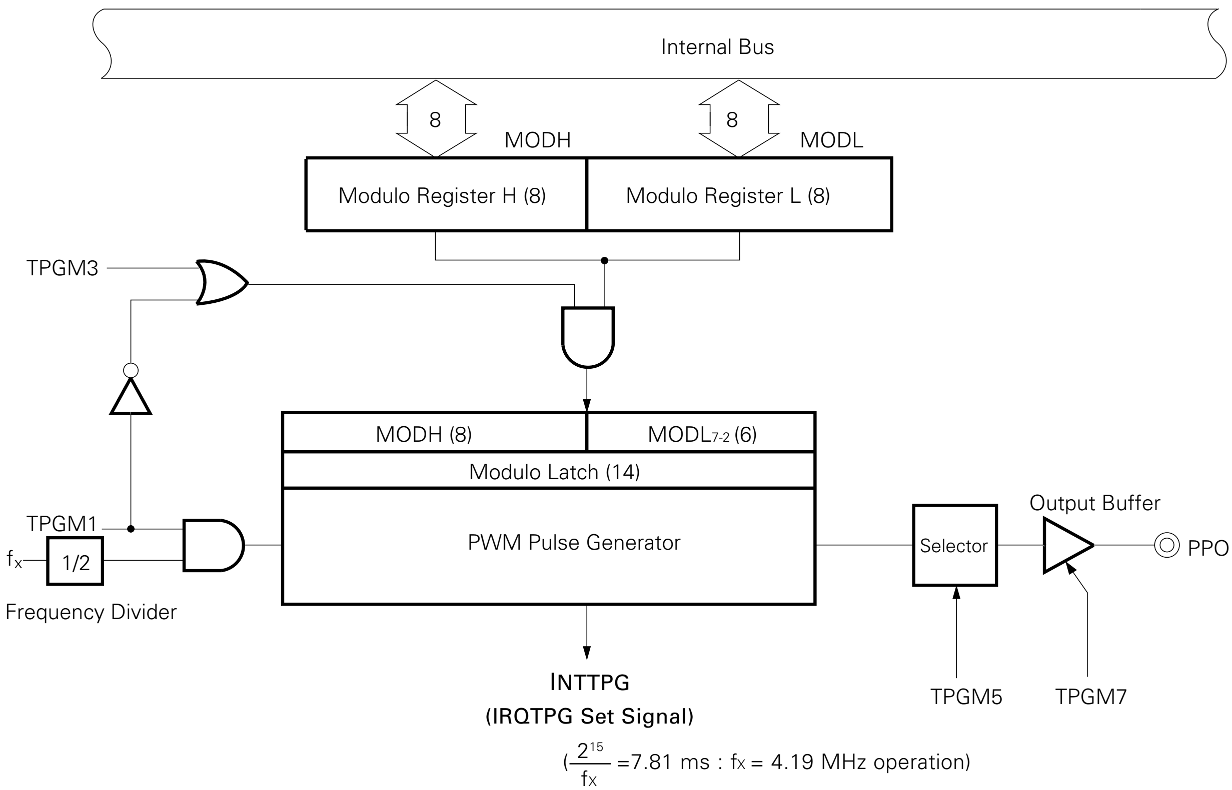


Fig. 5-7 Timer/Pulse Generator Block Diagram (PWM Pulse Generate Mode)



5.8 SERIAL INTERFACE

The μPD75516(A) has two serial interface channels on chip. The differences between channel 0 and channel 1 are shown in Table 5-2.

Table 5-2 Differences between Channels 0 and 1

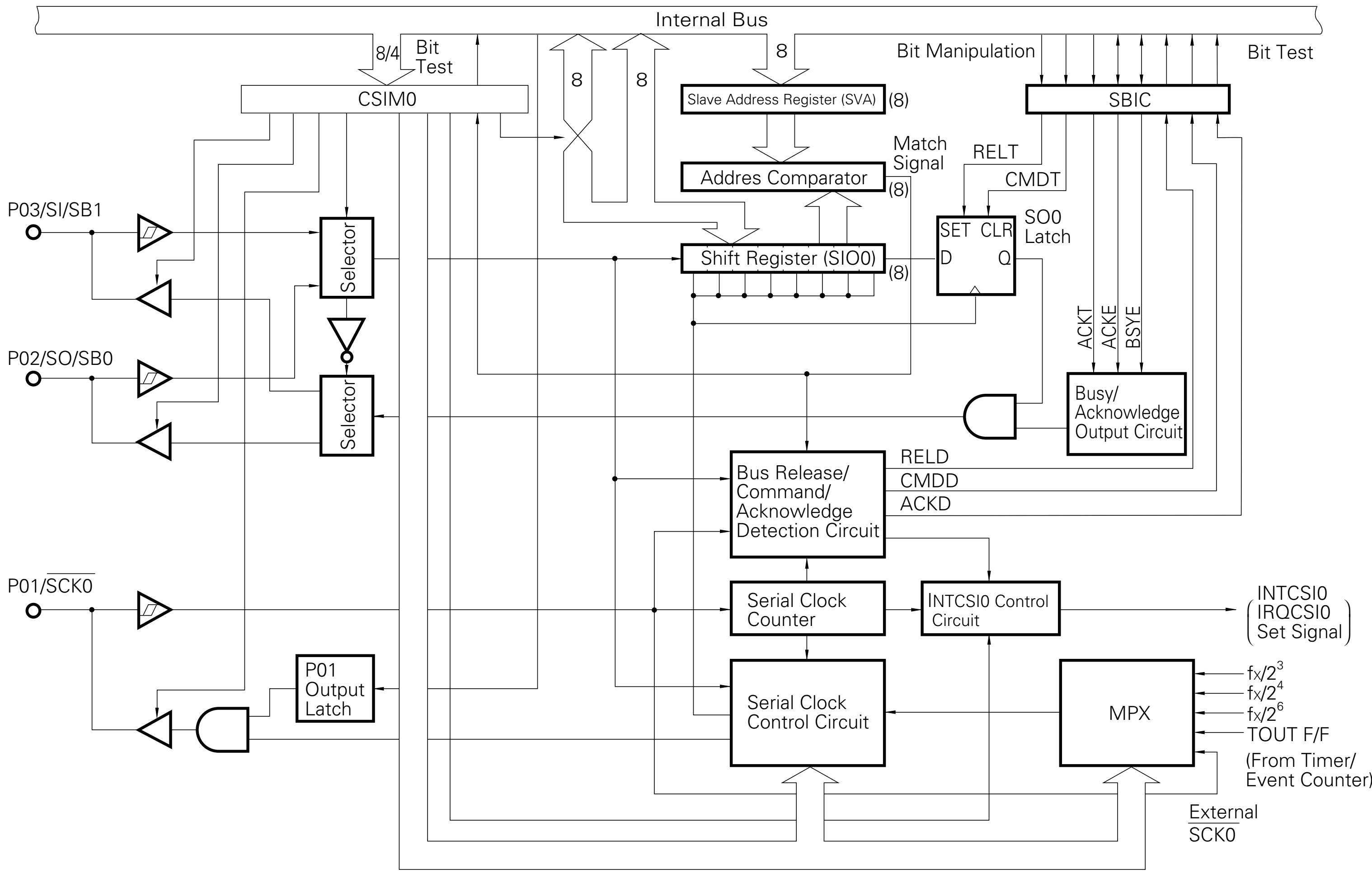
Serial Transfer Mode and Function		Channel 0	Channel 1
3-wire serial I/O	Clock selection	$f_X/2^4$, $f_X/2^3$, TOUT F/F, external clock	$f_X/2^4$, $f_X/2^3$, external clock
	Transfer mode	MSB first/LSB first switchable	MSB first
	Transfer end flag	Serial transfer end interrupt request flag (IRQCSI0)	Serial transfer end flag (EOT)
2-wire serial I/O		Use enabled	None
Serial bus interface (SBI)			

(1) Serial interface (channel 0)

The μPD75516(A) serial interface (channel 0) has the following four modes.

- Operation stop mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI mode (serial bus interface mode)

Fig. 5-8 Serial Interface (Channel 0) Block Diagram

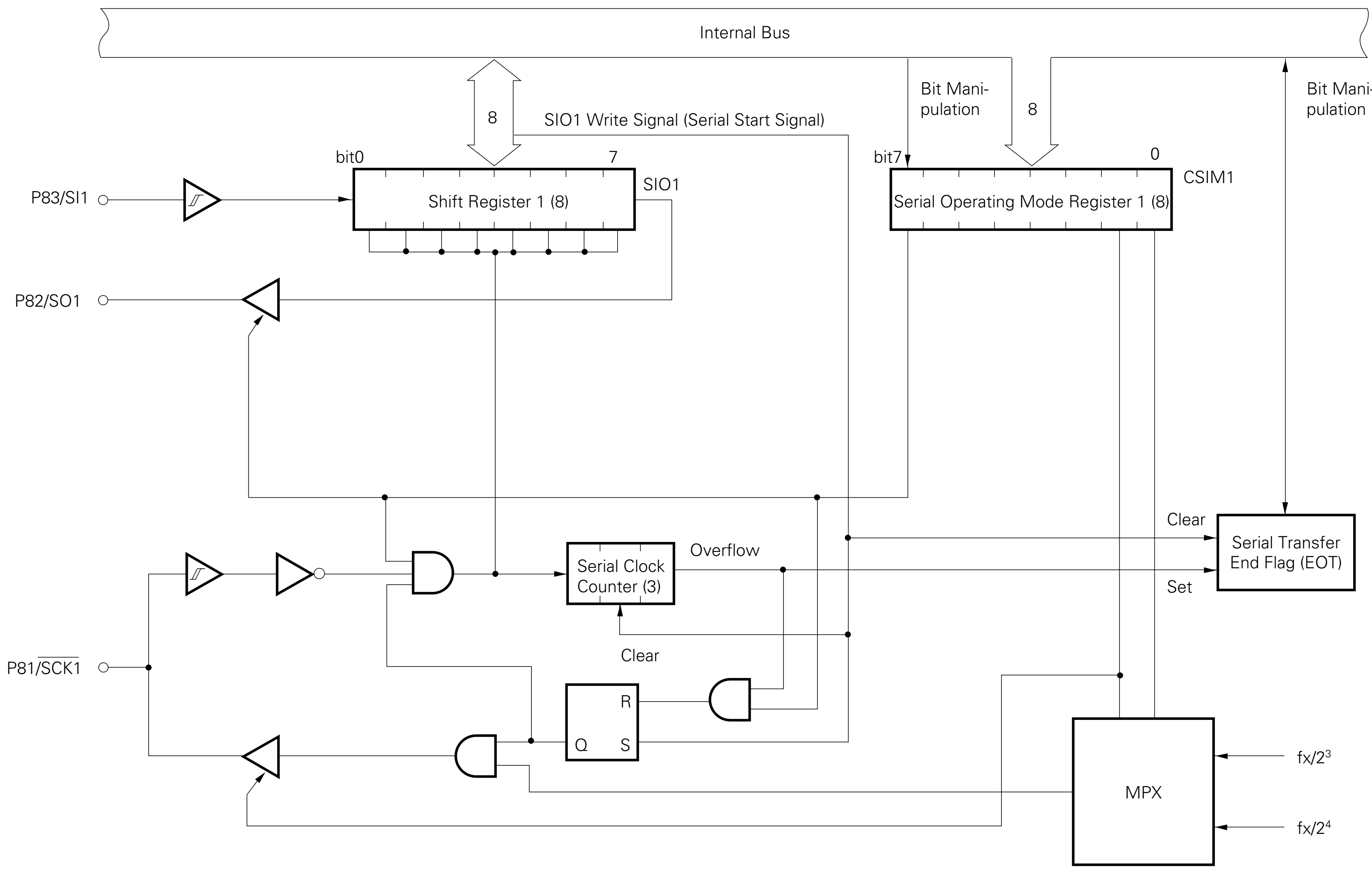


(2) Serial interface (channel 1)

The following two modes are available to the μPD75516(A) serial interface (channel 1).

- Operation stop mode
- 3-wire serial I/O mode

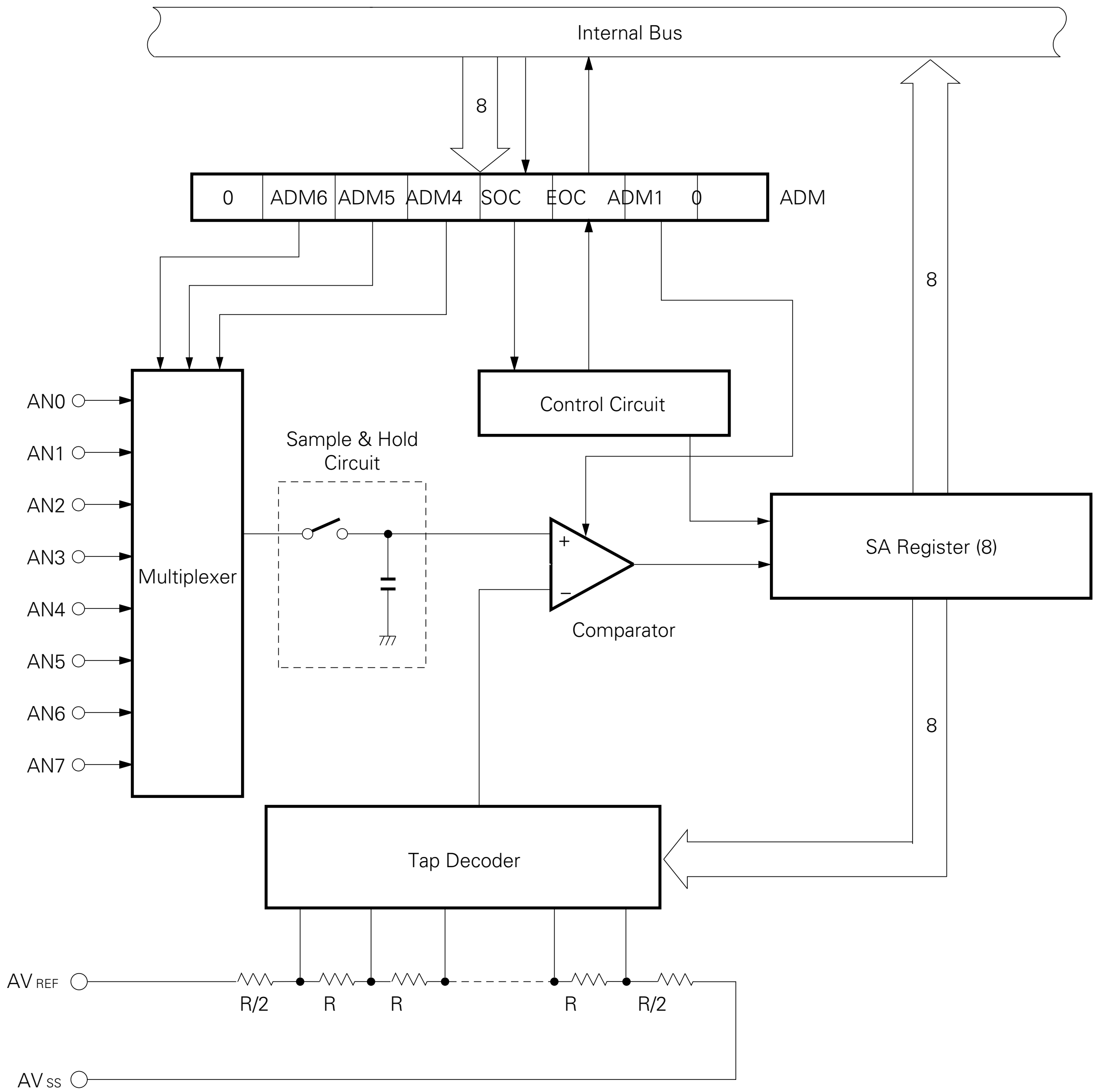
Fig. 5-9 Serial Interface (Channel 1) Block Diagram



5.9 A/D CONVERTER

The μPD75516(A) incorporates an 8-bit resolution A/D converter with 8-channel analog inputs (AN0 to AN7). The A/D converter employs successive approximation.

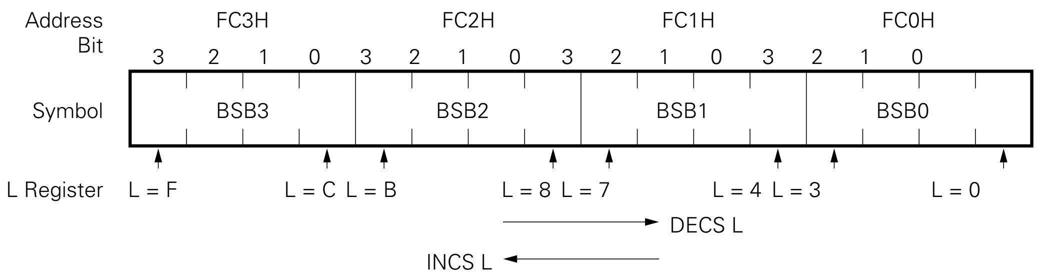
Fig. 5-10 A/D Converter Block Diagram



5.10 BIT SEQUENTIAL BUFFER : 16 BITS

The bit sequential buffer is a special data memory for bit manipulation. In particular it facilitates bit manipulation switch the address and bit specifications sequentially modified, and is thus useful for bit-wise processing of data comprising many bits.

Fig. 5-11 Bit Sequential Buffer Format



Remarks In pmem.@L addressing, the specified bit shifts in accordance with the L register.

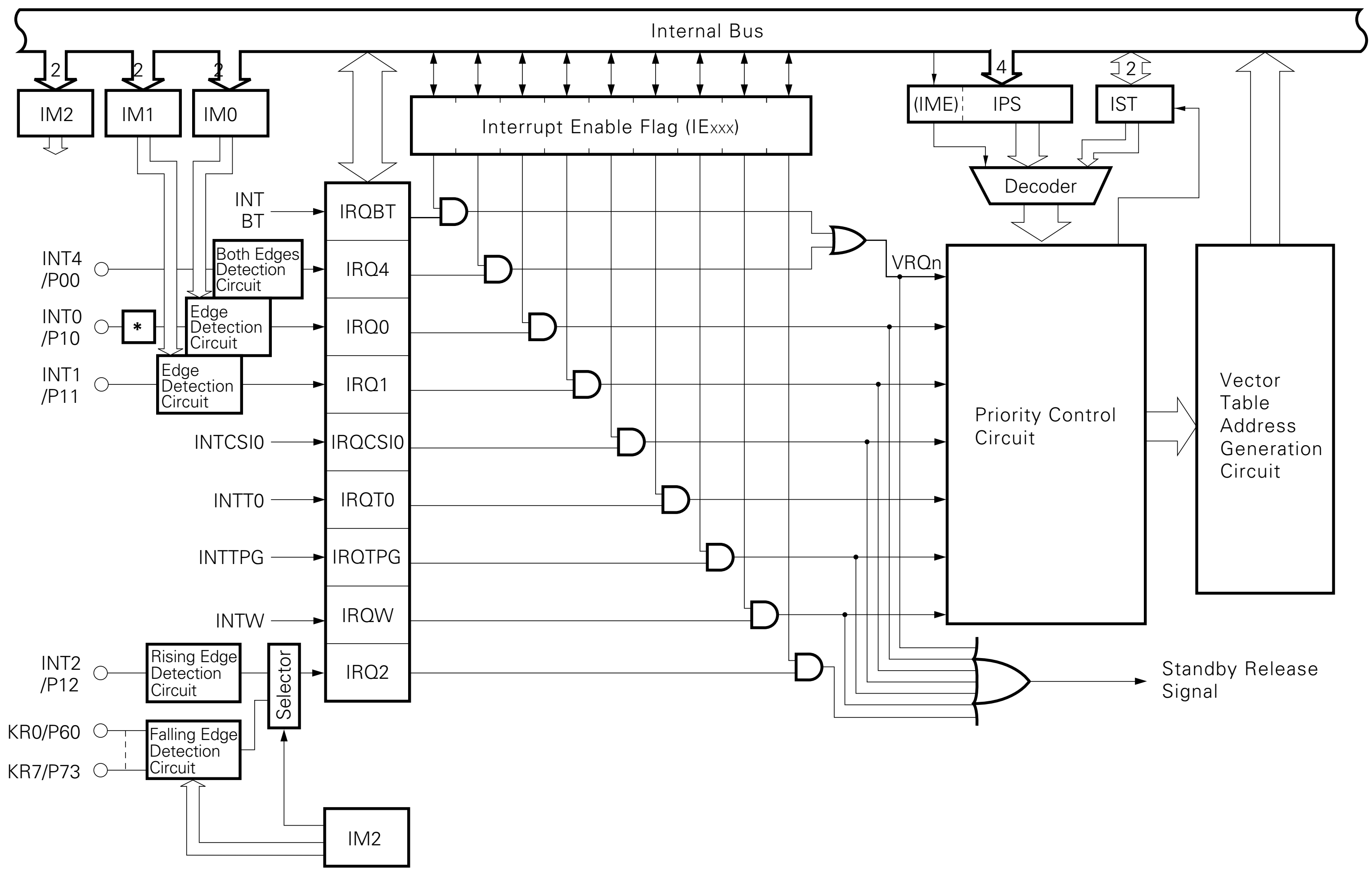
6. INTERRUPT FUNCTIONS

The μPD75516(A) has seven interrupt sources, and prioritized multiple interruption is possible. There are also two test sources, one of which, INT2, is provided with two edge-detected testable inputs.

The μPD75516(A) interrupt control circuit has the following functions.

- Hardware-controller vectored interrupt function which can control interrupt acknowledge with the interrupt enable flag (IE×××) and the interrupt master enable flag (IME).
- Function of setting any interrupt start address.
- Multiple interrupt function which can specify priority order with the interrupt priority select register (IPS).
- Interrupt request flag (IRQ×××) test function (Interrupt generation can be checked by software).
- Standby mode release function (Interrupt to be released by interrupt enable flag can be selected).

Fig. 6-1 Interrupt Control Circuit Block Diagram



* Noise Eliminator

7. STANDBY FUNCTIONS

Two standby modes (STOP mode and HALT mode) are available for the μPD75516(A) to decrease power consumption in the program standby mode.

Table 7-1 Operation Status in Standby Mode

<table>
<tr><th colspan="2"></th><th>STOP Mode</th><th>HALT Mode</th></tr>
<tr><td colspan="2">Set instruction</td><td>STOP instruction</td><td>HALT instruction</td></tr>
<tr><td colspan="2">System clock when set</td><td>Setting enabled only with main system clock.</td><td>Setting enabled with either main system clock or subsystem clock.</td></tr>
<tr><td rowspan="10">Operating state</td><td>Clock oscillator</td><td>Oscillator stops only with main system clock.</td><td>Stops only with CPU clock Φ (Oscillation continued).</td></tr>
<tr><td>Basic interval timer</td><td>Operation stopped.</td><td>Operation (IRQBT set at reference time intervals).</td></tr>
<tr><td>Serial interface (channel 0)</td><td>Operation enabled only when external $\overline{\text{SCK0}}$ input is selected for serial clock.</td><td>Operation enabled when the main system clock oscillates or with external $\overline{\text{SCK0}}$.</td></tr>
<tr><td>Serial interface (channel 1)</td><td>Operation enabled only when external $\overline{\text{SCK1}}$ input is selected for serial clock.</td><td>Operation enabled only when the main system clock oscillates.</td></tr>
<tr><td>Timer/event counter</td><td>Operation enabled only when TI0 pin input is specified for count clock.</td><td>Operation enabled only when the main system clock oscillates.</td></tr>
<tr><td>Watch timer</td><td>Operation enabled only f_{XT} is selected for count clock.</td><td>Operation enabled.</td></tr>
<tr><td>A/D converter</td><td>Operation stopped.</td><td>Operation enabled only when the main system clock oscillates.</td></tr>
<tr><td>Timer/pulse generator</td><td>Operation stopped.</td><td>Operation enabled only when the main system clock oscillates.</td></tr>
<tr><td>External interrupt</td><td colspan="2">INT1, 2, and 4 operation enabled.
INT0 operation disabled.</td></tr>
<tr><td>CPU</td><td colspan="2">Operation stopped.</td></tr>
<tr><td colspan="2">Release signal</td><td colspan="2">Interrupt request signal or $\overline{\text{RESET}}$ input from operational hardware enabled by interrupt enable flag.</td></tr>
</table>

8. RESET FUNCTIONS

The μPD75516(A) is reset and the hardware is initialized as shown in Table 8-1 by $\overline{\text{RESET}}$ input. The reset operation timing is shown in Fig. 8-1.

Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

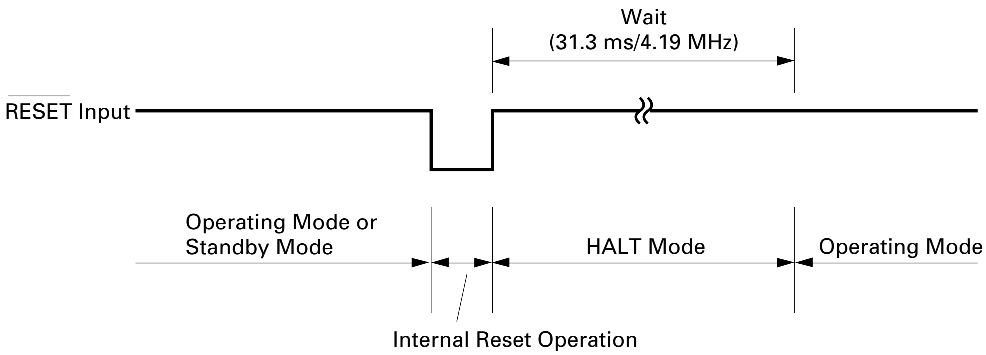


Table 8-1 Status of Each Hardware after Reset (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program counter (PC)		Low-order 6 bits of program memory address 0000H are set in PC13 to PC8 and the contents of address 0001H are set in PC7 to PC0.	Same as the left
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0, IST1)	0	0
	Bank enable flag (MBE, RBE)	Bit 6 of program memory address 0000H is set in RBE, and bit 7 is set in MBE.	Same as the left
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held*	Undefined
General register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank selection register (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Timer/pulse generator	Modulo register	Held	Held
	Mode register	0	0
Watch timer	Mode register (WM)	0	0

* Data of data memory addresses 0F8H to 0FDH becomes undefined by $\overline{\text{RESET}}$ input.

Table 8-1 Status of Each Hardware after Reset (2/2)

Hardware		RESET Input in Standby Mode	RESET Input during Operation
Serial interface (channel 0)	Shift register 0 (SIO0)	Held	Undefined
	Operating mode register 0 (CSIM0)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Held	Undefined
	P01/SCK0 output latch	1	1
A/D converter	Mode register (ADM), EOC	04H (EOC = 1)	04H (EOC = 1)
	SA register	7FH	7FH
Clock generator and clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Serial interface (channel 1)	Shift register (SIO1)	Held	Undefined
	Operating mode register 1 (CSIM1)	0	0
	Serial transfer end flag (EOT)	0	0
Interrupt function	Interrupt request flag (IRQ×××)	Reset (0)	Reset (0)
	Interrupt enable flag (IE×××)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0, 1, and 2 mode registers (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital port	Output buffer	Off	Off
	Output latch	Clear (0)	Clear (0)
	Input/output mode register (PMGA, B, C)	0	0
	Pull-up resistor specify register (POGA)	0	0
Bit sequential buffer (BSB0 to BSB3)		Held	Undefined

9. INSTRUCTION SET

(1) Operand identifier and description

Enter an operand in the operand column of each instruction using the description method relating to the operand identifier of the instruction (See the **RA75X Assembler Package User's Manual Language Volume (EEU-730)** for details). If more than one description method is available, select one. Capital alphabetic letters, plus and minus signs are keywords. Describe them as they are.

In the case of immediate data, describe appropriate numerical values or labels

Identifier	Description Method
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL-, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label* 2-bit immediate data or label
fmem pmem	FB0H to FBFH and FF0H to FFFH immediate data or labels FC0H to FFFH immediate data or labels
addr caddr faddr	0000H to 3F7FH immediate data or labels 12-bit immediate data or label 11-bit immediate data or label
taddr	20H to 7FH immediate data (bit0 = 0) or label
PORTn IE××× RBn MBn	PORT0 to PORT15 IEBT, IECSI0, IET0, IE0, IE1, IE2, IE4, IEW, IETPG RB0 to RB3 MB0, MB1, MB15

* For 8-bit data processing, only even addresses can be specified as mem.

(2) Legend for operation description

A	:	A register; 4-bit accumulator
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
X	:	X register
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
XA'	:	Expanded register pair (XA')
BC'	:	Expanded register pair (BC')
DE'	:	Expanded register pair (DE')
HL'	:	Expanded register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; Bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 to 15)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority select register
IE×××	:	Interrupt enable flag
RBS	:	Register bank select register
MBS	:	Memory bank select register
PCC	:	Processor clock control register
.	:	Address and bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Description of symbols in the addressing area column

*1	MB = MBE • MBS (MBS = 0, 1, 15)	Data Memory Addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H to 7FH) MB = 15 (80H to FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 3F7FH	Program Memory Addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1, (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H to 0FFFH ($PC_{13, 12}$ = 00B) or 1000H to 1FFFH ($PC_{13, 12}$ = 01B) or 2000H to 2FFFH ($PC_{13, 12}$ = 10B) or 3000H to 3F7FH ($PC_{13, 12}$ = 11B)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	

Remarks **1.** MB indicates accessible memory bank.
2. In *2, MB = 0 irrespective of MBE and MBS.
3. In *4 and *5, MB = 15 irrespective of MBE and MBS.
4. *6 to *10 indicate addressable areas.

(4) Description of the machine cycle column

S indicates the number of machine cycles required for skip operation by an instruction having skip function. The S value varies as follows:

- When not skipped .... S = 0
- When 1-byte or 2-byte instructions are skipped .... S = 1
- When 3-byte instructions are skipped (BR !adder, CALL !adder instruction) ... S = 2

Note GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle of CPU clock Φ (=t_{CY}) and three time periods are available according to PCC setting.

Note 1	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A←n4		Stack A
		reg1, #n4	2	2	reg1←n4		
		XA, #n8	2	2	XA←n8		Stack A
		HL, #n8	2	2	HL←n8		Stack B
		rp2, #n8	2	2	rp2←n8		
		A, @HL	1	1	A←(HL)	*1	
		A, @HL+	1	2 + S	A←(HL), then L←L+1	*1	L = 0
		A, @HL–	1	2 + S	A←(HL), then L←L–1	*1	L = FH
		A, @rpa1	1	1	A←(rpa1)	*2	
		XA, @HL	2	2	XA←(HL)	*1	
		@HL, A	1	1	(HL)←A	*1	
		@HL, XA	2	2	(HL)←XA	*1	
		A, mem	2	2	A←(mem)	*3	
		XA, mem	2	2	XA←(mem)	*3	
		mem, A	2	2	(mem)←A	*3	
		mem, XA	2	2	(mem)←XA	*3	
		A, reg	2	2	A←reg		
		XA, rp'	2	2	XA←rp'		
		reg1, A	2	2	reg1←A		
		rp'1, XA	2	2	rp'1←XA		
	XCH	A, @HL	1	1	A↔(HL)	*1	
		A, @HL+	1	2 + S	A↔(HL), then L←L+1	*1	L = 0
		A, @HL–	1	2 + S	A↔(HL), then L←L–1	*1	L = FH
		A, @rpa1	1	1	A↔(rpa1)	*2	
		XA, @HL	2	2	XA↔(HL)	*1	
		A, mem	2	2	A↔(mem)	*3	
		XA, mem	2	2	XA↔(mem)	*3	
		A, reg1	1	1	A↔reg1		
		XA, rp'	2	2	XA↔rp'		
Note 2	MOVT	XA, @PCDE	1	3	XA←$(PC_{13-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA←$(PC_{13-8}+XA)_{ROM}$		

Note **1.** Instruction Group
2. Table reference

Note	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY←(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY←(H+mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit)←CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))←CY	*5	
		@H+mem.bit, CY	2	2	(H+mem_{3-0}.bit)←CY	*1	
Operation	ADDS	A, #n4	1	1 + S	A←A+n4		carry
		XA, #n8	2	2 + S	XA←XA+n8		carry
		A, @HL	1	1 + S	A←A+(HL)	*1	carry
		XA, rp'	2	2 + S	XA←XA+rp'		carry
		rp'1, XA	2	2 + S	rp'1←rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY←A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY←XA+rp'+CY		
		rp'1, XA	2	2	rp'1, CY←rp'1+XA+CY		
	SUBS	A, @HL	1	1 + S	A←A–(HL)	*1	borrow
		XA, rp'	2	2 + S	XA←XA–rp'		borrow
		rp'1, XA	2	2 + S	rp'1←rp'1–XA		borrow
	SUBC	A, @HL	1	1	A, CY←A–(HL)–CY	*1	
		XA, rp'	2	2	XA, CY←XA–rp'–CY		
		rp'1, XA	2	2	rp'1, CY←rp'1–XA–CY		
	AND	A, #n4	2	2	A←A∧n4		
		A, @HL	1	1	A←A∧(HL)	*1	
		XA, rp'	2	2	XA←XA∧rp'		
		rp'1, XA	2	2	rp'1←rp'1∧XA		
	OR	A, #n4	2	2	A←A∨n4		
		A, @HL	1	1	A←A∨(HL)	*1	
		XA, rp'	2	2	XA←XA∨rp'		
		rp'1, XA	2	2	rp'1←rp'1∨XA		
	XOR	A, #n4	2	2	A←A⊻n4		
		A, @HL	1	1	A←A⊻(HL)	*1	
		XA, rp'	2	2	XA←XA⊻rp'		
		rp'1, XA	2	2	rp'1←rp'1⊻XA		

Note Instruction Group

Note 1	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Note 2	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/decrement	INCS	reg	1	1 + S	reg←reg+1		reg = 0
		rp1	1	1 + S	rp1←rp1+1		rp1 = 00H
		@HL	2	2 + S	(HL)←(HL)+1	*1	(HL) = 0
		mem	2	2 + S	(mem)←(mem)+1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg←reg–1		reg = FH
		rp'	2	2 + S	rp'←rp'–1		rp' = FFH
Compare	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	CY←1		
	CLR1	CY	1	1	CY←0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Note **1.** Instruction Group

2. Accumulator manipulation

Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit)←1	*3	
		fmem.bit	2	2	(fmem.bit)←1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←1	*5	
		@H + mem.bit	2	2	(H+mem$_{3-0}$.bit)←1	*1	
	CLR1	mem.bit	2	2	(mem.bit)←0	*3	
		fmem.bit	2	2	(fmem.bit)←0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit)←0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY←CY∧(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∧(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY∧(H+mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY←CY∨(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∨(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY∨(H+mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY←CY⊻(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY⊻(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY⊻(H+mem$_{3-0}$.bit)	*1	
Branch	BR	addr	—	—	PC$_{13-0}$←addr (Optimum instruction is selected from among BR !addr, BRCB !caddr and BR $addr by an assembler.)	*6	
		!addr	3	3	PC$_{13-0}$←addr	*6	
		$addr	1	2	PC$_{13-0}$←addr	*7	
	BRCB	!caddr	2	2	PC$_{13-0}$←PC$_{13,12}$+caddr$_{11-0}$	*8	
	BR	PCDE	2	3	PC$_{13-0}$←PC$_{13-8}$+DE		
		PCXA	2	3	PC$_{13-0}$←PC$_{13-8}$+XA		

Note Instruction Group

Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALL	!addr	3	3	(SP–4) (SP–1) (SP–2)←PC_{11-0} (SP–3)← MBE, RBE, $PC_{13, 12}$ PC_{13-0}←addr, SP←SP–4	*6	
	CALLF	!faddr	2	2	(SP–4) (SP–1) (SP–2)←PC_{11-0} (SP–3)← MBE, RBE, $PC_{13, 12}$ PC_{13-0}←00, faddr, SP←SP–4	*9	
	RET		1	3	MBE, RBE, $PC_{13, 12}$←(SP+1) PC_{11-0}←(SP) (SP+3) (SP+2) SP←SP+4		
	RETS		1	3 + S	MBE, RBE, $PC_{13, 12}$←(SP+1) PC_{11-0}←(SP) (SP+3) (SP+2) SP←SP+4 then skip unconditionally		Unconditional
	RETI		1	3	$PC_{13, 12}$←(SP+1) PC_{11-0}←(SP) (SP+3) (SP+2) PSW←(SP+4) (SP+5), SP←SP+6		
	PUSH	rp	1	1	(SP–1) (SP–2)←rp, SP←SP–2		
		BS	2	2	(SP–1)←MBS, (SP–2)←RBS, SP←SP–2		
	POP	rp	1	1	rp←(SP+1) (SP), SP←SP+2		
		BS	2	2	MBS←(SP+1), RBS←(SP), SP←SP+2		
Interrupt control	EI		2	2	IME(IPS.3)←1		
		IE×××	2	2	IE×××←1		
	DI		2	2	IME(IPS.3)←0		
		IE×××	2	2	IE×××←0		
Input/output	IN *	A, PORTn	2	2	A←PORTn (n = 0 to 15)		
		XA, PORTn	2	2	XA←PORTn+1, PORTn (n = 4, 6)		
	OUT *	PORTn, A	2	2	PORTn←A (n = 2 to 7, 9 to 14)		
		PORTn, XA	2	2	PORTn+1, PORTn←XA (n = 4, 6)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2←1)		
	STOP		2	2	Set STOP Mode (PCC.3←1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS←n (n = 0 to 3)		
		MBn	2	2	MBS←n (n = 0, 1, 15)		

* MBE = 0 or MBE = 1 and MBE = 15 must be set for execution of IN/OUT instruction

Note Instruction Group

<table>
<tr><th>Note</th><th>Mnemonic</th><th>Operands</th><th>No. of Bytes</th><th>Machine Cycle</th><th>Operation</th><th>Addressing Area</th><th>Skip Condition</th></tr>
<tr><td rowspan="3">Special</td><td rowspan="3">GET1 *</td><td rowspan="3">taddr</td><td rowspan="3">1</td><td rowspan="3">3</td><td>• TBR instruction
$PC_{13-0} \leftarrow (taddr)_{4-0} + (taddr+1)$</td><td rowspan="3">*10</td><td></td></tr>
<tr><td>• TCALL instruction
$(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$
$(SP-3) \leftarrow$ MBE, RBE, $PC_{13, 12}$
$PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr+1)$
$SP \leftarrow SP-4$</td><td></td></tr>
<tr><td>• (taddr) (taddr+1) instruction executed in the case of instruction except TBR and TCALL instructions</td><td>Depends on instructions referred to.</td></tr>
</table>

* TBR and TCALL instructions are assembled pseudo-instructions to define the GETI instruction table.

Note Instruction Group

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Power supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_{I1}	Except ports 4, 5 and 12 to 14		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5 and 12 to 14	Internal pull-up resistor	–0.3 to V_{DD} +0.3	V
			Open-drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}*	1 pin	Peak value	–10	mA
			Effective value	–5	mA
		All pins	Peak value	–30	mA
			Effective value	–15	mA
Output current low	V_{OL}*	1 pin	Peak value	10	mA
			Effective value	5	mA
		Total of ports 0, 2, 3 and 4	Peak value	100	mA
			Effective value	60	mA
		Total of ports 5 to 11	Peak value	100	mA
			Effective value	60	mA
		Total of ports 12 to 14	Peak value	40	mA
			Effective value	25	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

* Calculate the effective value with the formula [Effective value] = [Peak value] $\times \sqrt{duty}$.

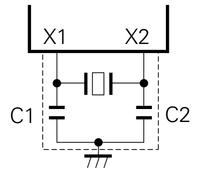
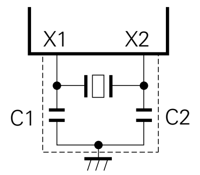
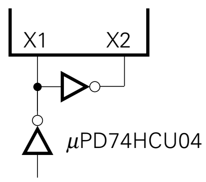
OPERATING VOLTAGE

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
A/D converter	Power supply voltage	V_{DD}		3.5	6.0	V
	Ambient temperature	Ta		–40	+85	°C
Timer/pulse generator	Power supply voltage	V_{DD}		4.5	6.0	V
	Ambient temperature	Ta		–40	+85	°C
Other circuits	Power supply voltage	V_{DD}		2.7	6.0	V
	Ambient temperature	Ta		–40	+85	°C

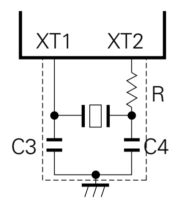
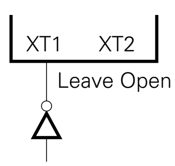
CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f = 1 MHz Unmeasured pin returned to 0 V			15	pF
Output capacitance	C_O				15	pF
Input/output capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_X) *1	V_{DD} = Oscillation voltage range	1.0		5.0*3	MHz
		Oscillation stabilization time *2	After V_{DD} reaches the minimum value in the oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (f_X) *1		1.0	4.19	5.0*3	MHz
		Oscillation stabilization time *2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) *1		1.0		5.0*3	MHz
		X1 high and low level widths (t_{XH}, t_{XL})		100		500	ns

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT}) *1		32	32.768	35	kHz
		Oscillation stabilization time *2	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) *1		32		100	kHz
		XT1 high and low level widths (t_{XTH}, t_{XTL})		5		15	μs

* **1.** Oscillator characteristics only. Refer to the description of AC characteristics for instruction execution time.

2. Time required for oscillation to become stabilized after V_{DD} application or STOP mode release.

★ **3.** When the oscillator frequency is 4.19 MHz < fX ≤ 5.0 MHz, PPC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, one machine cycle is less than 0.95 μs, and the specification MIN. value of 0.95 μs will not be achieved.

Note When the main system clock and subsystem clock oscillators are used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc. ★

- The wiring should be kept as short as possible.
- No other signal lines should be crossed. Keep away from lines carrying a high fluctuating current.
- The oscillator capacitor grounding point should be at the same potential as V_{DD}. Do not ground to a ground pattern carrying a high current.
- A signal should not be taken from the oscillator.

The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

DC CHARACTERISTICS (Ta = –40 to 85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2, 3, 9 to 11, P80, P82		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, 15, P81, P83, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Port 4, 5, 12 to 14	Internal pull-up resistor	0.7 V_{DD}		V_{DD}	V
			Open-drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD}–0.5		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2 to 5, 9 to 14, P80, P82		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, 15, P81, P83, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
Output voltage high	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = –100 µA		V_{DD}–0.5			V
Output voltage low	V_{OL}	Ports 3, 4, 5	V_{DD} = 4.5 to 6.0V, I_{OL} = 5 mA		0.2	1.0	V
		V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 µA				0.5	V
		SB0, 1	Open-drain pull-up resistance ≥ 1 kΩ			0.2 V_{DD}	V
Input leakage current high	I_{LIH1}	V_I = V_{DD}	Except below			3	µA
	I_{LIH2}		X1, X2, XT1			20	µA
	I_{LIH3}	V_I = 9 V	Ports 4, 5, 12 to 14 (when open-drain)			20	µA
Input leakage current low	I_{LIL1}	V_I = 0 V	Except below			–3	µA
	I_{LIL2}		X1, X2, XT1			–20	µA
Output leakage current high	I_{LOH1}	V_O = V_{DD}	Except below			3	µA
	I_{LOH2}	V_O = 9 V	Ports 4, 5, 12 to 14 (when open-drain)			20	µA
Output leakage current low	I_{LOL}	V_O = 0 V				–3	µA
Internal pull-up resistor	R_{U1}	Ports 0, 1, 2, 3, 6, 7 (except P00) V_I = 0 V	V_{DD} = 5.0 V ±10%	15	40	80	kΩ
			V_{DD} = 3.0 V ± 10%	30		300	kΩ
	R_{U2}	Ports 4, 5, 12 to 14 V_O = V_{DD} –2.0 V	V_{DD} = 5.0 V ± 10%	15	40	70	kΩ
			V_{DD} = 3.0 V ± 10%	10		60	kΩ
Internal pull-down resistor	R_D	V_O = 2 V	Port 9	20	70	140	kΩ

DC CHARACTERISTICS (Ta = –40 to 85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Supply current ***1**	I_{DD1}	4.19 MHz***2** crystal oscillation C1 = C2 = 22 pF	Operating mode	V_{DD} = 5 V ± 10% ***3**		3	9	mA
				V_{DD} = 3 V ± 10% ***4**		0.55	1.5	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ± 10%		600	1800	μA
				V_{DD} = 3 V ± 10%		200	600	μA
	I_{DD3}	32.768 kHz***5** crystal oscillation	Operating mode	V_{DD} = 3 V ± 10%		40	120	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ± 10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ± 10%			0.5	20	μA
			V_{DD} = 3 V ± 10%			0.3	10	μA
				Ta = 25 °C			5	μA

* **1.** Current flowing to the internal pull-up resistor excluded.

2. The case of subsystem clock oscillation included.

3. When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

4. When operated in the low-speed mode with PCC = 0000.

5. When the system clock control register (SCC) is set to 1001, main system clock oscillation is stopped, and the device is operated on the subsystem clock.

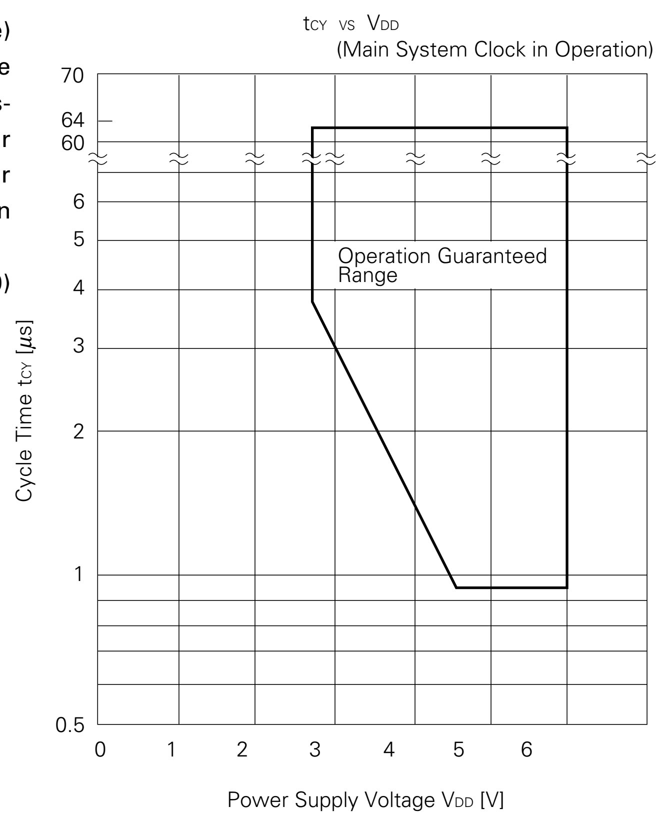
AC CHARACTERISTICS (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

(1) Basic Operation

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Cycle time (minimum instruction execution time)*1	t_{CY}	Operation with main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operation with subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHZ
				0		275	kHz
TI0 input high and low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high and low-level widths	t_{INTH}, t_{INTL}	INT0		*2			μs
		INT1, 2, 4		10			μs
		KR0–7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

* **1.** The cycle time (minimum instruction execution time) is determined by the oscillator frequency of the connected resonator, the system clock control register (SCC) and the processor clock control register (PCC). The cycle time t_{CY} characteristics for power supply voltage V_{DD} when the main system clock is in operation is shown below.

2. $2t_{CY}$ or $128/f_X$ is set by interrupt mode register (IM0) setting.



(2) Serial Transfer Operation

(a) 2-wire and 3-wire serial I/O mode ($\overline{SCK}$...Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V	1600			ns
			3800			ns
$\overline{SCK}$ high and low level widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V	$(t_{KCY}/2)-50$			ns
	t_{KH1}		$(t_{KCY}/2)-150$			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}		150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}		400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R_L = 1 k Ω, C_L = 100 pF*; V_{DD} = 4.5 to 6.0 V			250	ns
		R_L = 1 k Ω, C_L = 100 pF*			1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

(b) 2-wire and 3-wire serial I/O mode ($\overline{SCK}$...External clock input)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V	800			ns
			3200			ns
$\overline{SCK}$ high and low level widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V	400			ns
	t_{KH2}		1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}		100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}		400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R_L = 1 k Ω, C_L = 100 pF*; V_{DD} = 4.5 to 6.0 V			300	ns
		R_L = 1 k Ω, C_L = 100 pF*			1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

(c) SBI mode ($\overline{SCK}$...Internal clock output (master))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V	1600			ns
			3800			ns
$\overline{SCK}$ high and low level widths	t_{KL3}	V_{DD} = 4.5 to 6.0 V	$t_{KCY3}/2-50$			ns
	t_{KH3}		$t_{KCY3}/2-150$			ns
SB0 and SB1 setup time (to $\overline{SCK}$↑)	t_{SIK3}		150			ns
SB0 and SB1 hold time (from $\overline{SCK}$↑)	t_{KSI3}		$t_{KCY3}/2$			ns
SB0 and SB1 output delay time from $\overline{SCK}$↓	t_{KSO3}	V_{DD} = 4.5 to 6.0 V	0		250	ns
			0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}		t_{KCY3}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}		t_{KCY3}			ns
SB0 and SB1 low-level widths	t_{SBL}		t_{KCY3}			ns
SB0 and SB1 high-level widths	t_{SBH}		t_{KCY3}			ns

(d) SBI mode ($\overline{SCK}$...External clock input (slave))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high and low level widths	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0 and SB1 setup time (to $\overline{SCK}$↑)	t_{SIK4}			100			ns
SB0 and SB1 hold time (from $\overline{SCK}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0 and SB1 output delay time from $\overline{SCK}$↓	t_{KSO4}	R_L = 1 kΩ C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0 and SB1 low-level widths	t_{SBL}			t_{KCY4}			ns
SB0 and SB1 high-level widths	t_{SBH}			t_{KCY4}			ns

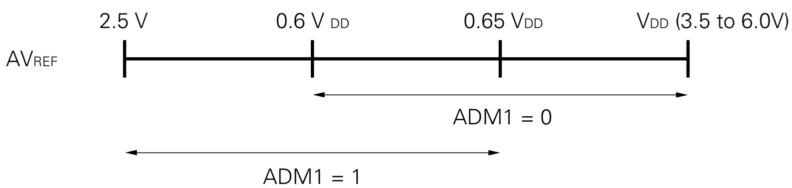
* R_L and C_L are SO output line load resistance and load capacitance, respectively.

(3) A/D Converter (Ta = –40 to +85 °C, V_{DD} = 3.5 to 6.0 V, AV_{SS} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8	8	8	bit
Absolute accuracy***1**		2.5 V ≤ AV_{REF} ≤ V_{DD}***2**			±2.0	LSB
Conversion time***3**	t_{CONV}				168/f_X	μs
Sampling time***4**	t_{SAMP}				44/f_X	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}			1000		MΩ
AV_{REF} current	AI_{REF}			1.0	2.0	mA

* **1.** Absolute accuracy with the quantization error (±1/2 LSB) excluded.

2. ADM1 is set as shown below with regard to the A/D converter reference voltage (AV_{REF}).



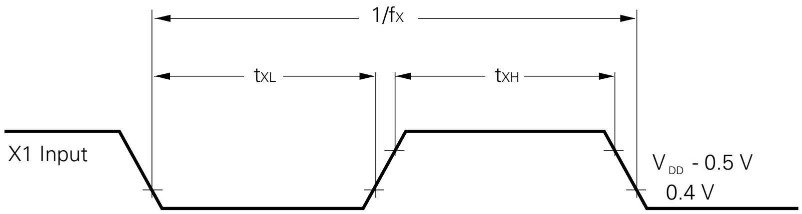
When 0.6 V_{DD} ≤ AV_{REF} ≤ 0.65 V_{DD}, the ADM1 can be set either to 0 or 1.

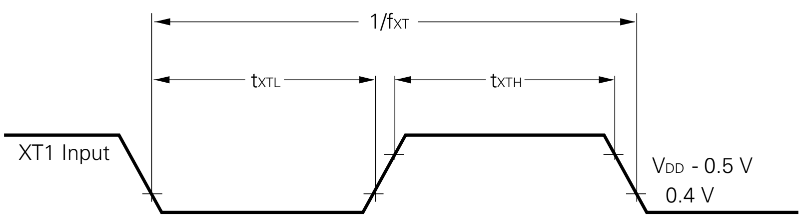
3. This is the time form the execution of the conversion start instruction to the conversion end (EOC = 1) (operating at 40.1 μs : f_X = 4.19 MHz).

4. This is the time from the execution of the conversion start instruction to the sampling end (operating at 10.5 μs : f_X = 4.19 MHz).

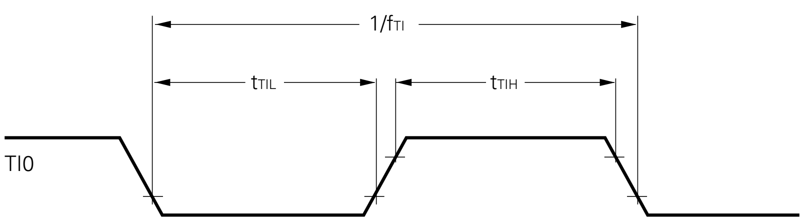
AC Timing Test Points (Except X1 and XT1 Inputs)

Clock Timing



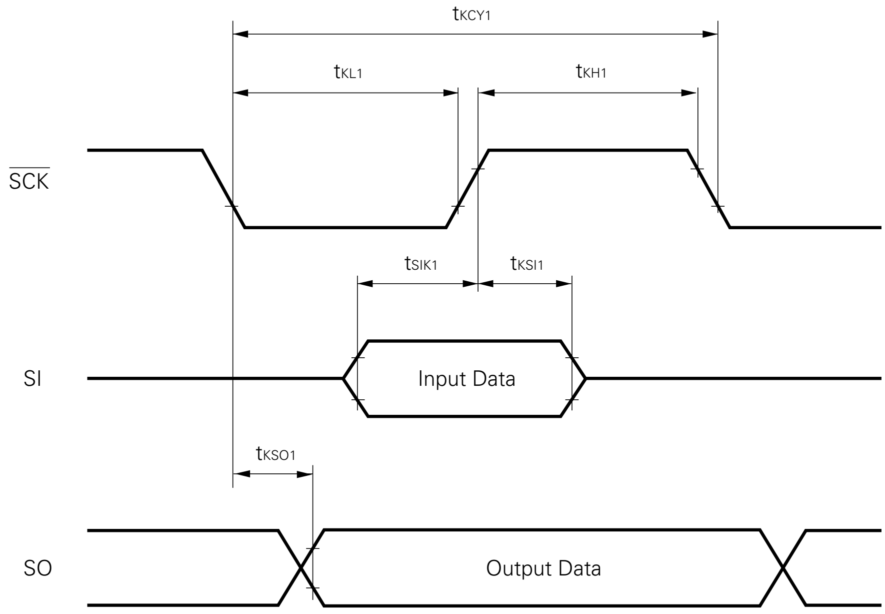


TI0 Timing

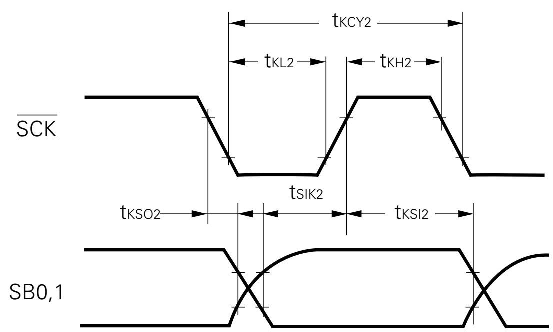


Serial Transfer Timing

3-wire serial I/O mode:

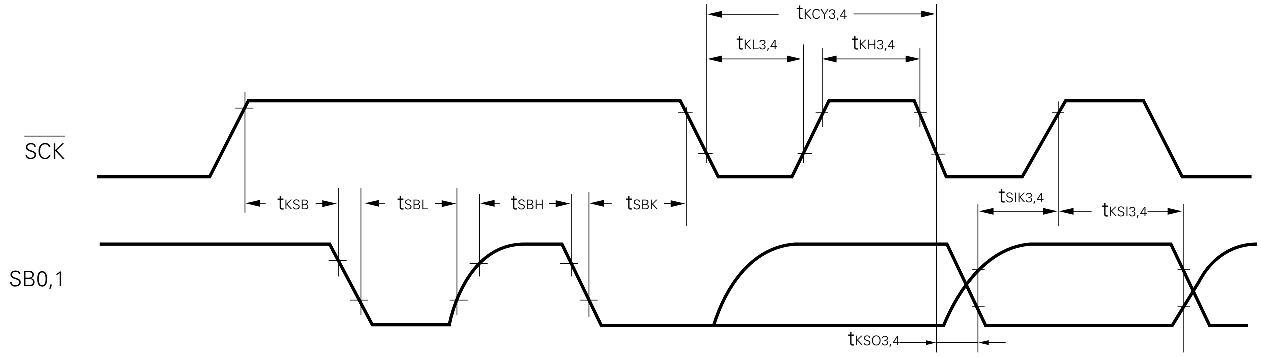


2-wire serial I/O mode:

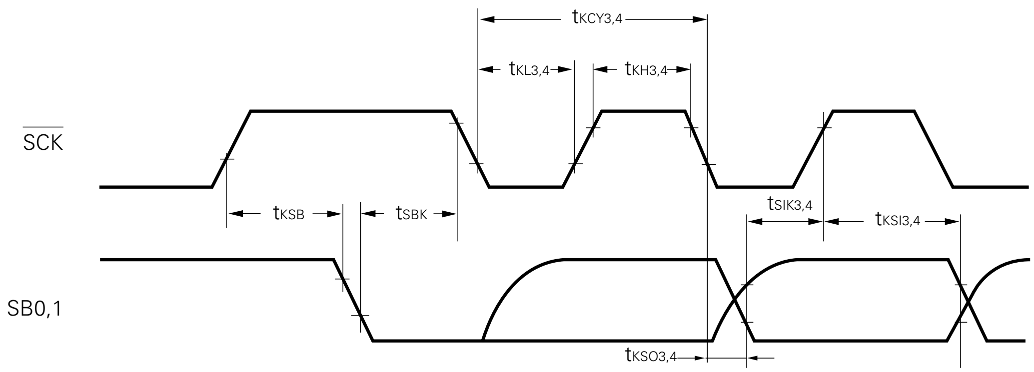


Serial Transfer Timing

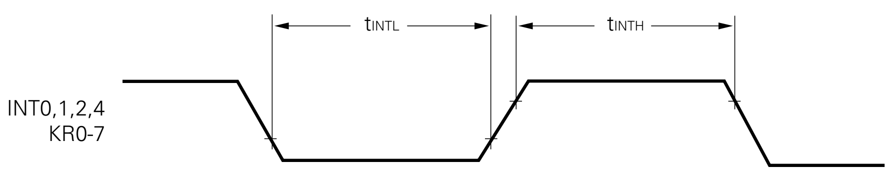
Bus release signal transfer:



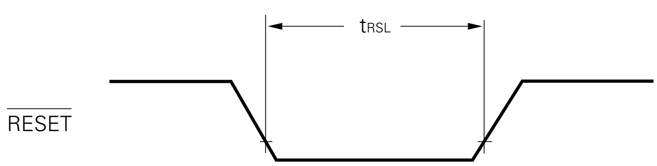
Command signal transfer:



Interrupt Input Timing



RESET Input Timing



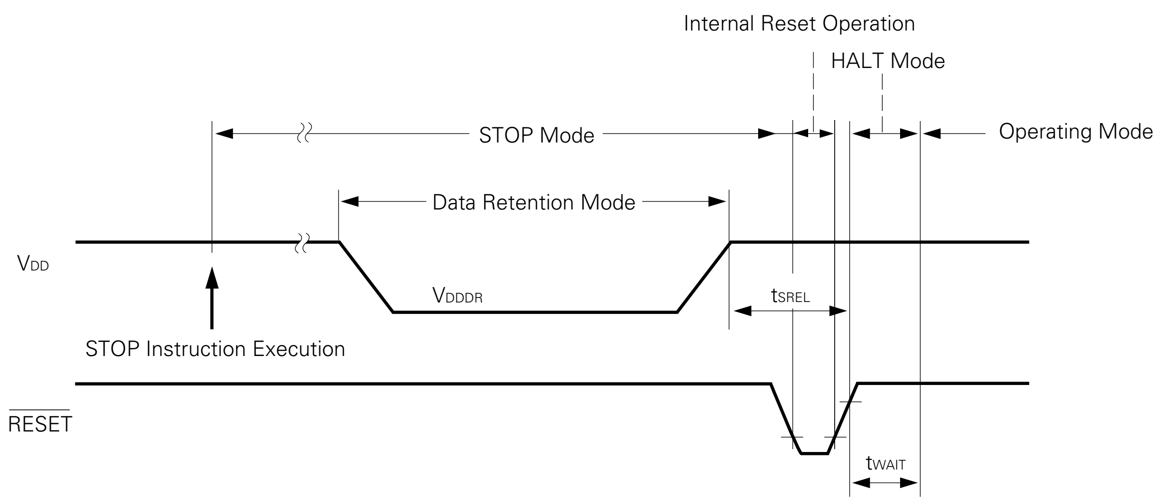
DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V_{DDDR}		2.0		6.0	V
Data retention power supply current *1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time *2	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		*3		ms

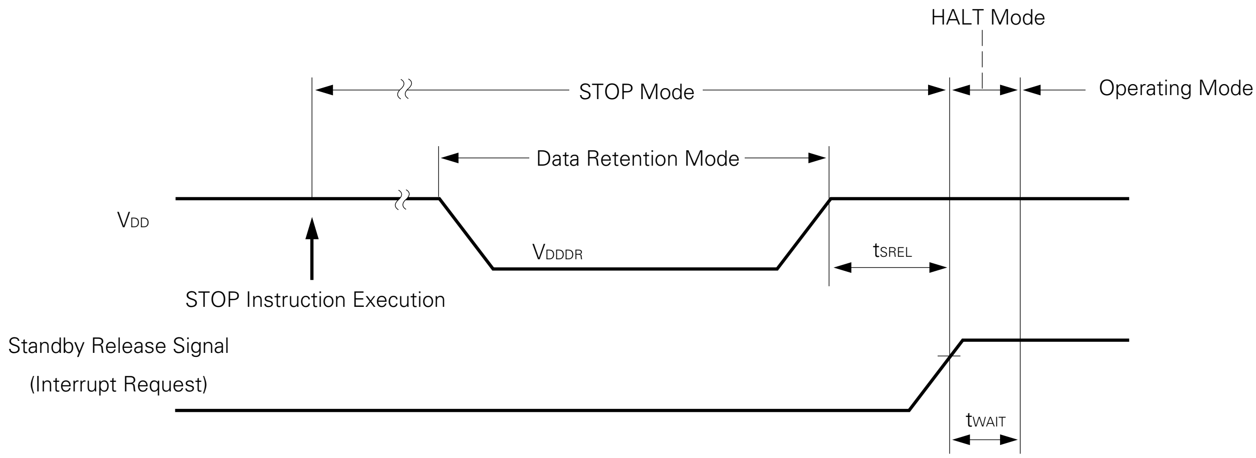
* **1.** Current to the internal pull-up resistor is not included.
2. Oscillation stabilization wait time is time to stop CPU operation to prevent unstable operation upon oscillation start.
3. According to the setting of the basic interval timer mode register (BTM) (see below).

BTM3	BTM2	BTM1	BTM0	Wait Time (Values at f_X = 4.19 MHz in parentheses)
—	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

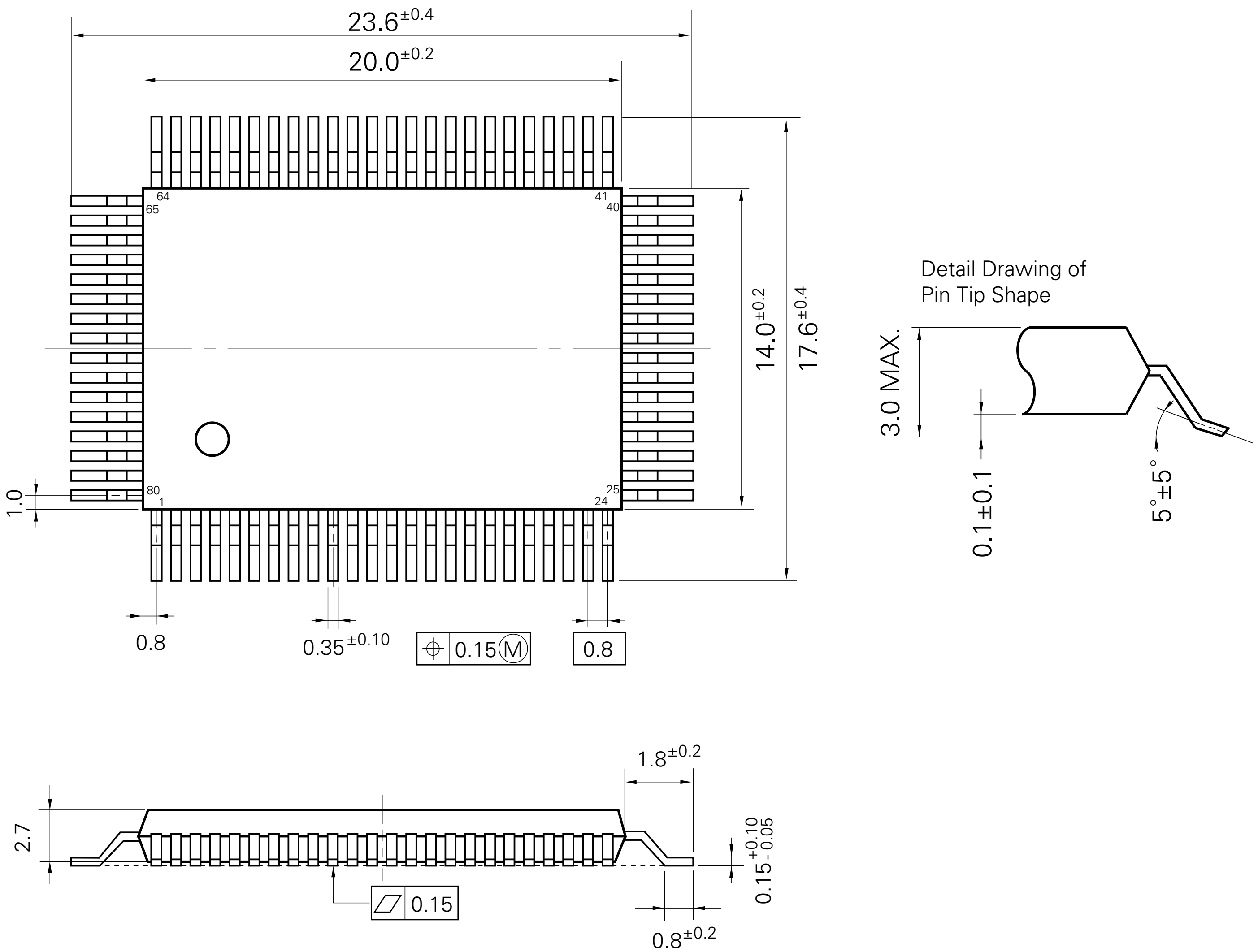


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



11. PACKAGE INFORMATION

80-Pin Plastic QFP (14 × 20) (Unit: mm)



P80GF-80-3B9-2

12. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **"Surface Mount Technology Manual (IEI 1207)"**.

For soldering methods and conditions other than those recommended, please contact our salesman.

Table 12-1 Surface Mount Type Soldering Conditions

μPD75516GF(A)-×××-3B9: 80-Pin Plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommende Condition Symbol
Infrared reflow	Package peak temperature: 230°C Duration: 30 sec. max. (210°C or above) Number of times: once	IR30-00-1
VPS	Package peak temperature: 215°C Duration: 40 sec. max. (200°C or above) Number of times: once	VP15-00-1
Wave soldering	Solder bath temperature: 260°C or less Duration: 10 sec. max. Number of times: once Preparatory heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin part temperature: 300°C or less Duration: 3 sec. max. (per side of device)	—

Note **Use of more than one soldering method should be avoided (except in the case of pin part heating).**

NOTICE

Recommended soldering conditions have been improved for some of these products.
(Improvements: Relaxation of infrared reflow peak temperature (235°C, number of applications (two), time limit, etc.)
Please contact your NEC sales representative for details.

APPENDIX A. DIFFERENCES BETWEEN μPD755××(A) SERIES PRODUCTS

Item		μPD75512(A)	μPD75516(A)	μPD75P516
ROM CONFIGURATION		Mask ROM		EPROM/One Time PROM
ROM (bit)		12160 × 8	16256 × 8	16256 × 8
RAM (bit)		512 × 4		
Mask Option		• Pull-up registor incorporated in port 4, 5, 12, 14 • Pull-down registor incorporated in port 9		No
V_{PP}, PROM pin for program		No		Yes
LED direct drive		Not possible		Possible
Electrical specifications	Power supply voltage range	2.7 to 6.0 V		4.75 to 5.5 V
	Absolute maximum rating	Differ in high-level output current and low-level output current		
	DC characteristic	Differ in low-level output voltage		
	A/D converter characteristic	Differ in ambient temperature range and absolute accuracy.		
Quality grade		Special		Standard
Package		80-Pin Plastic QFP (14 × 20 mm)		• 80-Pin Plastic QFP (14 × 20 mm) • 80-Pin Ceramic WQFN

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for the development of systems using the μPD75516(A).

Hardware	IE-75000-R***1** IE-75001-R		75X series in-circuit emulator
	IE-75000-R-EM***2**		Emulation board for the IE-75000-R or IE-75001-R
	EP-75516GF-R	EV-9200G-80	Emulation probe for the μPD75516(A). An 80-pin conversion socket (EV-9200G-80) is also provided.
	PG-1500		PROM programmer
	PA-75P516GF		PROM programmer adapter for the μPD75P516GF, connected to the PG-1500.
Software	IE Control Program		Host machines PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A***3**) IBM PC/AT™(PC DOS™ Ver. 3.1)
	PG-1500 Controller		
	RA75X Relocatable Assembler		

* **1.** Maintenance product
2. Not incorporated in the IE-75001-R.
3. A task swapping function is provided in Ver. 5.00/5.00A, but this function cannot be used with this software.

Remarks Please refer to the **75X Series Selection Guide (IF-151)** for third party development tools.

APPENDIX C. RELATED DOCUMENTATION

Device Documentation

Document Name		Document No.
User's Manual		IEM-5049
Instruction Application Table		IEM-5036
Application Note	Introduction	IEM-5104
	A/D converter	IEA-630
75X Series Selection Guide		IF-151

Development Tools Documentation

	Document Name		Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846
	IE-75000-R-EM User's Manual		EEU-673
	EP-75516GF-R User's Manual		EEU-703
	PG-1500 User's Manual		EEU-651
Software	RA75X Assembler Package User's Manual	Operation	EEU-731
		Language	EEU-730
	PG-1500 Controller User's Manual		EEU-704

Other Documentation

Document Name	Document No.
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-1207
Quality Grande on NEC Semiconductor Device	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge(ESD) Test	MEM-539
Semiconductor Devices Quality Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604

Note The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.

[MEMO]