NEC

MOS INTEGRATED CIRCUIT

μPD75116H,75117H

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75117H is a 75X Series 4-bit single-chip microcomputer.

The μPD75117H is a product which has the same functions as those of the μPD751××F, with the minimum operating voltage reduced from the previous 2.7 V to 1.8 V, and achieving 1.91 μs operation at 1.8 V. Therefore, it facilitates low-voltage operation for a set requiring high-speed operation.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μPD75117H User's Manual : IEU-799

FEATURES

- Memory capacity
  ROM : 24448 × 8 bits (μPD75117H)
  : 16256 × 8 bits (μPD75116H)
  RAM : 768 × 4 bits
- High-speed low voltage operation
  Minimum instruction execution time : 1.91 μs (V_{DD} = 1.8 V)
  0.95 μs (V_{DD} = 2.7 V)
- Operating voltage range : 1.8 to 5.5 V (T_a = –40 to +60 °C) ★
- Input/output ports : 58
- Timer/counter : 3 channels
  - Timer/event counter × 2 channels
  - Basic interval timer × 1 channel
- 8-bit serial interface on chip
- Programmable threshold port : 4-bit resolution × 4 channels
- On-chip PROM product available : μPD75P117H (One-time PROM)

APPLICATIONS

Cordless telephone subsets, portable radio equipment, pager, etc.

"Unless there are any particular functional differences, the μPD75117H is described in this document as a representative product."

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μPD75116HGC-×××-AB8	64-pin plastic QFP (□14 mm)	Standard
μPD75116HGK-×××-8A8	64-pin plastic QFP (□12 mm)	Standard
μPD75117HGC-×××-AB8	64-pin plastic QFP (□14 mm)	Standard
μPD75117HGK-×××-8A8	64-pin plastic QFP (□12 mm)	Standard

Remarks ×××: ROM code number

OVERVIEW OF FUNCTIONS

Item		Contents
Basic instructions		43
Instruction cycle		0.95 μs, 1.91 μs, 15.3 μs (4.19 MHz operation) 3-stage switching capability
On-chip memory	ROM	24448 × 8 bits (μPD75117H), 16256 × 8 bits (μPD75116H)
	RAM	768 × 4 bits
General register		4 bits × 8 × 4 banks (memory mapping)
Input/output port		Total 58 • CMOS input pins : 10 • CMOS input/output pins : 32 (pins with LED direct drive capability***1**) • N-ch open-drain input/output pins : 12 (pins with LED direct drive capability***2**) (A pull-up resistor can be incorporated bit-wise.) • Comparator input pins (4-bit precision) : 4
Timer/counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (watchdog timer applicable)
Serial interface		• 8 bits • LSB-first/MSB-first switchable • 2 transfer modes (transmission/reception and dedicated reception modes)
Vectored interrupt		• External : 3 • Internal : 4
Test input		• External : 2
Standby		• STOP/HALT mode
Instruction set		• Various bit manipulation instructions (set, reset, test, Boolean operation) • 8-bit data transfer, comparison, operation, increment/decrement instructions • 1-byte relative branch instruction • GETI instruction that can implement arbitrary 2-byte/3-byte instructions with 1 byte
Others		• Bit manipulation memory (bit sequential buffer: 16 bits) on chip
★ Package		• 64-pin plastic QFP (□14 mm) • 64-pin plastic QFP (□12 mm)

★ * **1.** When V_{DD} = 5 V, I_{OL} = 15 mA.

★ **2.** When V_{DD} = 5 V, I_{OL} = 10 mA.

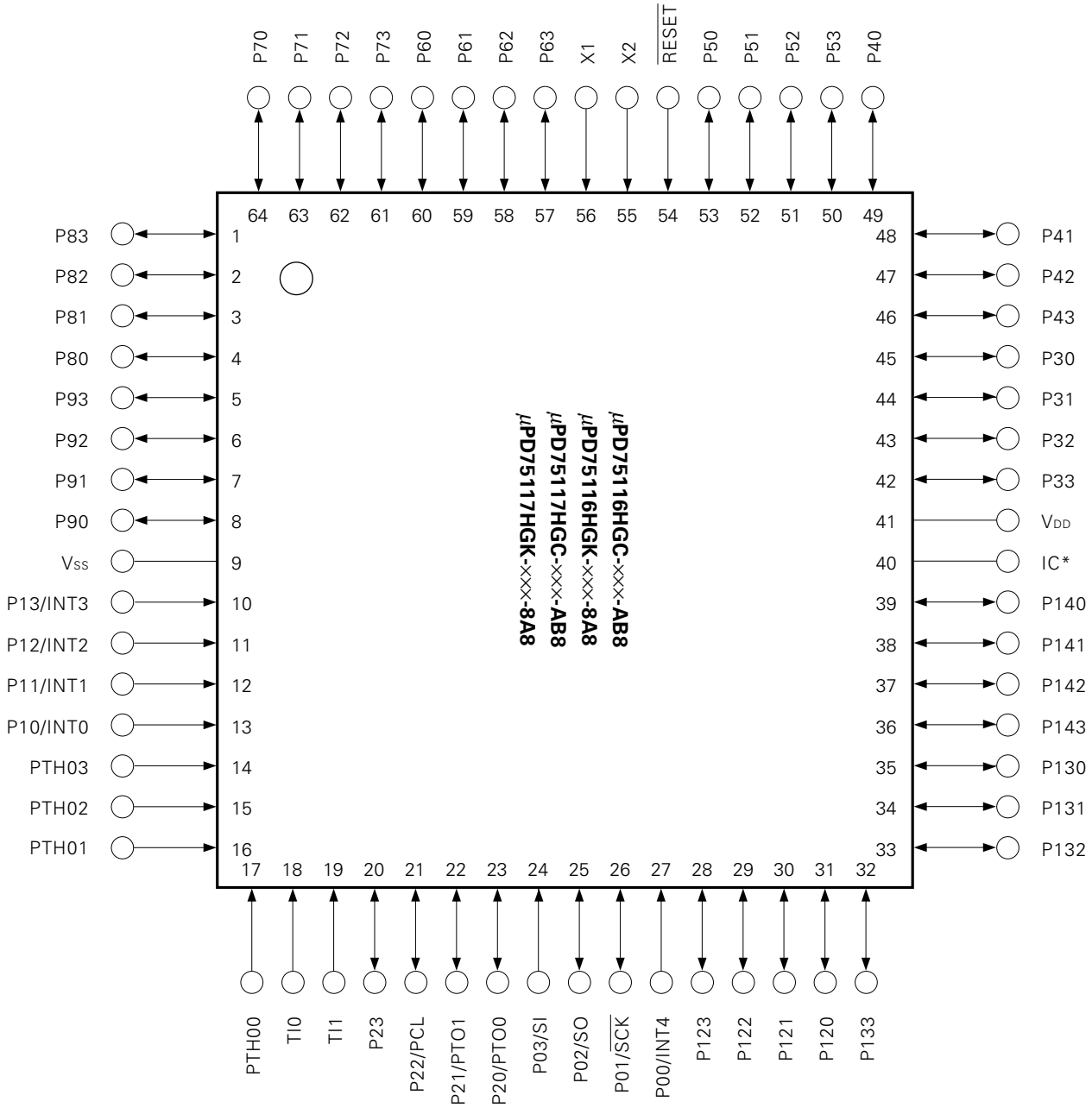
DIFFERENCES BETWEEN μPD75116H AND μPD75117H ★

Item		μPD75116H	μPD75117H
ROM		16256 × 8 bits (Mask ROM)	24448 × 8 bits (Mask ROM)
RAM		768 × 4 bits	
Stack	SBS register	No	Yes
	Stack area	Memory bank 0	Memory banks 0, 1, 2
Stack operation when subroutine call instruction is executed		2-byte stack	3-byte stack
CALL instruction machine cycle		3 machine cycles	4 machine cycles
CALLF instruction machine cycle		2 machine cycles	3 machine cycles

BRA instruction
CALLA instruction
MOVT XA, BCDE
MOVT XA, BCXA
BR BCDE
BR BCXA
		Undefined operation	Normal operation

CONTENTS

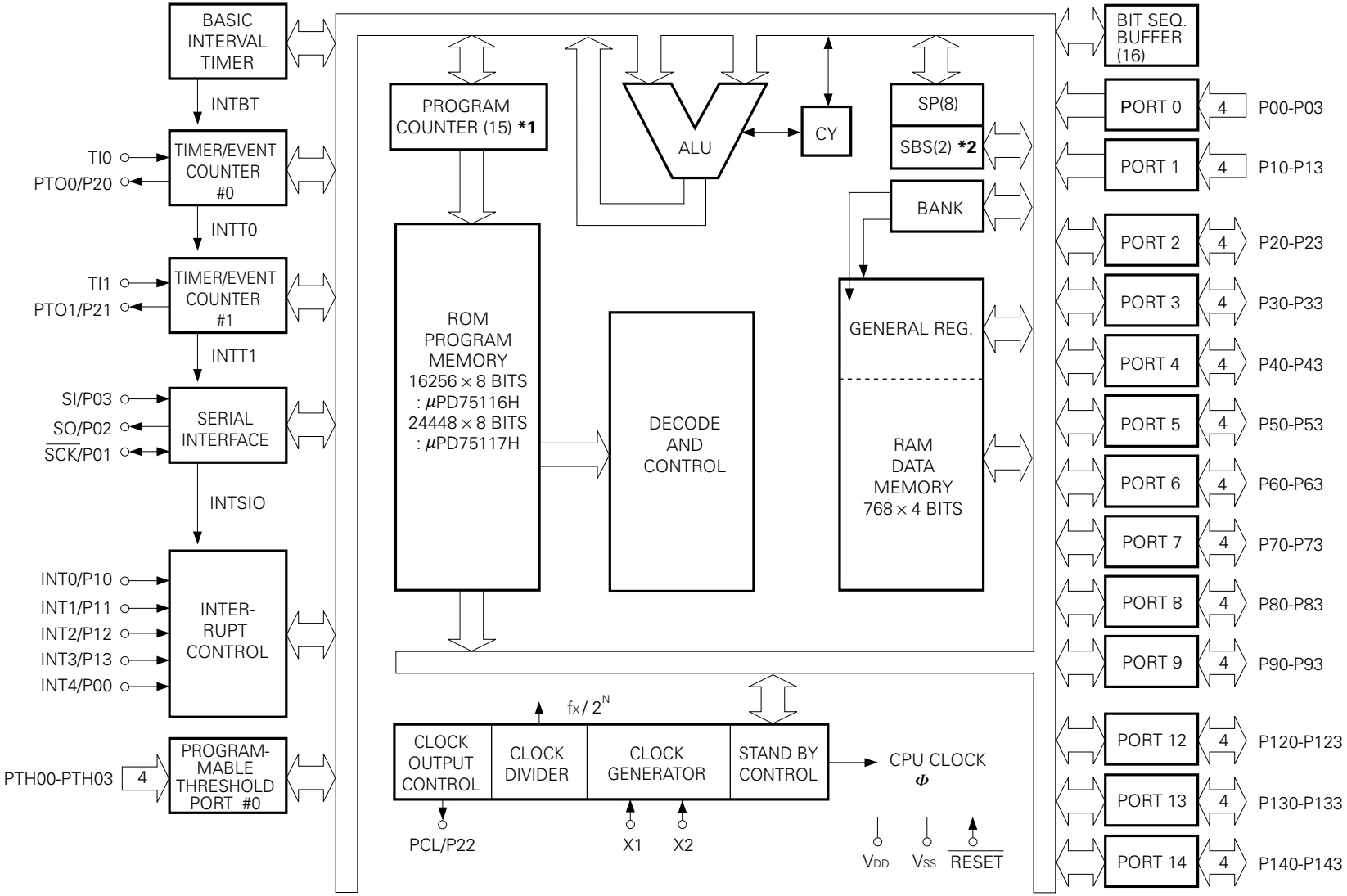
1. PIN CONFIGURATION (TOP VIEW)



* Connect the IC (Internally Connected) pin to V_{DD} directly.

Pin Name

P00-P03	:	Port 0
P10-P13	:	Port 1
P20-P23	:	Port 2
P30-P33	:	Port 3
P40-P43	:	Port 4
P50-P53	:	Port 5
P60-P63	:	Port 6
P70-P73	:	Port 7
P80-P83	:	Port 8
P90-P93	:	Port 9
P120-P123	:	Port 12
P130-P133	:	Port 13
P140-P143	:	Port 14
TI0, TI1	:	Timer Input 0, 1
PTO0, PTO1	:	Programmable Timer Output 0, 1
PCL	:	Programmable Clock Output
$\overline{SCK}$	:	Serial Clock
SO	:	Serial Data Output
SI	:	Serial Data Input
PTH00-PTH03	:	Programmable Treshold Input
INT0, INT1, INT4	:	External Vectored Interrupt Input 0, 1, 4
INT2, INT3	:	External Test Input 2, 3
X1, X2	:	System Clock Oscillation 1, 2
$\overline{RESET}$	:	Reset
V_{DD}	:	Positive Power Supply
V_{SS}	:	Ground
IC	:	Internally Connected



* **1.** The μPD75116H program counter is composed of 14 bits.

2. The μPD75117H incorporates the SBS register.

3. PIN FUNCTIONS

3.1 PORT PINS

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT 0).	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ
P02	Input/output	SO				E
P03	Input	SI				Ⓑ
P10	Input	INT0	4-bit input port (PORT 1).		Input	Ⓑ
P11		INT1				
P12		INT2				
P13		INT3				
P20	Input/output	PTO0	4-bit input/output port (PORT 2). *2	×	Input	E
P21		PTO1				
P22		PCL				
P23		—				
P30 to P33	Input/output	—	Programmable 4-bit input/output port (PORT 3). Input/output can be specified bit-wise. *2		Input	E
P40 to P43	Input/output	—	4-bit input/output port (PORT 4). *2	○	Input	E
P50 to P53	Input/output	—	4-bit input/output port (PORT 5). *2		Input	E
P60 to P63	Input/output	—	Programmable 4-bit input/output port (PORT 6). Input/output can be specified bit-wise. *2	○	Input	E
P70 to P73	Input/output	—	4-bit input/output port (PORT 7). *2		Input	E
P80 to P83	Input/output	—	4-bit input/output port (PORT 8). *2	○	Input	E
P90 to P93	Input/output	—	4-bit input/output port (PORT 9). *2		Input	E
P120 to P123	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 12). On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: +6 V withstand voltage *3	○	Input *4	M
P130 to P133	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 13). On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: +6 V withstand voltage *3		Input *4	M
P140 to P143	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 14). On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: +6 V withstand voltage *3	—	Input *4	M

* **1.** ◯ : Schmitt trigger input

2. Direct LED drive capability (When V_{DD} = 5 V, I_{OL} = 15 mA). ★

3. Direct LED drive capability (When V_{DD} = 5 V, I_{OL} = 10 mA). ★

4. Open-drain ... high impedance
On-chip pull-up resistor ... high level

3.2 OTHER PINS

Pin Name	Input/Output	Dual-Function Pin	Function	Reset	I/O Circuit Type *1
PTH00 to PTH03	Input	—	Variable threshold voltage 4-bit analog input port.		N
TI0	Input	—	External event pulse input to timer/event counter. Or edge detection vectored interrupt input, or 1-bit input is also possible.		Ⓑ
TI1					
PTO0	Input/output	P20	Timer/event counter output.	Input	E
PTO1		P21			
$\overline{SCK}$	Input/output	P01	Serial clock input/output.	Input	Ⓕ
SO	Input/output	P02	Serial data output.	Input	E
SI	Input	P03	Serial data input.	Input	Ⓑ
INT4	Input	P00	Edge detection vector interrupt input (detection of both rising and falling edges)	Input	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge selectable)	Input	Ⓑ
INT1		P11			
INT2	Input	P12	Edge detection test input (rising edge detection)	Input	Ⓑ
INT3		P13			
PCL	Input/output	P22	Clock output	Input	E
X1, X2	Input	—	System clock oscillation crystal/ceramic connection pin. When an external clock is used, the clock is input to X1 and the inverted clock is input to X2.		
$\overline{RESET}$	Input	—	System reset input (low-level active).		Ⓑ
IC	—	—	Internally Connected. IC pin should be connected to V_{DD} directly.		
V_{DD}	—	—	Positive power supply.		
V_{SS}	—	—	GND potential.		

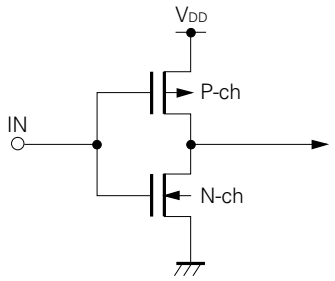
* ◯ : Schmitt trigger input

3.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuits of each pin of the μPD75117H are shown by in abbreviated form.

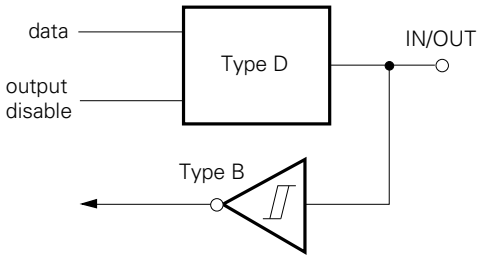
Fig. 3-1 Pin Input/Output Circuit List

Type A



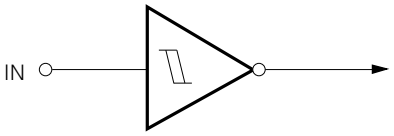
CMOS standard input buffer

Type F



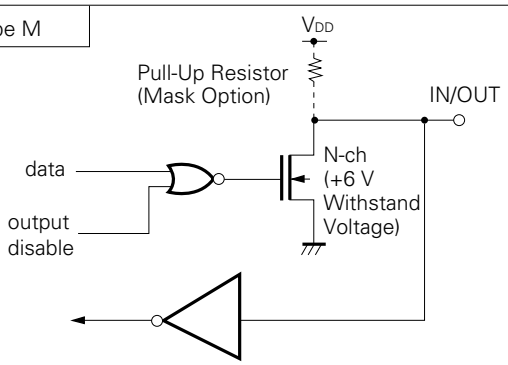
This is an input/output circuit made up of a Type D push-pull output and Type B Schmitt-triggered input.

Type B



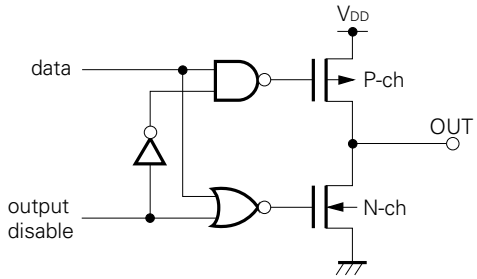
Schmitt-trigger input with hysteresis characteristic

Type M



Middle-High Voltage Input Buffer
(+6 V Withstand Voltage)

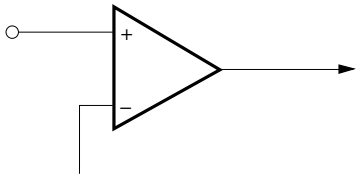
Type D



Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

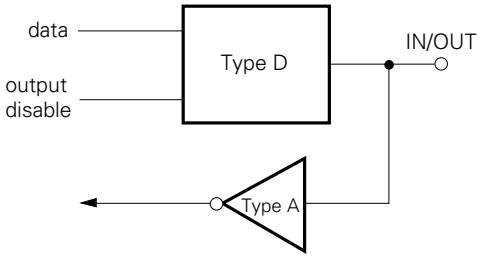
Type N

Comparator



VREF (Threshold Voltage)

Type E



This is an input/output circuit made up of a Type D push-pull output and Type A input buffer.

3.4 RECOMMENDED CONNECTION OF UNUSED PINS

Pin	Recommended Connection
PTH00 to PTH03	Connect to V_{SS} or V_{DD}.
TI0	
TI1	
P00	Connect to V_{SS}.
P01 to P03	Connect to V_{SS} or V_{DD}.
P10 to P13	Connect to V_{SS}.
P20 to P23	Input status : Connect to V_{SS} or V_{DD}. Output status : Leave open.
P30 to P33	
P40 to P43	
P50 to P53	
P60 to P63	
P70 to P73	
P80 to P83	
P90 to P93	
P120 to P123	
P130 to P133	
P140 to P143	
IC	Connect to V_{DD} directly.

4. MEMORY CONFIGURATION

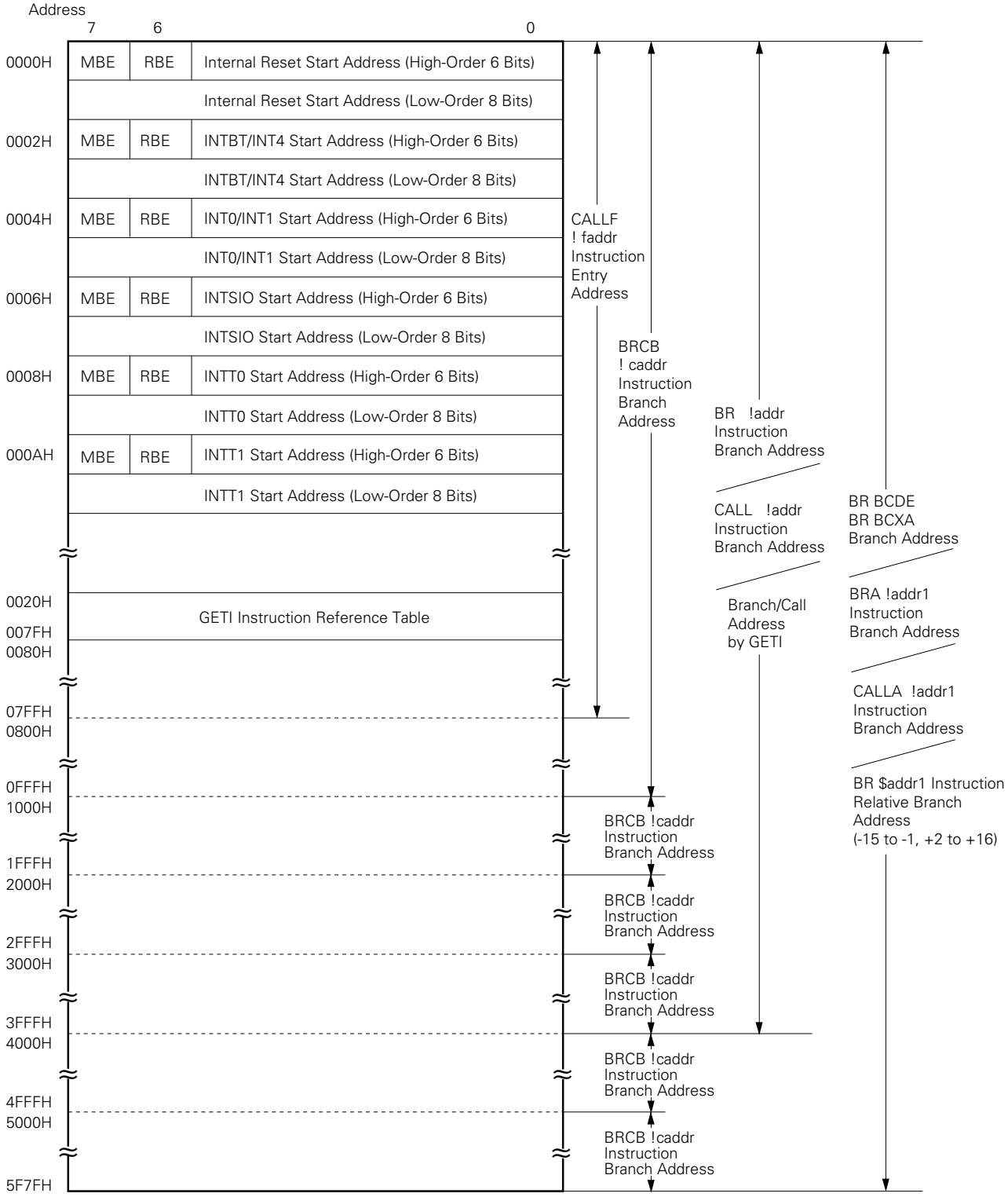
- Program memory (ROM) : 24448 × 8 bits (0000H to 5F7FH) : μPD75117H
  16256 × 8 bits (0000H to 3F7FH) : μPD75116H

  - 0000H, 0001H : Vector table in which a program start address after reset is written.
  - 0002H to 000BH : Vector table in which program start addresses after interruption are written.
  - 0020H to 007FH : Table area referred by GETI instruction

- Data memory
  - Data area : 768 × 4 bits (000H to 2FFH)
  - Peripheral hardware area : 128 × 4 bits (F80H to FFFH)

Fig. 4-1 Program Memory Map (1/2)

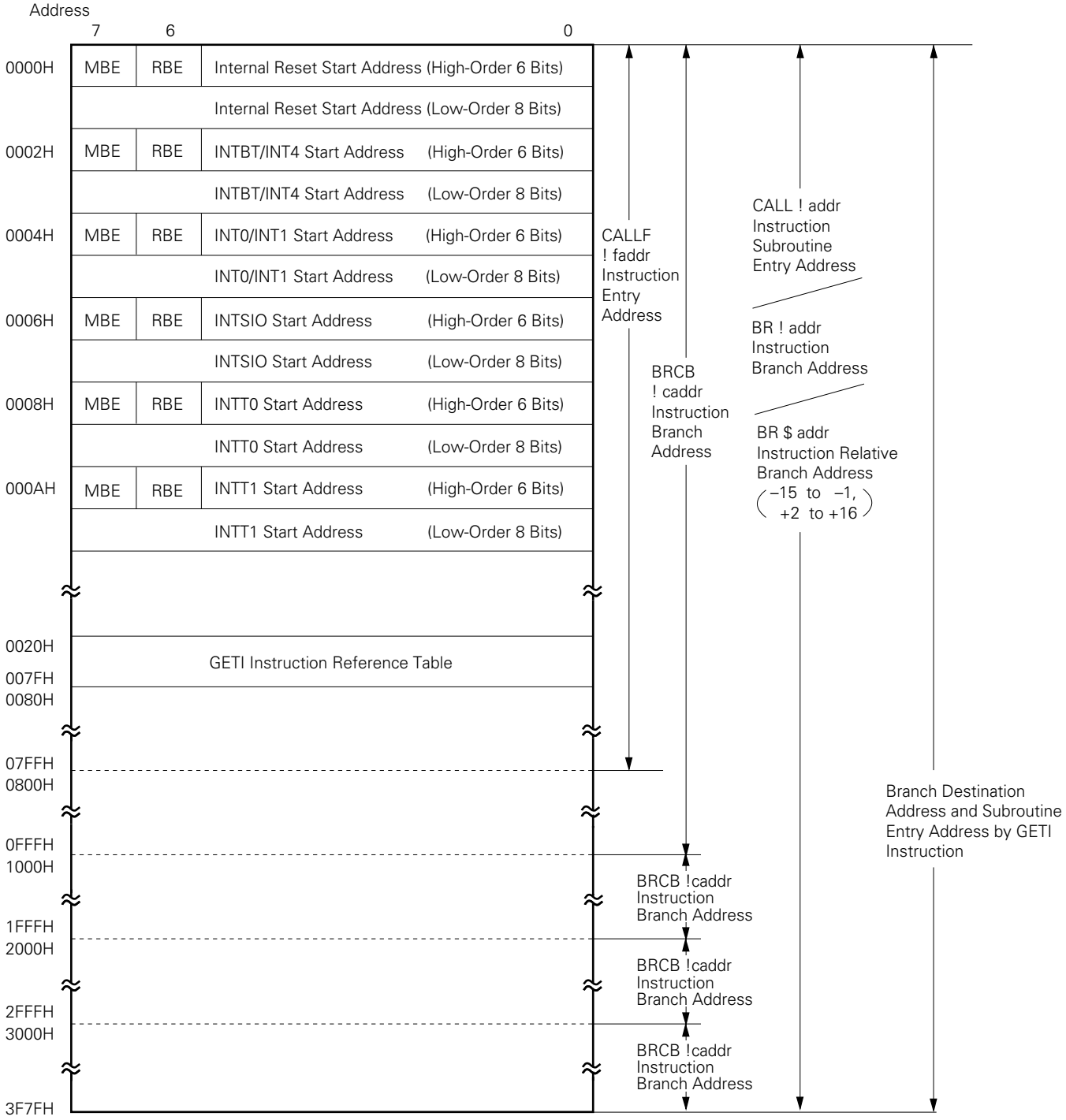
(a) μPD75117H



Note Since the above interrupt vector start address is a 14-bit address, set it in a 16K space (0000H to 3FFFH).

Remarks Apart from the above instructions, branching is possible to an address at which only the PC low-order 8 bits have been changed by the BR PCDE or BR PCXA instruction.

Fig. 4-1 Program Memory Map (2/2)
(b) μPD75116H



Remarks Apart from the above instructions, branching is possible to an address at which only the PC low-order 8 bits have been changed by the BR PCDE or BR PCXA instruction.

Fig. 4-2 Data Memory Map (1/2)
(a) μPD75117H

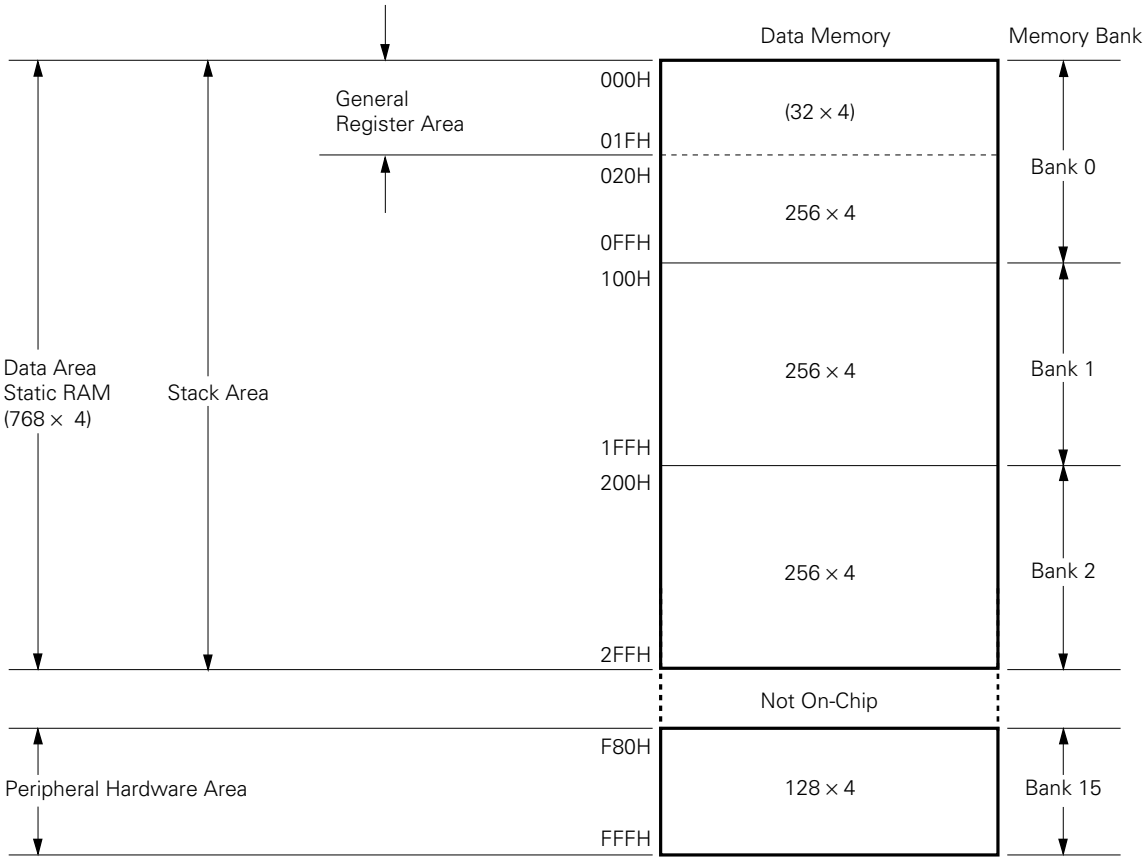
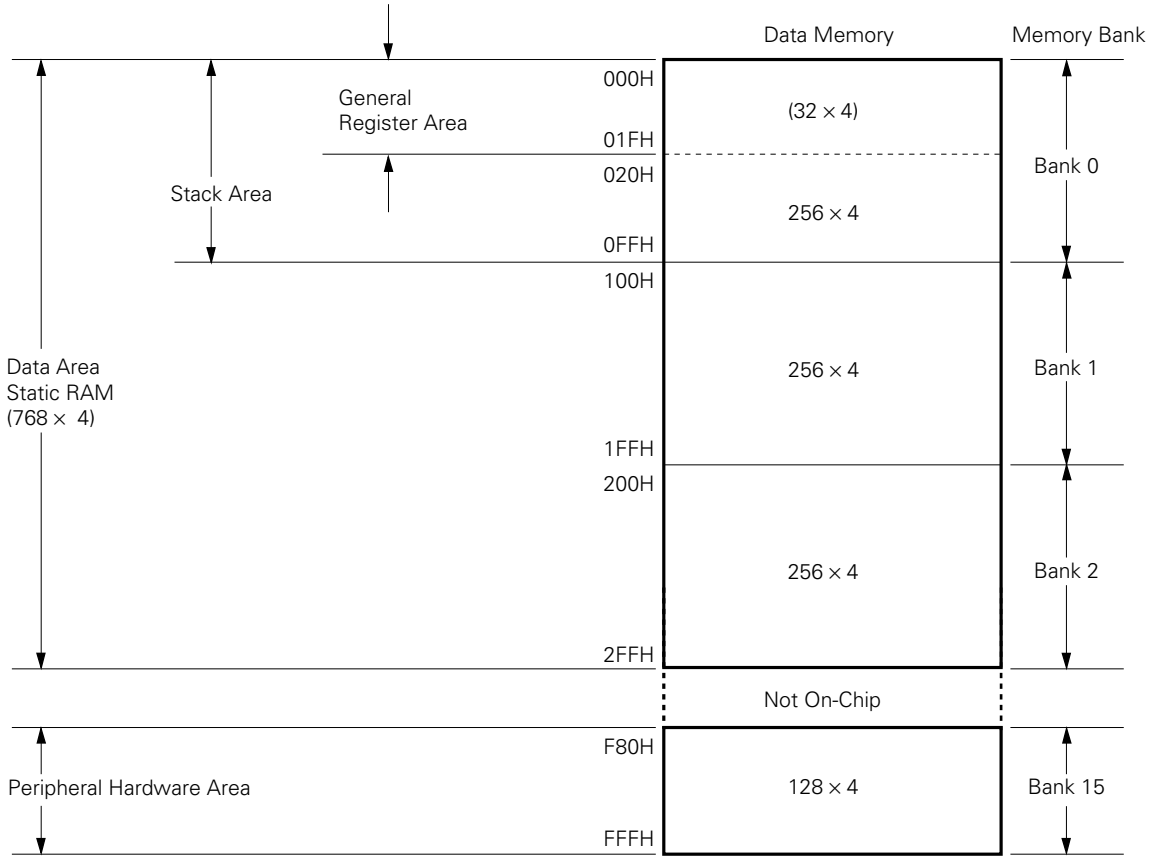


Fig. 4-2 Data Memory Map (2/2)
(b) μPD75116H



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORT

There are the following three digital input/output ports.

- CMOS input (PORT0, PORT1) : 8
- CMOS input/output (PORT2 to PORT9) : 32
- N-ch open-drain input/output (PORT12 to PORT14) : 12

Total : 52

Table 5-1 Port Function

Port Name	Function	Operation/Features	Remarks
PORT 0 PORT 1	4-bit input	Regardless of the operating mode of the shared pin, reading or test is always possible.	These pins are shared with SI, SO, $\overline{SCK}$, INT0 to INT4.
PORT 3 *1 PORT 6 *1	4-bit input/output	Can be set in the input or output bit-wise.	———
PORT 2 *1 PORT 4 *1 PORT 5 *1 PORT 7 *1 PORT 8 *1 PORT 9 *1		Can be set in the input or output mode as a 4-bit unit. Ports 4 and 5, 6 and 7, and 8 and 9 are paired and data input/output is possible as an 8-bit unit.	Port 2, PTO0, PTO1, and PCL share the same pins.
PORT12 *2 PORT13 *2 PORT14 *2	4-bit input/output (N-ch open-drain +6 V withstand voltage)	Can be set to input or output mode as a 4-bit unit. Ports 12 and 13 are paired and data input/output is possible as an 8-bit unit.	On-chip pull-up resistor specifiable bit-wise by mask option.

★ * **1.** When V_{DD} = 5 V, I_{OL} = 15 mA.

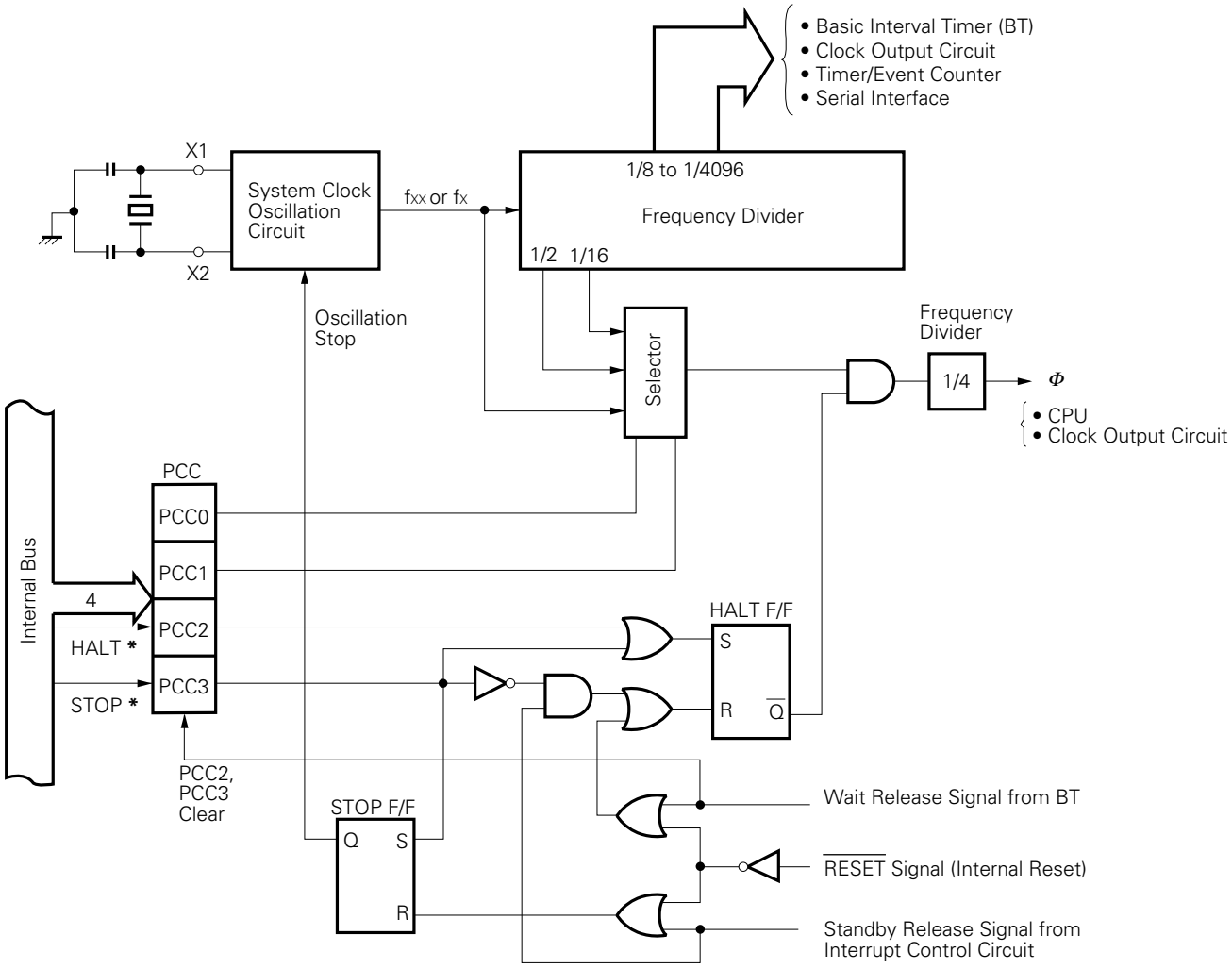
★ **2.** When V_{DD} = 5 V, I_{OL} = 10 mA.

5.2 CLOCK GENERATOR

The clock generator operation is determined by the processor clock control register (PCC).
This circuit can also change the instruction execution time.

- 0.95 μs/1.91 μs/15.3 μs (4.19 MHz operation)

Fig. 5-1 Clock Generator Block Diagram



* Instruction execution

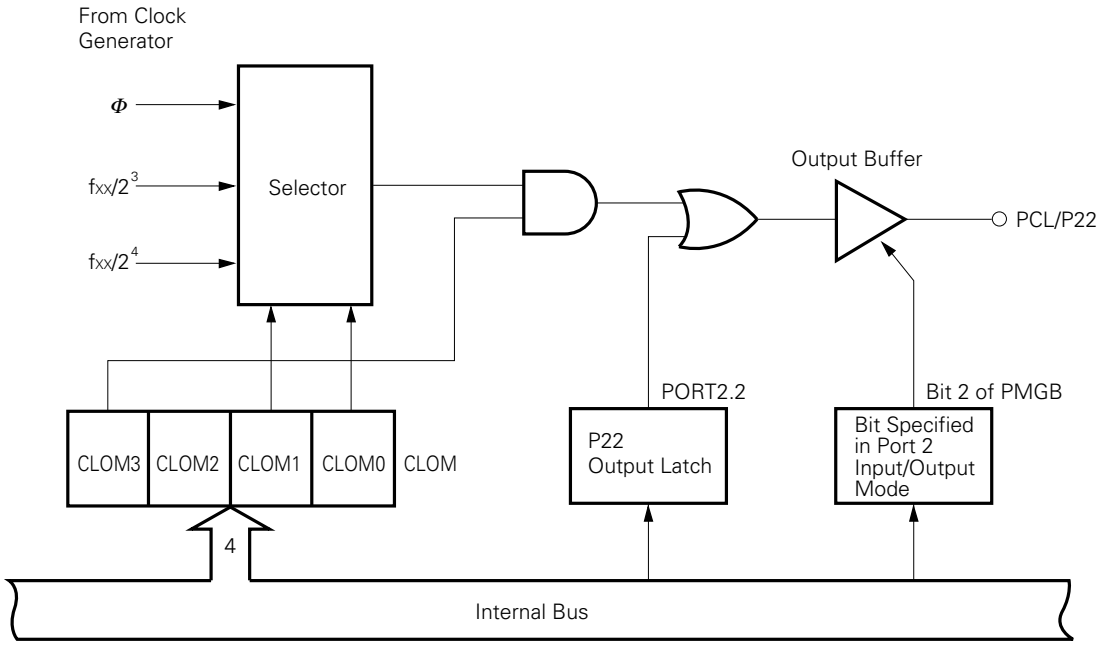
Remarks
1. fxx = Crystal/ceramic oscillator frequency
2. fx = External clock frequency
3. Φ = CPU Clock
4. PCC : Processor clock control register
5. One Φ clock cycle (tcy) is one machine cycle. See "AC CHARACTERISTICS" in **12. "ELECTRICAL SPECIFICATIONS"** for tcy. ★

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit is a circuit which outputs a clock pulse from P22/PCL and is used to supply clock pulses to remote control outputs or peripheral LSI's.

- Clock output (PCL) : Φ, 524 kHz, 262 kHz (4.19 MHz operation)

Fig. 5-2 Configuration of Clock Output Circuit

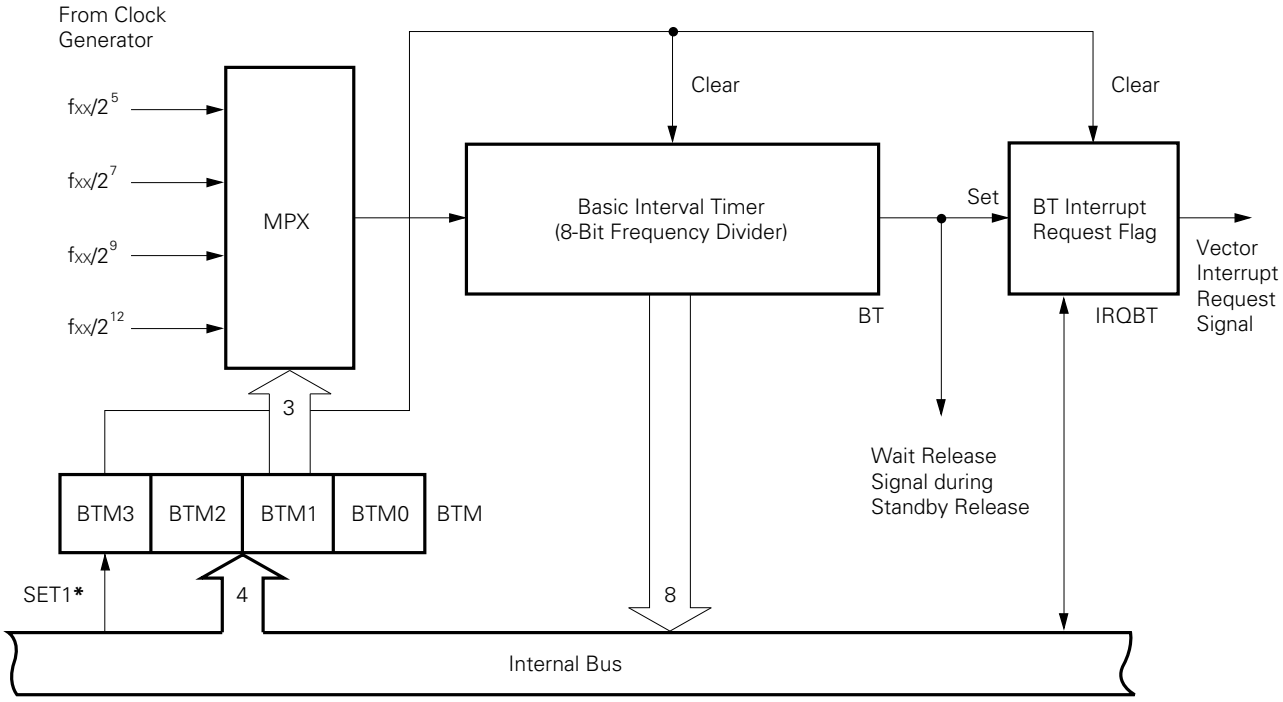


5.4 BASIC INTERVAL TIMER

The basic interval timer includes the following functions.

- It operates as an interval timer which generates reference time interrupts.
- It can be applied as a watchdog timer which detects when a program is out of control.
- Selects and counts wait times when the standby mode is released.
- It reads count contents.

Fig. 5-3 Basic Interval Timer Configuration



* SET1 indicates instruction execution.

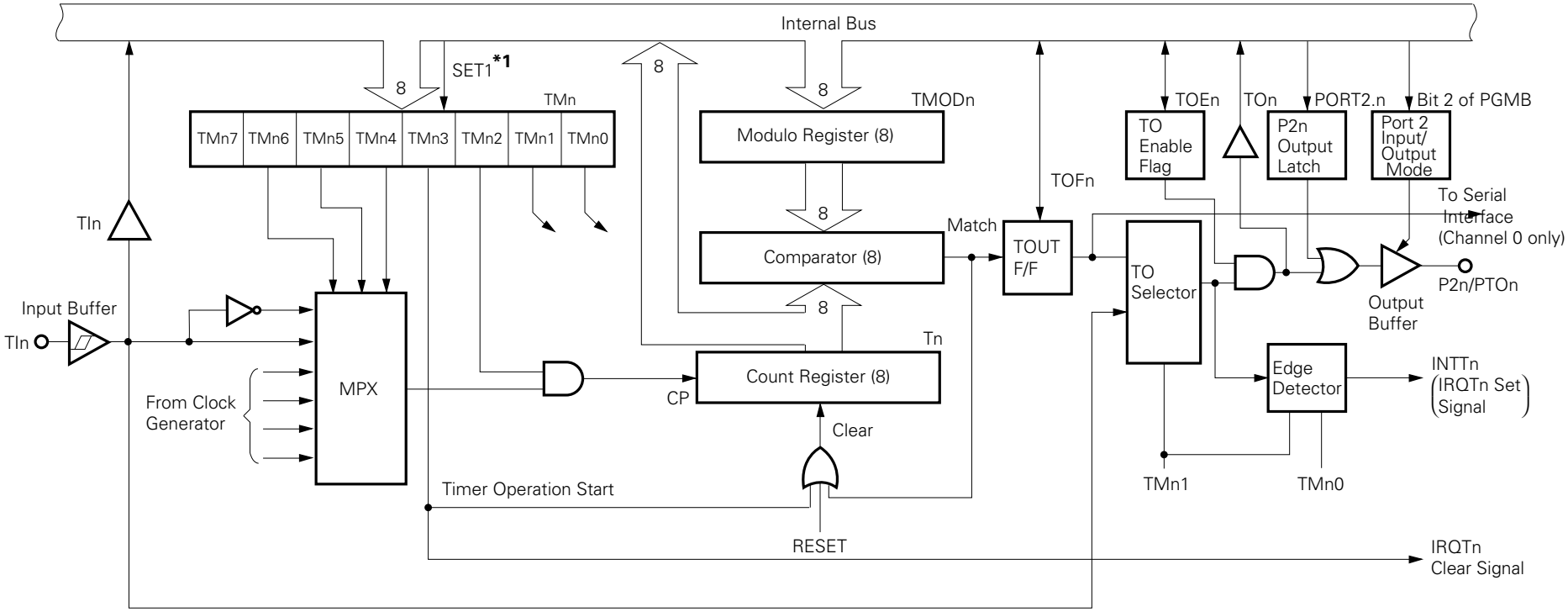
5.5 TIMER/EVENT COUNTER

The μPD75117H incorporates two internal timer/event counter channels.

Timer/event counter channel 0 and channel 1 differ only in selectable count pulse (CP) and clock supply function to serial interface and are the same in other configurations and functions.

- Operates as a programmable interval timer.
- Outputs square waves in the desired frequency to the PTOn pin.
- Operates as an event counter.
- Use of TIn pin as an external interrupt input pin.
- Divides the TIn pin input into N divisions and outputs it to the PTOn pin (frequency divider operation).
- Supplies a serial shift clock to the serial interface circuit. (channel 0 only)
- Count status read function.

Fig. 5-4 Timer/Event Counter Block Diagram (n = 0, 1)



* SET1 : Instruction execution.

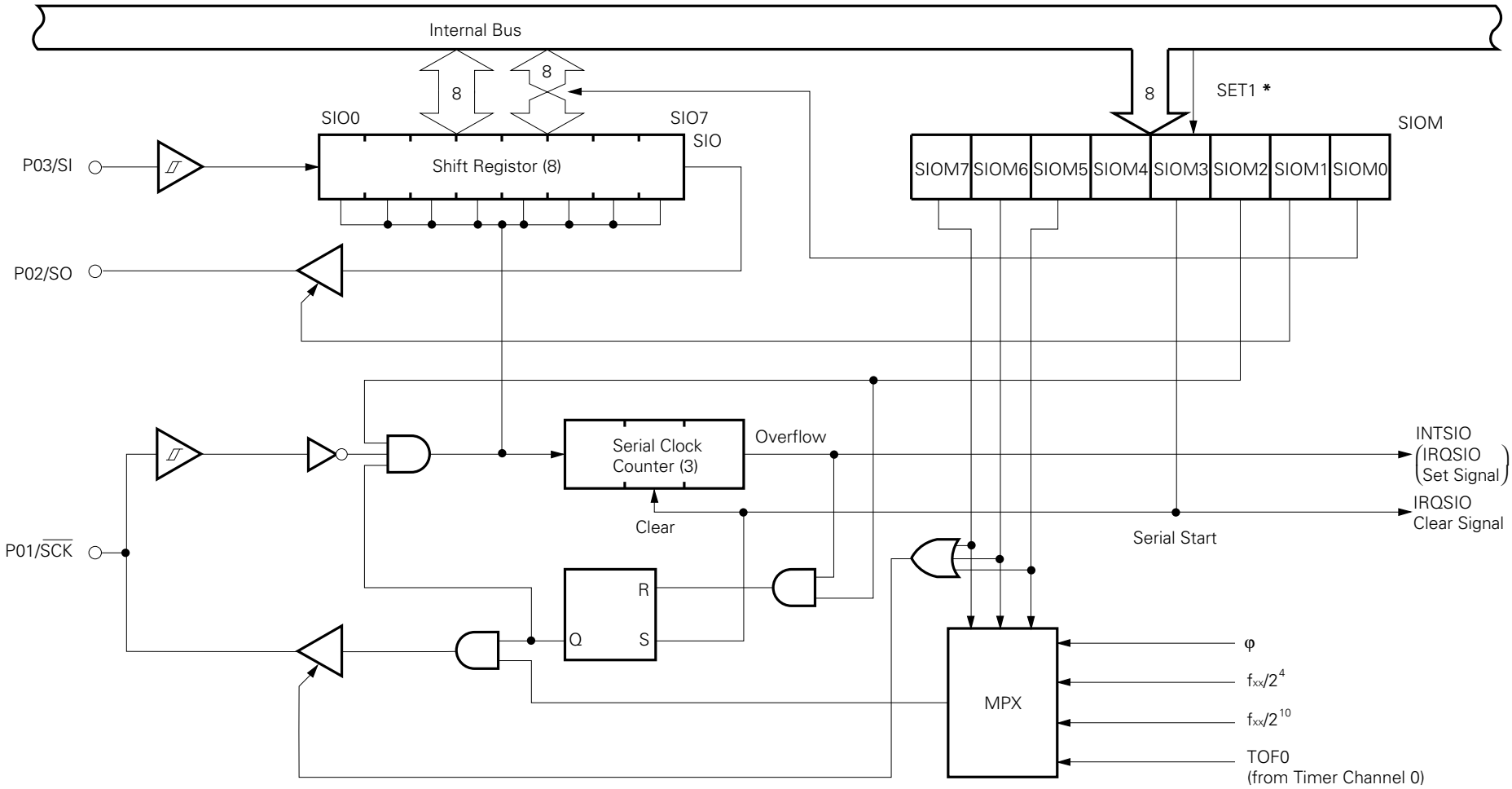
5.6 SERIAL INTERFACE

The serial interface has the following functions.

- Clock 8-bit transmission/reception operation (simultaneous transmission/reception)
- Clock 8-bit reception operation (SO output high impedance)
- Half-duplex asynchronous transfer (software control)
- LSB-first/MSB-first switchable

These functions facilitate serial bus data communications with other computers such as μPD7500 series, 78K series, etc., or conjunction with a peripheral device.

Fig. 5-5 Serial Interface Block Diagram



* SET1 : instruction execution

5.7 PROGRAMMABLE THRESHOLD PORT (ANALOG INPUT PORT)

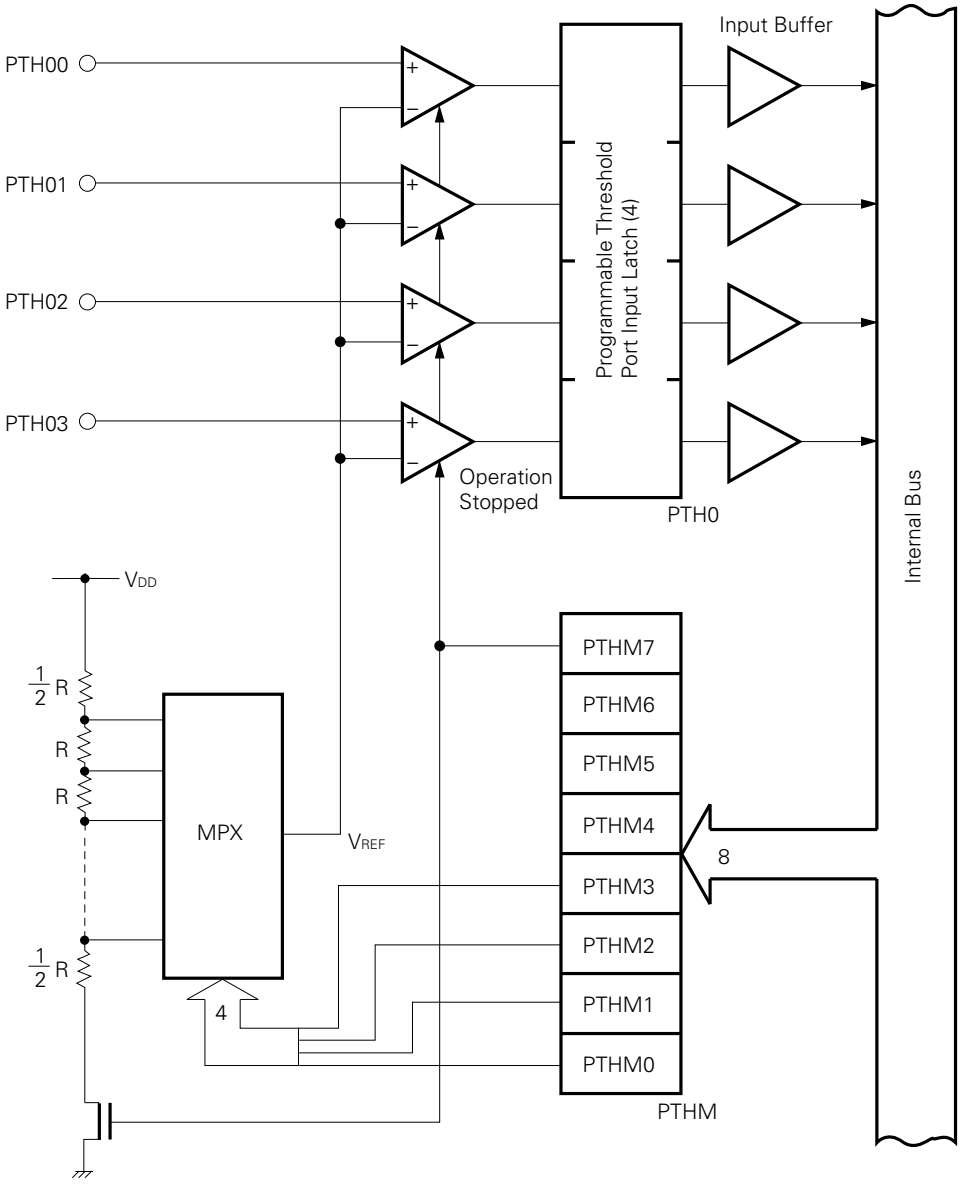
The μPD75117H is provided with 4-bit analog input pins (PTH00 to PTH03) for which the threshold voltage can be changed. These pins have a configuration as shown in Fig. 5-6.

The threshold voltage (V_{REF}) can be selected in 16 ways ($V_{DD} \times \frac{0.5}{16} - V_{DD} \times \frac{15.5}{16}$) and analog signals can be directly input.

This port can also be used as a digital signal input port by selecting $V_{DD} \times \frac{7.5}{16}$ as V_{REF}.

★

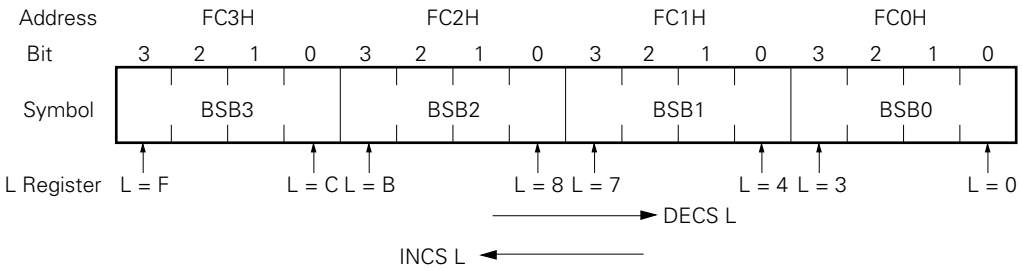
Fig. 5-6 Programmable Threshold Port Block Diagram



5.8 BIT SEQUENTIAL BUFFER ····· 16 BITS

Bit manipulation of the bit sequential buffer is the bit manipulation special data memory. Since, in particular, the bit manipulation can easily be performed by changing sequentially address and bit specification, it is convenient when processing data comprising a large number of bits bit-wise.

Fig. 5-7 Bit Sequential Buffer Format



Remarks In pmem. @L addressing, the specified bit moves according to the L register.

6. INTERRUPT FUNCTION

The μPD75117H has 7 interrupt sources. Multiple interrupts with priority is are also possible. Two test sources are also provided. The test sources are edge detection testable inputs.

Table 6-1 Interrupt Sources

Interrupt Source		Internal/External	Interrupt Order***1**	Vector Interrupt Request Signal (Vector Table Address)
INTBT (standard time interval signal from basic interval timer)		Internal	1	VRQ1 (0002H)
INT4 (both rising edge and falling edge detection)		External		
INT0	(rising edge and falling edge detection selection)	External	2	VRQ2 (0004H)
INT1		External		
INTSIO (serial data transfer end signal)		Internal	3	VRQ3 (0006H)
INTT0 (match signal from timer/event counter# 0 or TI0 input edge detection)		Internal/external	4	VRQ4 (0008H)
INTT1 (match signal from timer/event counter# 1 or TI1 input edge detection)		Internal/external	5	VRQ5 (000AH)

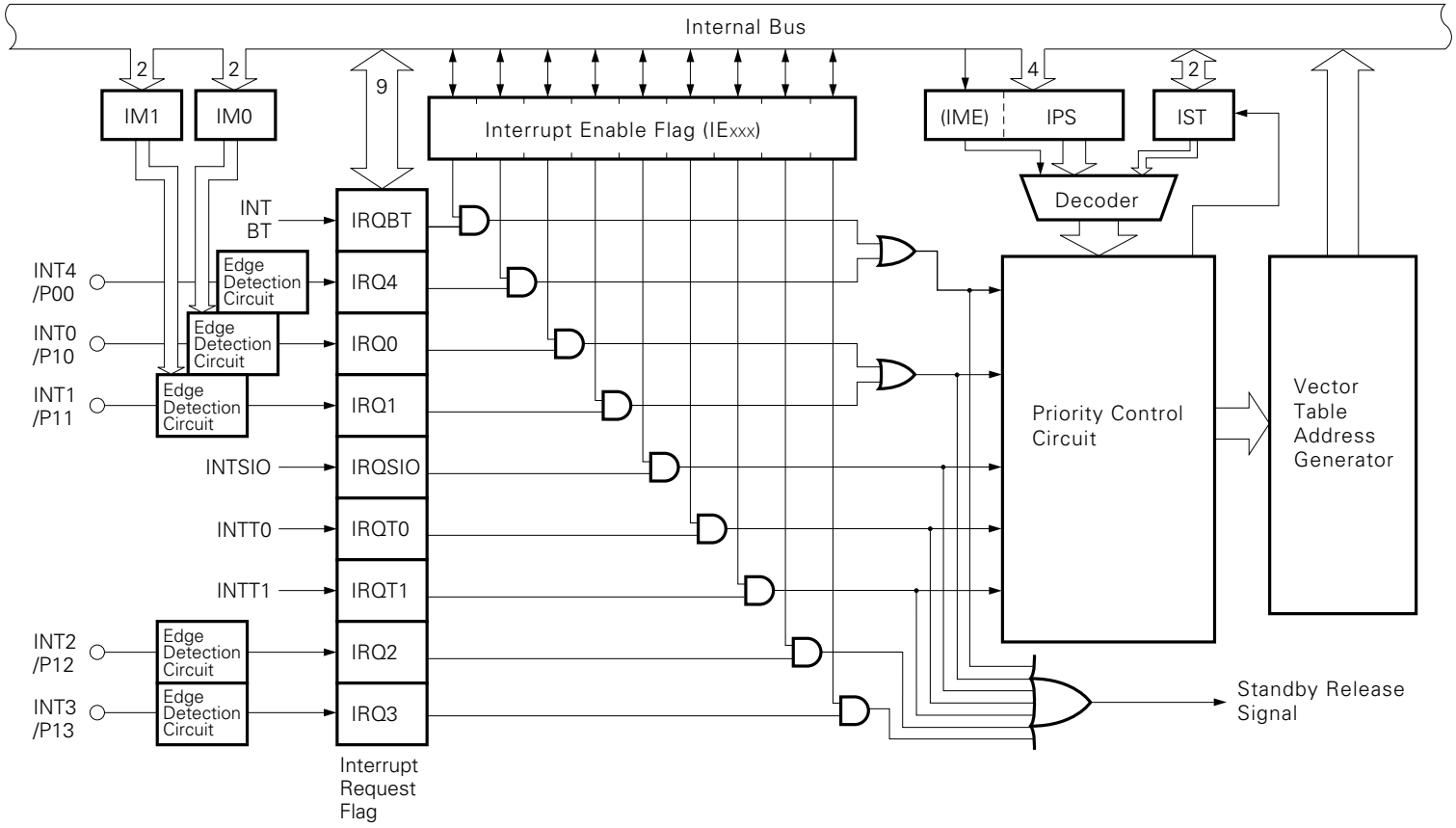
INT2***2** (rising edge detection)	External	Testable input signal (Set IRQ2 and IRQ3)
INT3***2** (rising edge detection)		

* **1.** The interrupt order is the priority order when multiple interrupt requests are generated simultaneously.
2. INT2 and INT3 are of test sources . These are affected by interrupt enable flags in the same way as interrupt sources, but do not generate vector interrupts.

The μPD75117H interrupt control circuit has the following functions:

- Hardware control vector interrupt function that can control interrupt acceptance by interrupt enable flag (IE×××) and interrupt master enable flag (IME).
- Arbitrary setting of interrupt start address.
- Multiple interruption function by which priority can be specified using the interrupt priority selection register (IPS).
- Interrupt request flag (IRQ×××) test function (interrupt generation confirmation by software possible).
- Standby mode release (selection of interrupt that releases the standby mode by interrupt enable flag possible).

Fig. 6-1 Interrupt Control Circuit Block Diagram



7. STANDBY FUNCTION

To reduce the power consumption during program wait, the μPD75117H has two standby modes (STOP mode and HALT mode).

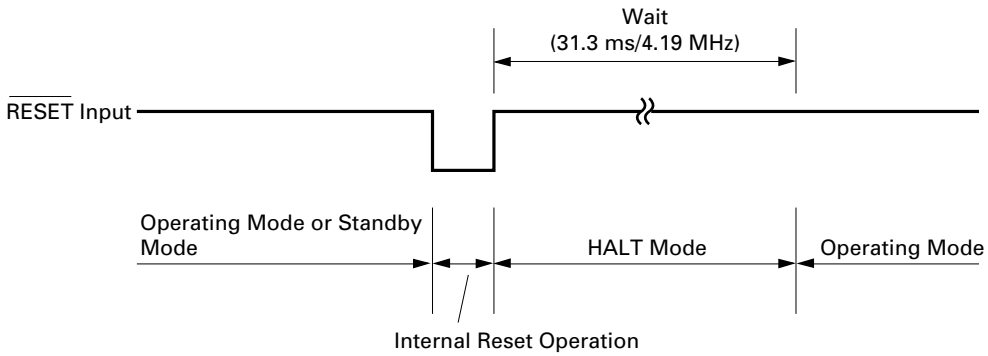
Table 7-1 Standby Mode Setting and Operation Status

		STOP Mode	HALT Mode
Setting instruction		STOP instruction	HALT instruction
Operation Status	Clock generator	System clock oscillation stopped	Only CPU clock Φ stopped
	Basic interval timer	Operation stopped	Operable (IRQBT set at reference time intervals)
	Serial interface	Operation possible only when the external $\overline{SCK}$ input and TO0 output (when timer/event counter 0 is external TI0 input) are selected as a serial clock	Operation possible if a clock other than Φ is specified as a serial clock
	Timer/event counter	Operable only when TIn pin input specified as count clock	Operation possible
	Clock output circuit	Operation stopped	Except CPU clock Φ, output possible.
	External interrupt	Operation of INT0 to INT4 possible	
	CPU	Operation stopped	Operation stopped
Release signal		Interrupt request signal from operable hardware enabled by interrupt enable flag, or $\overline{RESET}$ input	

8. RESET FUNCTION

The reset operation timing is shown in Fig. 8-1.

Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input



The state of hardware after reset operation is as shown in Table 8-1.

Table 8-1 Status of Each Hardware after Resetting (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program counter (PC)		Low-order 6 bits of program memory address 0000H are set in PC_{13} to PC_8 and the contents of address 0001H are set in PC_7 to PC_0. PC_{14}***1** is set to 0.	Low-order 6 bits of program memory address 0000H are set in PC_{13} to PC_8 and the contents of address 0001H are set in PC_7 to PC_0. PC_{14}***1** is set to 0.
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0, IST1)	0	0
	Bank enable flag (MBE, RBE)	Sets program memory address 000H bit 6 and bit 7 to RBE and MBE, respectively.	Sets program memory address 000H bit 6 and bit 7 to RBE and MBE, respectively.
Stack pointer (SP)		Undefined	Undefined
Stack bank selection register (SBS) ***1**		Undefined	Undefined
Data memory (RAM)		Held ***2**	Undefined
General register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank selection register (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter (n = 0, 1)	Counter (Tn)	0	0
	Modulo register (TMODn)	FFH	FFH
	Mode register (TMn)	0	0
	TOEn, TOFn	0, 0	0, 0
Serial interface	Shift register (SIO)	Held	Undefined
	Mode register (SIOM)	0	0
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	Clock output mode register (CLOM)	0	0

*** 1.** Compatible with the μPD75117H only.

2. Data of data memory addresses 0F8H to 0FDH becomes undefined by $\overline{\text{RESET}}$ input.

Table 8-1 Status of Each Hardware after Resetting (2/2)

Hardware			$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
★ Interrupt function	Interrupt request flag (IRQ×××)	IRQ1,IRQ2, IRQ4	Undefined	Undefined
		Other than above	0	0
	Interrupt enable flag (IE×××)		0	0
	Priority selection register (IPS)		0	0
	INT0, INT1 mode registers (IM0, IM1)		0, 0	0, 0
Digital port	Output buffer		OFF	OFF
	Output latch		Clear (0)	Clear (0)
	I/O mode register (PMGA, PMGB, PMGC)		0	0
Analog port	PTH00 to PTH03 input latch		Undefined	Undefined
	Mode register (PTHM)		0	0
Bit sequential buffer (BSB0 to BSB3)			0	0

9. INSTRUCTION SET

(1) Operand identifier and description

The operand is described in the operand field of each instruction in accordance with the description for the operand identifier of the instruction. (For details, refer to **RA75X Assembler Package User's Manual Language Volume (EEU-730)**.) When there are multiple elements in the description, one of the elements is selected. Upper case letters and symbols (+,–) are keywords and are described unchanged.

Various register or flag symbols can be used as a label instead of mem, fmem, pmem, bit, etc. (For details, refer to **μPD75117H User's Manual (IEU-799)**.) However, there are restrictions on the labels for which fmem and pmem can be used.

Identifier	Description	
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'	
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem bit	8-bit immediate data or label* 2-bit immediate data or label	
fmem pmem	FB0H to FBFH, FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label	
addr	μPD75116H	0000H to 3F7FH immediate data or label
	μPD75117H	0000H to 3FFFH immediate data or label
addr1	0000H to 5F7FH immediate data or lebel	
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (however, bit0 = 0) or label	
PORTn IE××× RBn MBn	PORT 0 to PORT 9, PORT12 to PORT14 IEBT, IESIO, IET0, IET1, IE0 to IE4 RB0 to RB3 MB0, MB1, MB2, MB15	

***** In the case of the 8-bit data processing, an even address only can be described for mem.

(2) Operation description legend

A	:	A register; 4-bit accumulator
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
X	:	X register
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
XA'	:	Extension register pair (XA')
BC'	:	Extension register pair (BC')
DE'	:	Extension register pair (DE')
HL'	:	Extension register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Portn (n = 0 to 9, 12 to 14)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority selection register
IE×××	:	Interrupt enable flag
RBS	:	Register bank selection register
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
.	:	Address, bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Description of addressing area field symbols

*1	MB = MBE • MBS (MBS = 0, 1, 2, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H to 7FH) MB = 15 (80H to FFH) MBE = 0 : MB = MBS (MBS = 0, 1, 2, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 3F7FH (μPD75116H) 0000H to 3FFFH (μPD75117H)	Program memory addressing
*7	• μPD75116H addr = (Current PC) –15 to (Current PC) –1, (Current PC) + 2 to (Current PC) + 16	
	• μPD75117H addr1 = (Current PC) –15 to (Current PC) –1, (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H to 0FFFH (PC$_{13, 12}$ = 00B : μPD75116H) = 0000H to 0FFFH (PC$_{14, 13, 12}$ = 000B : μPD75117H) = 1000H to 1FFFH (PC$_{13, 12}$ = 01B : μPD75116H) = 1000H to 1FFFH (PC$_{14, 13, 12}$ = 001B : μPD75117H) = 2000H to 2FFFH (PC$_{13, 12}$ = 10B : μPD75116H) = 2000H to 2FFFH (PC$_{14, 13, 12}$ = 010B : μPD75117H) = 3000H to 3F7FH (PC$_{13, 12}$ = 11B : μPD75116H) = 3000H to 3FFFH (PC$_{14, 13, 12}$ = 011B : μPD75117H) = 4000H to 4FFFH (PC$_{14, 13, 12}$ = 100B : μPD75117H) = 5000H to 5F7FH (PC$_{14, 13, 12}$ = 101B : μPD75117H)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	
*11	addr1 = 0000H to 5F7FH (: μPD75117H only)	

Remarks
1. MB indicates the accessible memory bank.
2. For *2, MB = 0 without regard to MBE and MBS.
3. For *4 and *5, MB = 15 without regard to MBE and MBS.
4. *6 to *10 indicate the addressable area.

(4) Explanation of machine cycle field

S shows the number of machine cycles required when skip is performed by an instruction with skip. The value of S changes as follows:

- No skip ..... S = 0
- When instruction to be skipped is 1-byte or 2-byte instruction ..... S = 1
- When instruction to be skipped is 3-byte instruction ..... S = 2
  (BR !addr, BRA !addr1*, CALL !addr, CALLA !addr1* instructions)

* This instruction is valid for the μPD75117H only.

Note One machine cycle is required to skip a GETI instruction.

One machine cycle is equivalent to one cycle (= t_{CY}) of the CPU clock Φ. Three times can be selected by PCC setting.

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A ← n4		Stack A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		Stack A
		HL, #n8	2	2	HL ← n8		Stack B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A, @HL-	1	2 + S	A ← (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2 + S	A ↔ (HL), then L ← L + 1	*1	L = 0
		A, @HL-	1	2 + S	A ↔ (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A,reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Table reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8} + DE)_{ROM}$		
					XA ← $(PC_{14-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8} + XA)_{ROM}$		
					XA ← $(PC_{14-8} + XA)_{ROM}$		
		XA, @BCDE*	1	3	XA ← $(B_{2-0} + CDE)_{ROM}$	*11	
		XA, @BCXA*	1	3	XA ← $(B_{2-0} + CXA)_{ROM}$	*11	

* The 3 lower bits in the B register are valid only.

Remarks Shading indicates a part compatible with the μPD75117H.

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← (H + mem$_{3-0}$.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← CY	*5	
		@H+mem.bit, CY	2	2	(H + mem$_{3-0}$.bit) ← CY	*1	
Operations	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1, XA	2	2 + S	rp'1 ← rp'1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp'	2	2	XA, CY ← XA + rp' + CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
		XA, rp'	2	2 + S	XA ← XA – rp'		borrow
		rp'1, XA	2	2 + S	rp'1, CY ← rp'1 – XA – CY		borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
		XA, rp'	2	2	XA, CY ← XA – rp' – CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 – XA – CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
		XA, rp'	2	2	XA ← XA ⊻ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ⊻ XA		

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Accumulator manipulation	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment /decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
		rp'	2	2 + S	rp' ←rp' – 1		rp' = FFH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) \leftarrow 1$	*5	
		@H + mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 1$	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) \leftarrow 0$	*5	
		@H + mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 0$	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) = 1$	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) = 0$	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 0$	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0}))$ = 1 and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit)$ = 1 and clear	*1	(@H + mem.bit) = 1

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Memory bit manipulation	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∧ (H + mem_{3-0}.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨ (H + mem_{3-0}.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∨̄ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨̄ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨̄ (H + mem_{3-0}.bit)	*1	
Branch	BR	addr ***1**	—	—	PC_{13-0} ← addr (The assembler selects the optimum instruction from among the BR !addr, BRCB !caddr, and BR $addr instructions.)	*6	
		addr1	—	—	PC_{14-0} ← addr1 (The assembler selects the optimum instruction from among the BR !addr, BRA !addr1, BRCB !caddr, and BR $addr1 instructions.)	*11	
		!addr	3	3	PC_{13-0} ← addr	*6	
					PC_{14-0}, PC_{13-0} ← addr		
		$addr	1	2	PC_{13-0} ← addr	*7	
		$addr1	1	2	PC_{14-0} ← addr1		
		PCDE	2	3	PC_{13-0} ← PC_{13-8} + DE		
					PC_{14-0} ← PC_{14-8} + DE		
		PCXA	2	3	PC_{13-0} ← PC_{13-8} + XA		
					PC_{14-0} ← PC_{14-8} + XA		
		BCDE ***2**	2	3	PC_{14-0} ← B_{2-0} + CDE	*11	
		BCXA ***2**	2	3	PC_{14-0} ← B_{2-0} + CXA	*11	
	BRA	!addr1	3	3	PC_{14-0} ← !addr1	*11	
	BRCB	!caddr	2	2	PC_{13-0} ← $PC_{13,12}$ + $caddr_{11-0}$	*8	
					PC_{14-0} ← $PC_{14,13,12}$ + $caddr_{11-0}$		
Subroutine stack control	CALL	!addr	3	3	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, PC_{13}, PC_{12} PC_{13-0} ← addr, SP ← SP–4	*6	
				4	(SP – 2) ← ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, PC_{14}, PC_{13}, PC_{12} PC_{14} ← 0, PC_{13-0} ← addr, SP ← SP–6		

* **1.** μPD75116H only.

2. The 3 lower bits in the B register are valid only.

Remarks Shading indicates a part compatible with the μPD75117H.

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALLA	!addr1	3	3	(SP – 2) ← ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, PC_{14}, PC_{13}, PC_{12} PC_{14-0} ← addr1, SP ← SP–6	*11	
	CALLF	!faddr	2	2	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, PC_{13}, PC_{12} PC_{13-0} ← 000 + faddr, SP ← SP – 4	*9	
				3	(SP – 2) ← ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, PC_{14}, PC_{13}, PC_{12} PC_{14-0} ← 0000 + faddr, SP ← SP – 6		
	RET		1	3	MBE, RBE, PC_{13}, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4		
					PC_{11-0} ← (SP) (SP + 3) (SP + 2) ×, PC_{14}, PC_{13}, PC_{12} ← (SP + 1) ×, ×, MBE, RBE ← (SP + 4) SP ← SP +6		
	RETS		1	3 + S	MBE, RBE, PC_{13}, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4, then skip unconditionally		Unconditional
					PC_{11-0} ← (SP) (SP + 3) (SP + 2) ×, PC_{14}, PC_{13}, PC_{12} ← (SP + 1) ×, ×, MBE, RBE ← (SP + 4) SP ← SP +6 then skip unconditionally		
	RETI		1	3	PC_{13}, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP +6		
					PC_{11-0} ← (SP) (SP + 3) (SP + 2) ×, PC_{14}, PC_{13}, PC_{12} ← (SP + 1) PSW ← (SP + 4) (SP + 5), SP ← SP +6		
	PUSH	rp	1	1	(SP – 1) (SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← RBS, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1) (SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Interrupt control	EI		2	2	IME (IPS.3) ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IE×××	2	2	IE××× ← 0		

Remarks Shading indicates a part compatible with the μPD75117H.

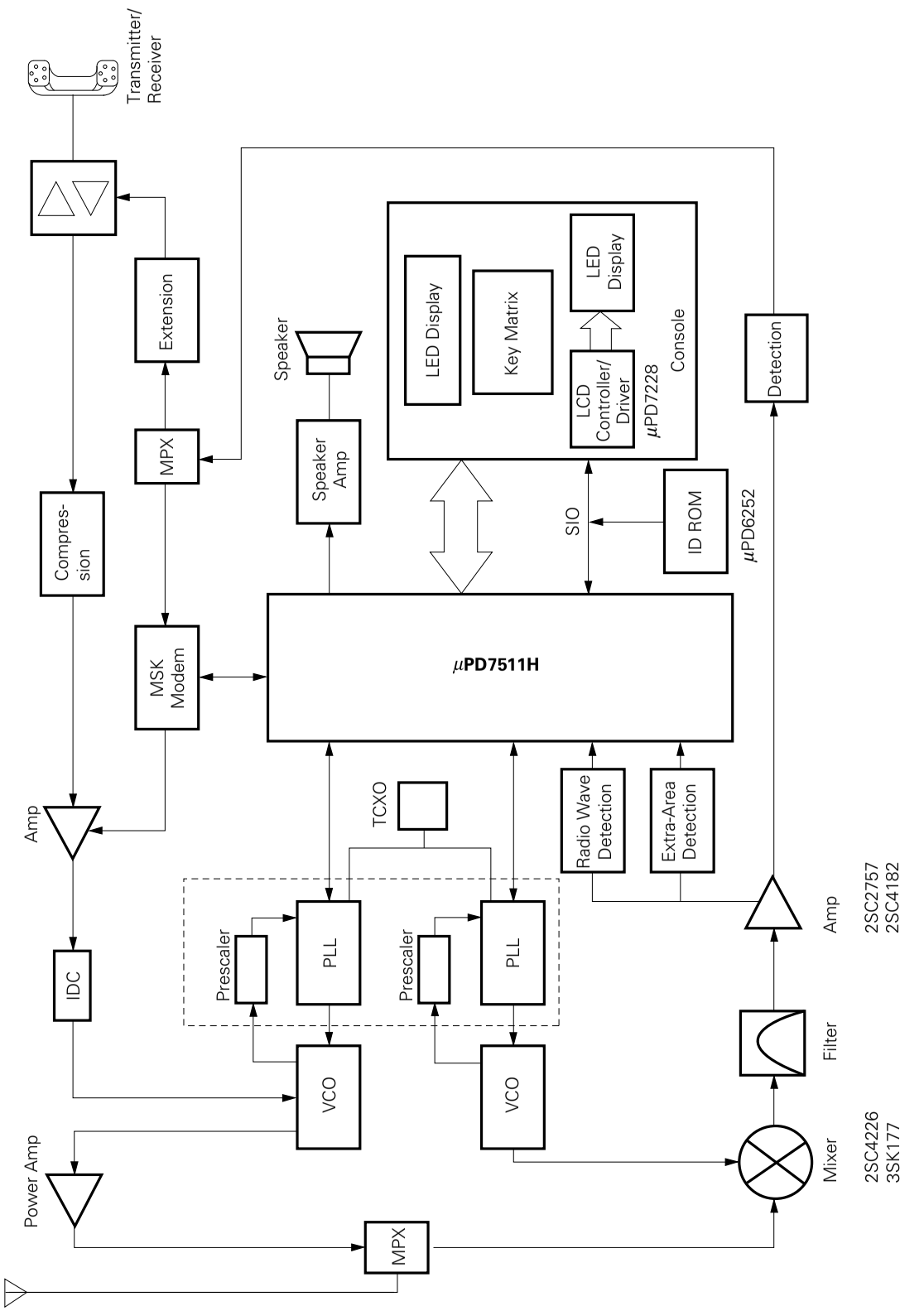
Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Input/output	IN *1	A, PORTn	2	2	A← PORTn (n = 0 to 9, 12 to 14)		
		XA, PORTn	2	2	XA ← PORTn + 1, PORTn (n = 4, 6, 8, 12)		
	OUT *1	PORTn, A	2	2	PORTn ← A (n = 2 to 9, 12 to 14)		
		PORTn, XA	2	2	PORTn + 1, PORTn ← XA (n = 4, 6, 8, 12)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SELL	RBn	2	2	RBS ← n (n = 0 to 3)		
		MBn	2	2	MBS ← n (n = 0, 1, 2, 15)		
	GETI *2	taddr	1	3	• TBR Instruction $PC_{13-0} \leftarrow (taddr)_{5-0} \leftarrow (taddr + 1)$ $PC_{14} \leftarrow 0$	*10	
				4	• TCALL Instruction (SP – 5) (SP – 6) (SP – 3)(SP – 4) ← PC_{14-0} (SP – 2) ← (×, ×, MBE, RBE) $PC_{13-0} \leftarrow (taddr)_{5-0} \leftarrow (taddr + 1)$ SP ← SP – 6 $PC_{14} \leftarrow 0$		
				3	• Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.
			1	3	• TBR Instruction $PC_{13-0} \leftarrow (taddr)_{5-0} \leftarrow (taddr + 1)$ $PC_{14} \leftarrow 0$	*10	
				4	• TCALL Instruction (SP – 5) (SP – 6) (SP – 3)(SP – 4) ← ×, PC_{14-0} (SP – 2) ← ×, ×, MBE, RBE $PC_{13-0} \leftarrow (taddr)_{5-0} \leftarrow (taddr + 1)$ SP ← SP – 6, $PC_{14} \leftarrow 0$		
				3	• Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.

* **1.** When executing the IN/OUT instruction, <MBE = 0> or <MBE = 1, MBS = 15> must be set.
2. The TBR or TCALL instruction is a GETI instruction table definition assembler pseudo-instruction.

Remarks Shading indicates a part compatible with the μPD75117H.

10. APPLICATION EXAMPLE

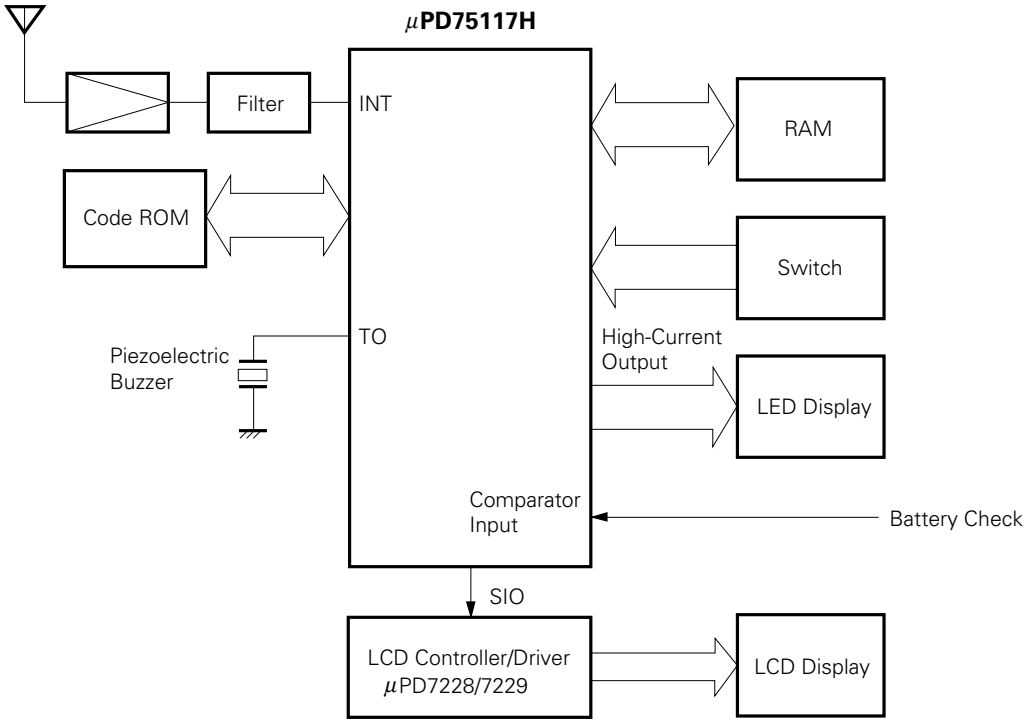
10.1 CORDLESS TELEPHONE (SUBSET)



Legend

IDC : Immediate Deviation Controller, ID ROM : ID (Identification) Code ROM, LCD : Liquid Crystal Display
LED : Light Emitting Diode, MPX : Multiplexer MSK : Minimum Shift Keying
PLL : Phase Locked Loop, SIO : Serial Data Input/Output TCXO : Temperature Compensation Crystal Oscillator
VCO : Voltage Control Oscillator

10.2 DISPLAY PAGER



11. MASK OPTION SELECTION

The μPD75117H has the following mask option.

Pin Function	Mask Option
P12 to P14	• Pull-up resistor (can be specified bit-wise.) • No pull-up resistor (can be specified bit-wise.)

★ 12. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_{I1}	Except ports 12, 13 and 14		–0.3 to V_{DD} +0.3	V
	V_{I2}***1**	Ports 12 to 14	Internal pull-up resistor	–0.3 to V_{DD} +0.3	V
			Open–drain	–0.3 to +7.3	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}	One pin		–15	mA
		All pins		–30	mA
Output current low	I_{OL}***2**	One pin	Peak value	30	mA
			Effective value	15	mA
		Total of ports 0, 2, 12 to 14	Peak value	100	mA
			Effective value	60	mA
		Total of ports 3 to 9	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T_{opt}			–40 to +60	°C
Storage temperature	T_{stg}			–65 to +150	°C

* **1.** When a voltage exceeding 6V is applied to ports 12, 13 and 14, the power supply impedance (pull-up resistor) should be 50KΩ or more.

2. Effective value should be calculated: [Effective value] = [Peak value] × $\sqrt{\text{duty}}$

Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily.

The absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

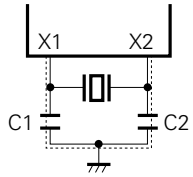
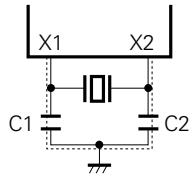
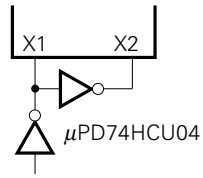
OPERATING VOLTAGE RANGE

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
CPU		– 40	+ 60	°C
Programmable threshold port (comparator input)		– 10	+ 60	°C
Other hardware		– 40	+ 60	°C

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
Input/output capacitance	C_{IO}				15	pF

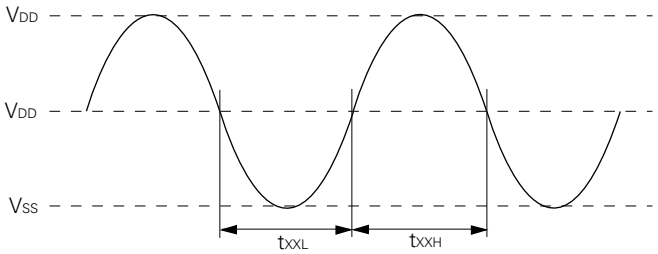
OSCILLATION CIRCUIT CHARACTERISTICS (Ta = –40 to +60 °C, V_{DD} = 1.8 to 5.5 V)

RESONATOR	RECOMMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
*1 Ceramic resonator		Oscillator frequency (f_{XX}) *2		2.0		5.0 *4	MHz
		Oscillation stabilization time *3	After V_{DD} reaches MIN. of oscillation voltage range			4	ms
*1 Crystal resonator		Oscillator frequency (f_{XX}) *2		2.0	4.19	5.0 *4	MHz
		Oscillation stabilization time *3	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
*5 External clock		X1 input frequency (f_X) *2	V_{DD} = 2.7 to 5.5 V	2.0		5.0 *4	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		100		250	ns

* **1.** When using in V_{DD} < 2.7 V, the X2 pin oscillation waveform duty should be set within the range between 40% and 60%.

$$\text{Duty} = \frac{t_{XXL} \text{ (or } t_{XXH})}{t_{XXL} + t_{XXH}} \times 100$$

X2 Oscillation Waveform



2. Oscillator frequency and X1 input frequency indicate oscillation circuit characteristics only. See AC CHARACTERISTICS for instruction execution time.

3. The oscillation stabilization time is the time required for oscillation to stabilize after V_{DD} reaches MIN. of oscillation voltage range or the STOP mode is released.

4. When the oscillator frequency is 4.19 MHz < f_{XX} ≤ 5.0 MHz, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, one machine cycle is less than 0.95 μs and the rated MIN. value of 0.95 μs is not observed.

5. The external clock cannot be used in V_{DD} < 2.7 V.

Note When the clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}. Do not connect to a ground pattern carrying a high current.**
- **A signal should be not taken from the oscillator.**

RECOMMENDED OSCILLATION CIRCUIT CONSTANT

RECOMMENDED CERAMIC RESONATOR (Ta = –40 to +60 °C)

MANUFACTURER	PRODUCT NAME	FREQUENCY (MHz)	EXTERNAL CAPACITANCE (pF)		OSCILLATION VOLTAGE RANGE [V]	
			C1	C2	MIN.	MAX.
Kyocera	KBR–2.0MS	2.00	47	47	1.8	5.5
	PBRC 2.00A					
	KBR–4.0MSA	4.00	33	33		
	PBRC 4.00A					
	KBR–4.0MKS		lincorporated	lincorporated		
	KBR–4.0MWS					
	KBR–4.19MSA	4.19	33	33		
	PBRC 4.19A					
	KBR–4.19MKS		lincorporated	lincorporated		
	KBR–4.19MWS					
	KBR–5.0MSA	5.00	33	33		
	PBRC 5.00A					
	KBR–5.0MKS		lincorporated	lincorporated		
	KBR–5.0MWS					

DC CHARACTERISTICS (Ta = –40 to +60 °C, V_{DD} = 1.8 to 5.5 V)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Other than below		V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0,1,TI0, 1, $\overline{RESET}$			0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 12 to 14	Internal pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0.8 V_{DD}		V_{DD}	V
			N-ch open–drain	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		6	V
				V_{DD} = 1.8 to 5.5 V	0.8 V_{DD}		6	V
	V_{IH4}	X1, X2		V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	V_{DD} – 0.3		V_{DD}	V
Input voltage low	V_{IL1}	Other than below		V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.2 V_{DD}	V
	V_{IL2}	Ports 0,1,TI0, 1, $\overline{RESET}$			0		0.2 V_{DD}	V
	V_{IL3}	X1, X2		V_{DD} = 2.7 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 2.7 V	0		0.25	V
Output voltage high	V_{OH}	I_{OH} = –1 mA		V_{DD} = 4.5 to 5.5 V	V_{DD} – 1.0			V
				V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.8			V
		I_{OH} = –100 μA		V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5			V
				V_{DD} = 1.8 to 2.7 V	V_{DD} – 0.2			V
Output voltage low	V_{OL}	Ports 0, 2, 4 to 8	I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V		0.35	2.0	V
			I_{OL} = 1.6 mA	V_{DD} = 2.7 to 5.5 V			0.4	V
			I_{OL} = 400 μA	V_{DD} = 2.7 to 5.5 V			0.5	V
			I_{OL} = 100 μA	V_{DD} = 1.8 to 5.5 V			0.3	V
		Ports 3, 9	I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V		0.35	2.0	V
			I_{OL} = 10 mA	V_{DD} = 2.7 to 5.5 V		0.3	1.0	V
			I_{OL} = 1.6 mA	V_{DD} = 2.7 to 5.5 V			0.4	V
			I_{OL} = 400 μA	V_{DD} = 2.7 to 5.5 V			0.5	V
			I_{OL} = 100 μA	V_{DD} = 1.8 to 5.5 V			0.3	V
		Ports 12 to 14	I_{OL} = 10 mA	V_{DD} = 4.5 to 5.5 V		0.35	2.0	V
			I_{OL} = 1.6 mA	V_{DD} = 2.7 to 5.5 V			0.4	V
			I_{OL} = 400 μA	V_{DD} = 2.7 to 5.5 V			0.5	V
			I_{OL} = 100 μA	V_{DD} = 1.8 to 5.5 V			0.3	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below				3	μA
	I_{LIH2}		X1, X2				20	μA
	I_{LIH3}	V_{IV} = 6 V	Ports 12 to 14 (open-drain)				15	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below				–3	μA
	I_{LIL2}		X1, X2				–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below				3	μA
	I_{LOH2}	V_{OUT} = 6 V	Ports 12 to 14 (open-drain)				15	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V					–3	μA
Internal pull-up resistor (mask option)	R_L	Ports 12 to 14			10	35	60	kΩ

DC CHARACTERISTICS (Ta = –40 to +60 °C, V_{DD} = 1.8 to 5.5 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Supply current*1	I_{DD1}	4.19 MHz Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5 V ±10 % *2		3.0	9.0	mA
			V_{DD} = 3 V ±10 % *2		1.6	4.8	mA
			V_{DD} = 2 V ±10 % *3		0.6	1.8	mA
	I_{DD2}	HALT mode	V_{DD} = 5 V ±10 %		0.7	2.1	mA
			V_{DD} = 3 V ±10 %		280	860	μA
			V_{DD} = 2 V ±10 %		120	360	μA
	I_{DD3}	STOP mode	V_{DD} = 5 V ±10 %		0.2	50	μA
			V_{DD} = 3 V ±10 %		0.1	20	μA
			V_{DD} = 2 V ±10 %		0.05	10	μA

* **1.** Excluding current flowing in the internal pull-up resistors and comparator circuit.
2. When the processor clock control register (PCC) is set to 0011 for operation in the high-speed mode.
3. When the PCC register is set to 0010 for operation in the low-speed mode.

COMPARATOR CHARACTERISTICS (Ta = –10 to +60 °C*, V_{DD} = 1.8 to 5.5 V)

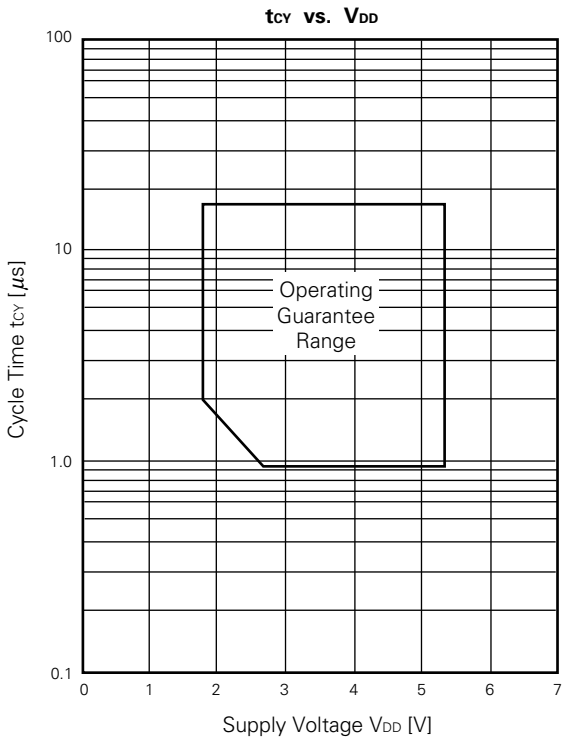
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Compare accuracy	V_{ACOMP}					±100	mV
Threshold voltage	V_{TH}			0		V_{DD}	V
PTH input voltage	V_{IPTH}			0		V_{DD}	V
Comparator circuit current consumption		PTHM7 set to "1"	V_{DD} = 5.0 V		0.7		mA
			V_{DD} = 3.0 V		0.3		mA
			V_{DD} = 2.0 V		0.1		mA

* The comparator cannot operate in the range of Ta = –40 to –10 °C. It must be used within the range of Ta = –10 to +60 °C.

AC CHARACTERISTICS (Ta = –40 to +60 °C, V_{DD} = 1.8 to 5.5 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time* (Minimum instruction execution time = 1 machine cycle)	t_{CY}	V_{DD} = 2.7 to 5.5 V		0.95		16	μs
				1.91		16	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1	MHz
				0		275	kHz
TI0, TI1 input high/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 to 5.5 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
$\overline{SCK}$ high/low-level width	t_{KH}, t_{KL}	V_{DD} = 4.5 to 5.5 V	Input	0.4			μs
			Output	$t_{KCY}/2 - 50$			ns
			Input	1.6			μs
			Output	$t_{KCY}/2 - 150$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK}			100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO}	V_{DD} = 4.5 to 5.5 V		0		300	ns
				0		1000	ns
INT0 to INT4 high/low-level width	t_{INTH}, t_{INTL}			5			μs
$\overline{RESET}$ low-level width	t_{RSL}			5			μs

* The CPU clock (Φ) cycle time is determined by the oscillator frequency of the connected resonator and the setting of the processor clock control register (PCC). The graph on the right shows the characteristic for cycle time t_{CY} supply current V_{DD} during system clock operation.



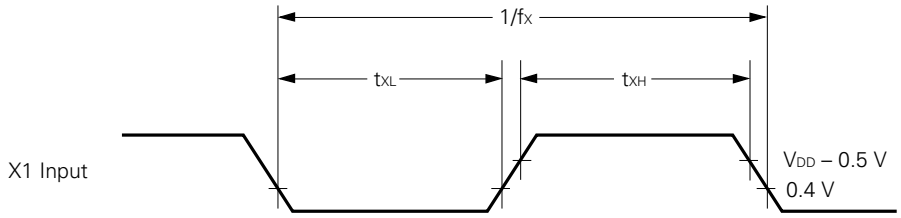
AC Timing Test Point (Except ports 0, 1, TI0, TI1, X1, X2, $\overline{\text{RESET}}$)

(1) V_{DD} = 2.7 to 5.5 V

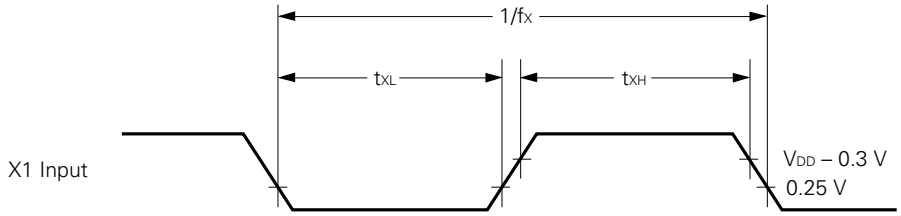
(2) V_{DD} = 1.8 to 2.7 V

Clock Timing

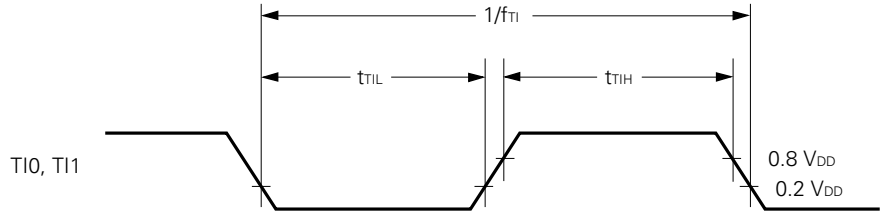
(1) V_{DD} = 2.7 to 5.5 V



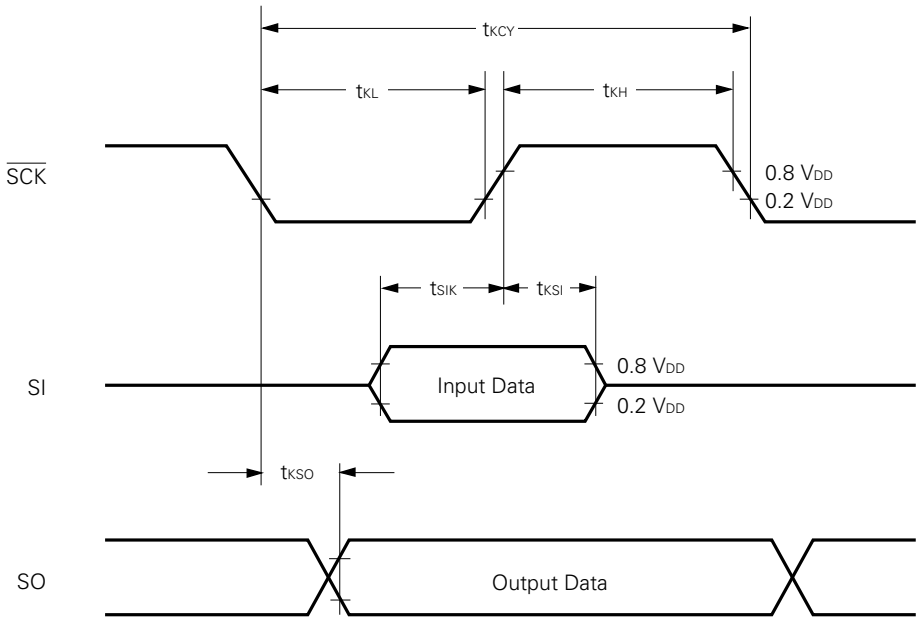
(2) V_{DD} = 1.8 to 2.7 V



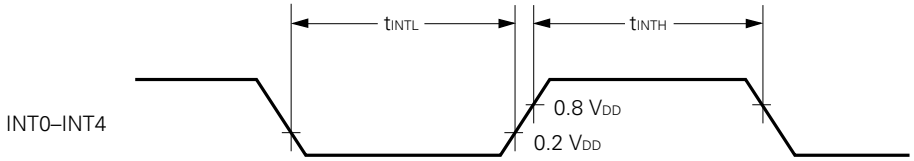
TI0,TI1 Input Timing



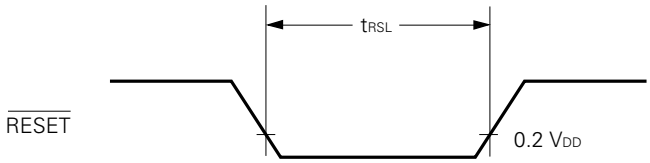
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



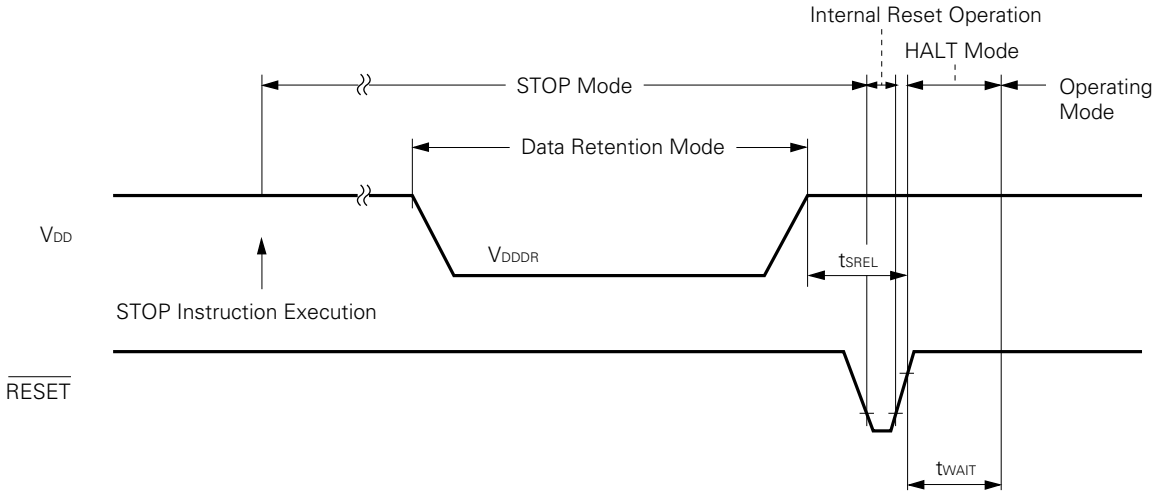
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +60 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.05	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time*2	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_{XX}$		ms
		Release by interrupt request		*3		ms

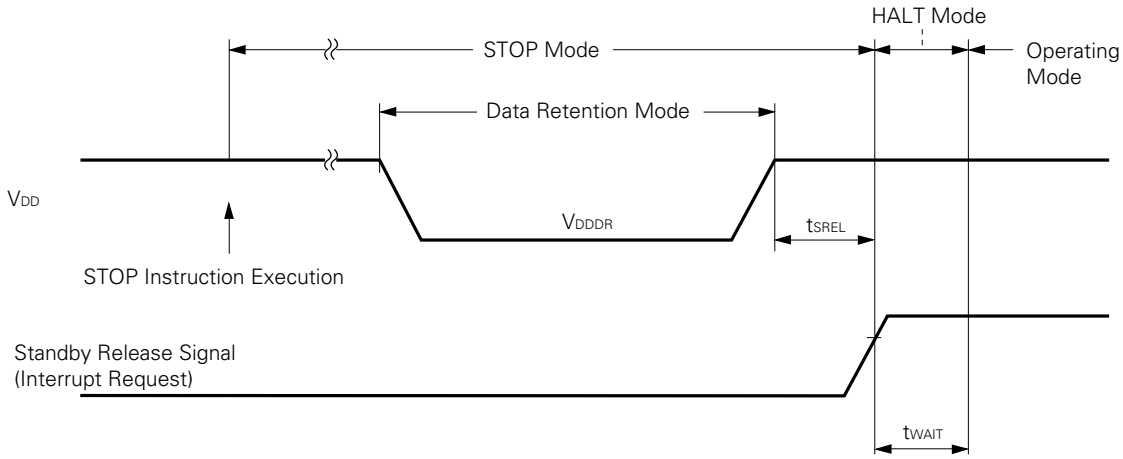
* 1. Excluding current flowing in the internal pull-up resistors and comparator circuit.
2. The oscillation stabilization wait time is the time during which CPU operation is stopped to prevent unstable operation when oscillation is started.
3. Depends on the basic interval timer mode register (BTM) setting (see table below).

BTM3	BTM2	BTM1	BTM0	WAIT TIME (Figures in parentheses are for operation at f_{XX} = 4.19 MHz)
—	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{RESET}$)

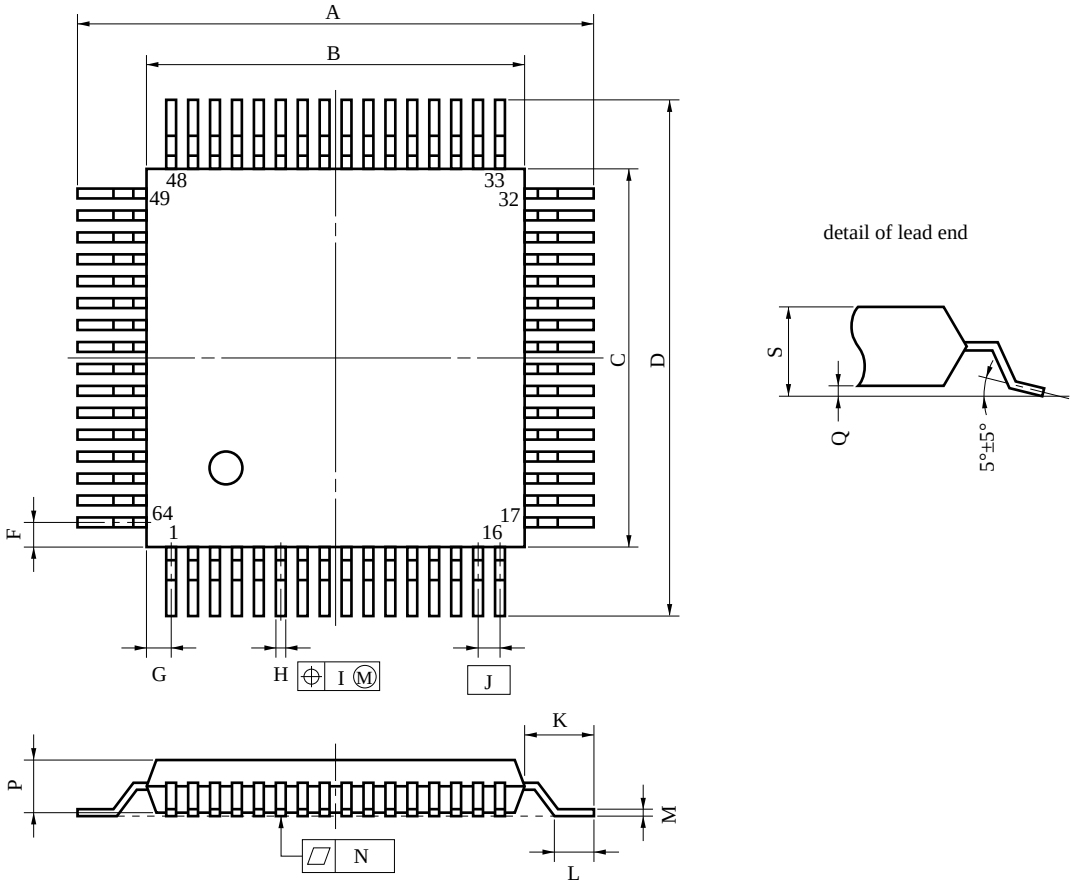


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



13. PACKAGE INFORMATION

64-PIN PLASTIC QFP (□14)



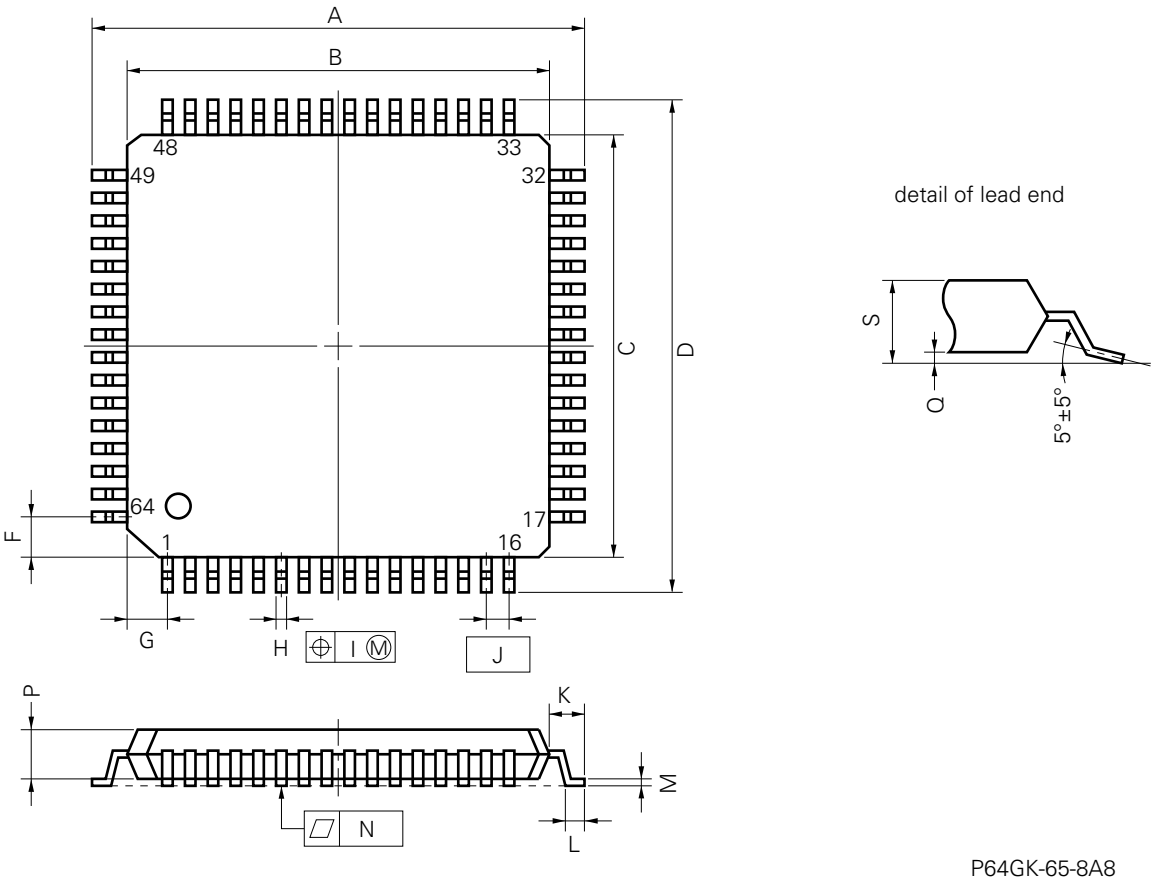
P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

★ **64-PIN PLASTIC QFP (□12)**



P64GK-65-8A8

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	1.4	0.055
Q	0.1±0.1	0.004±0.004
S	1.7 MAX.	0.067 MAX.

14. RECOMMENDED SOLDERING CONDITIONS ★

The μPD75117H should be soldered and mounted under the conditions recommended in the table below.

For details of recommended conditions, refer to **the information document "Semiconductor Device Mount Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 14-1 Surface Mount Type Soldering Conditions

(1) μPD75117HGC: 64-Pin Plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature : 230 °C, Duration : 30 sec. max. (at 210 °C or avove), Number of times : twice <Points to note> Flux washing by the water after the first reflow should be avoided.	IR30-00-2
VPS	Package peak temperature : 215 °C, Duration : 40 sec. max. (at 200 °C or above), Number of times : twice <Points to note> Flux washing by the water after the first reflow should be avoided.	VP15-00-2
Wave soldering	Solder bath temperature : 260 °C max., Duration : 10 sec. max., Number of times : once, Preheating temperature : 120 °C max. (package surface temperature)	WX60-00-1
Pin part heating	Pin part temperature : 300 °C max., Duration : 3 sec. max. (per device side)	—

(2) μPD75117GK: 64-Pin Plastic QFP (□12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature : 230 °C, Duration : 30 sec. max. (at 210 °C or avove), Number of times : twice, Time limit: 7 days* (thereafter 10 hours prebaking at 125 ˚C required) <Points to note> Flux washing by the water after the first reflow should be avoided.	IR35-107-2
VPS	Package peak temperature : 215 °C, Duration : 40 sec. max. (at 200 °C or above), Number of times : twice, Time limit: 7 days* (thereafter 10 hours prebaking at 125 ˚C required) <Points to note> Flux washing by the water after the first reflow should be avoided.	VP15-107-2
Pin part heating	Pin part temperature : 300 °C max., Duration : 3 sec. max. (per device side)	—

***** For the storage period after dry-pack decupsulation storage conditions are max. 25 ˚C, 65 % RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

★ APPENDIX A. FUNCTIONAL DIFFERENCES AMONG μPD751×× SERIES PRODUCTS

Item \ Product Name	μPD75104/106/108/112/116	μPD75104A/108A	μPD75108F/112F/116F
ROM (byte)	4K/6K/8K/12K/16K (Mask ROM)	4K/8K (Mask ROM)	8K/12K/16K (Mask ROM)
RAM (× 4 bits)	320/320/512/512/512	320/512	512
Instruction set	75X High-End		
I/O port: Total	58		
I/O port: CMOS input	10	10 (Pull-up resistor mask option : 4)	10
I/O port: CMOS input/output	32 (LED direct drive capability ***2**)	32 (Pull-up resistor mask option : 24, LED direct drive capability)	32 (LED direct drive capability ***2**)
I/O port: N-ch open-drain input/output	12 (LED direct drive capability ***2**)		
I/O port: N-ch open-drain input/output: Withstand voltage	+12 V		+10 V
I/O port: N-ch open-drain input/output: Pull-up resistor	Can be incorporated by mask option		
I/O port: Analog input	4 (4-bit precision)		
Power-on reset circuit / Power-on flag	On-chip (Mask option)		None
Operating voltage	2.7 to 6.0 V		2.7 to 5.0 V (Ta = –40 to +50 °C) 2.8 to 5.0 V
Operating temperature range	–40 to +85 °C		–40 to +60 °C
Minimum instruction execution time	0.95 μs (operating at 4.5 to 6.0 V) 3.8 μs (operating at 2.7 V)		0.95 μs (operating at 4.5 to 5.0 V) 1.91 μs (operating at 2.7V)
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic QFP (□14 mm) (Resin thick 2.55 mm) • 64-pin plastic QFP (□14 mm) (Resin thick 1.5 mm)	• 64-pin plastic QFP (14 × 20 mm)

***** **1.** 75X High-End can also be used by means of the 16K-byte mode/24K-byte mode switching function.

2. For details, refer to the electrical specifications in each data sheet.

μPD75116H/117H	μPD75P108B	μPD75P116	μPD75P117H
16K/24K (Mask ROM)	8K (One-time PROM, EPROM)	8K (One-time PROM)	24K (One-time PROM)
768	512		768
75X High-End/Extended High-End	75X High-End		75X Extended High-End***1**
58			
10			
32 (LED direct drive capability ***2**)			
12 (LED direct drive capability ***2**)			
+6 V	+12 V		+6 V
Can be incorporated by mask option	None		
4 (4-bit precision)			
None			
1.8 to 5.5 V	2.7 to 6.0 V	5 V ±10 %	1.8 to 5.5 V
–40 to +60 °C	–40 to +85 °C		–40 to +60 °C
0.95 μs (operating at 2.7 V) 1.91 μs (operating at 1.8 V)	0.95 μs (operating at 4.5 to 6.0 V) 3.8 μs (operating at 2.7 V)	0.95 μs (operating at 4.75 to 5.5 V)	0.95 μs (operating at 2.7 V) 1.91 μs (operating at 1.8 V)
• 64-pin plastic QFP (□12 mm) • 64-pin plastic QFP (□14 mm) (Resin thick 2.55 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin ceramic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic QFP (□12 mm) • 64-pin plastic QFP (□14 mm) (Resin thick 2.55 mm)

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75116H/75117H.

Hardware	IE-75000-R***1** IE-75001-R	75X series in-circuit emulator
	IE-75000-R-EM***2**	Emulation board for the IE-75000-R or IE-75001-R
	EP-75108AGC-R EV-9200G-64	Emulation probe for the μPD75116HGC/75117HGC. A 64-pin conversion socket (EV-9200G-64) is also provided.
	EP-75117GK-R EV-9500G-64	Emulation probe for the μPD75116HGK/75117HGK. A 64-pin conversion socket (EV-9500G-64) is also provided.
	PG-1500	PROM programmer
	PA-75P117GC	PROM programmer adapter for the μPD75P117HGC, connected to the PG-1500.
	PA-75P117GK	PROM programmer adapter for the μPD75P117HGK, connected to the PG-1500.
Software	IE control program	Host machines • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A***3**) • IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 controller	
	RA75X relocatable assembler	

* **1.** Maintenance product
2. Not incorporated in the IE-75001-R.
3. A task swapping function is provided in Ver. 5.00/5.00A, but this function cannot be used with this software.

APPENDIX C. RELATED DOCUMENTS ★

Device Related Documents

Document Name	Document Number
User's Manual	IEM–1340
Instruction Application Table	—
75X Series Selection Guide	IF–1027

Development Tools Documents

Document Name			Document Number
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU–1455
	IE-75000-R-EM User's Manual		EEU–1294
	EP-75117GK-R User's Manual		EEU–1318
	PG-1500 User's Manual		EEU–1335
Software	RA75X Assembler Package User's Manual	Operation Volume	EEU–1346
		Language Volume	EEU–1343
	PG-1500 Controller User's Manual		EEU–1291

Other Documents

Document Name	Document Number
Package Manual	IEI–1213
Surface Mount Technology Manual	IEI–1207
Quality grade on NEC Semiconductor Devices	IEI–1209
NEC Semiconductor Device Reliability & Quality Control	—
Electrostatic Discharge (ESD) Test	—
Semiconductor Devices Quality Guide Guarantee Guide	MEI–1202
Microcomputer Related Products Guide Other Manufacturers Volume	—

Note The information in these related documents is subject to change without notice. For design purpose, etc., be sure to use the latest ones.

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