NEC

MOS INTEGRATED CIRCUIT
μPD75P117H

4-BIT SINGLE CHIP MICROCOMPUTER

The μPD75P117H is the same product as the μPD75117H except that it contains one-time PROM (programmable read-only memory) in place of mask ROM contained in the μPD75117H.

The μPD75P117H, which can be programmed by the user, is appropriate for small production or preproduction at system development.

For detailed information on the μPD75P117H, refer to the following user's manual:

μPD75117H User's Manual: IEU-799

FEATURES

- Compatible with the μPD75117H
- Contains 16K-byte mode/24K-byte mode change function
- Memory capacity
  - Program memory (PROM) : 24448 × 8 bits
  - Data memory (RAM) : 768 × 4 bits
- Can operate in the same supply voltage range (1.8 to 5.5 V) as the mask version μPD75117H

Caution

Internal pull-up resistors provided by specifying mask options are not contained.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD75P117HGC-AB8	64-pin plastic QFP (14 × 14 mm)	One-time PROM
GK-8A8	64-pin plastic QFP (12 × 12 mm)	

QUALITY GRADE

Part Number	Package	Quality Grade
μPD75P117HGC-AB8	64-pin plastic QFP (14 × 14 mm)	Standard
GK-8A8	64-pin plastic QFP (12 × 12 mm)	

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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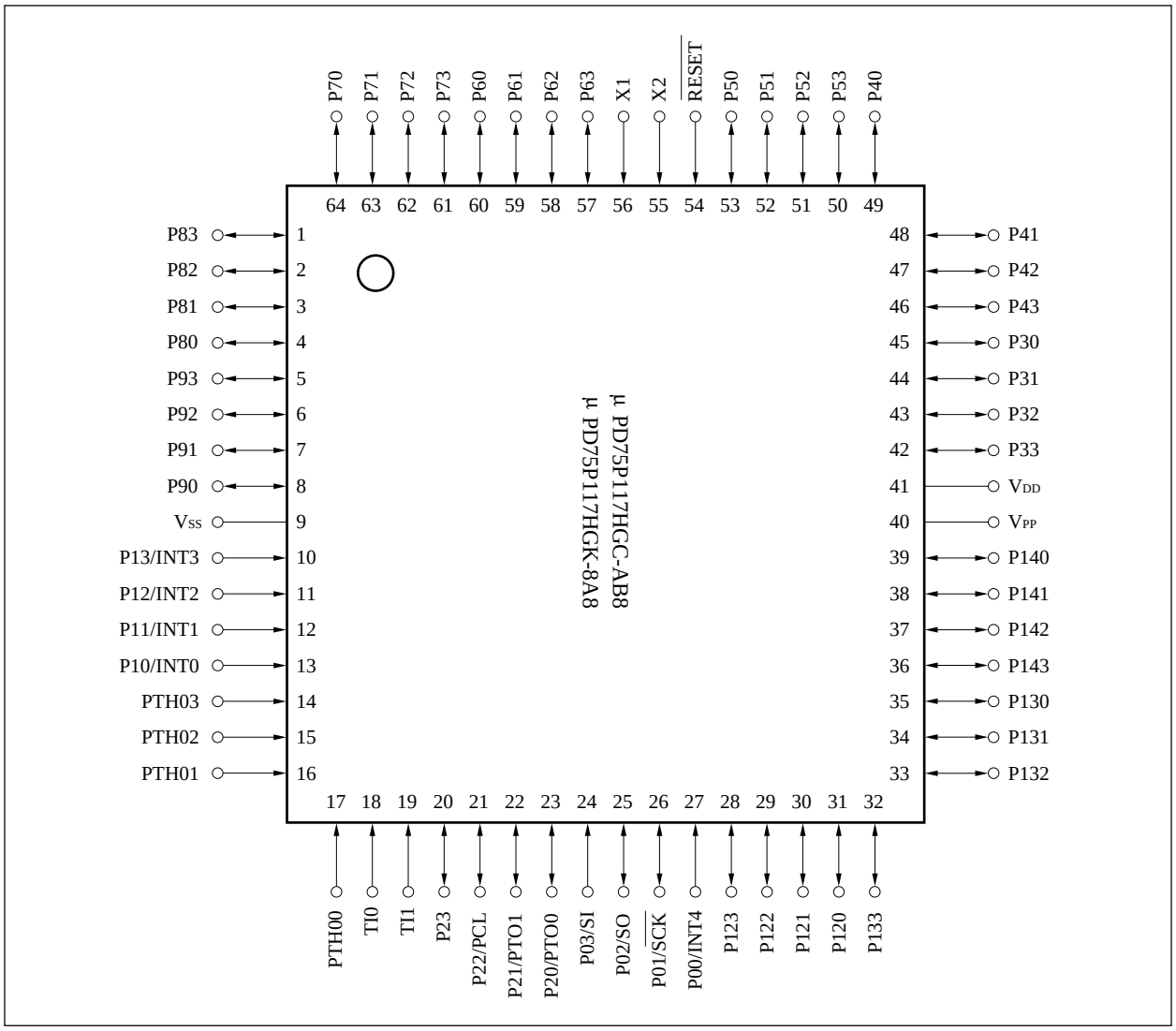
PIN CONFIGURATION (Top View)

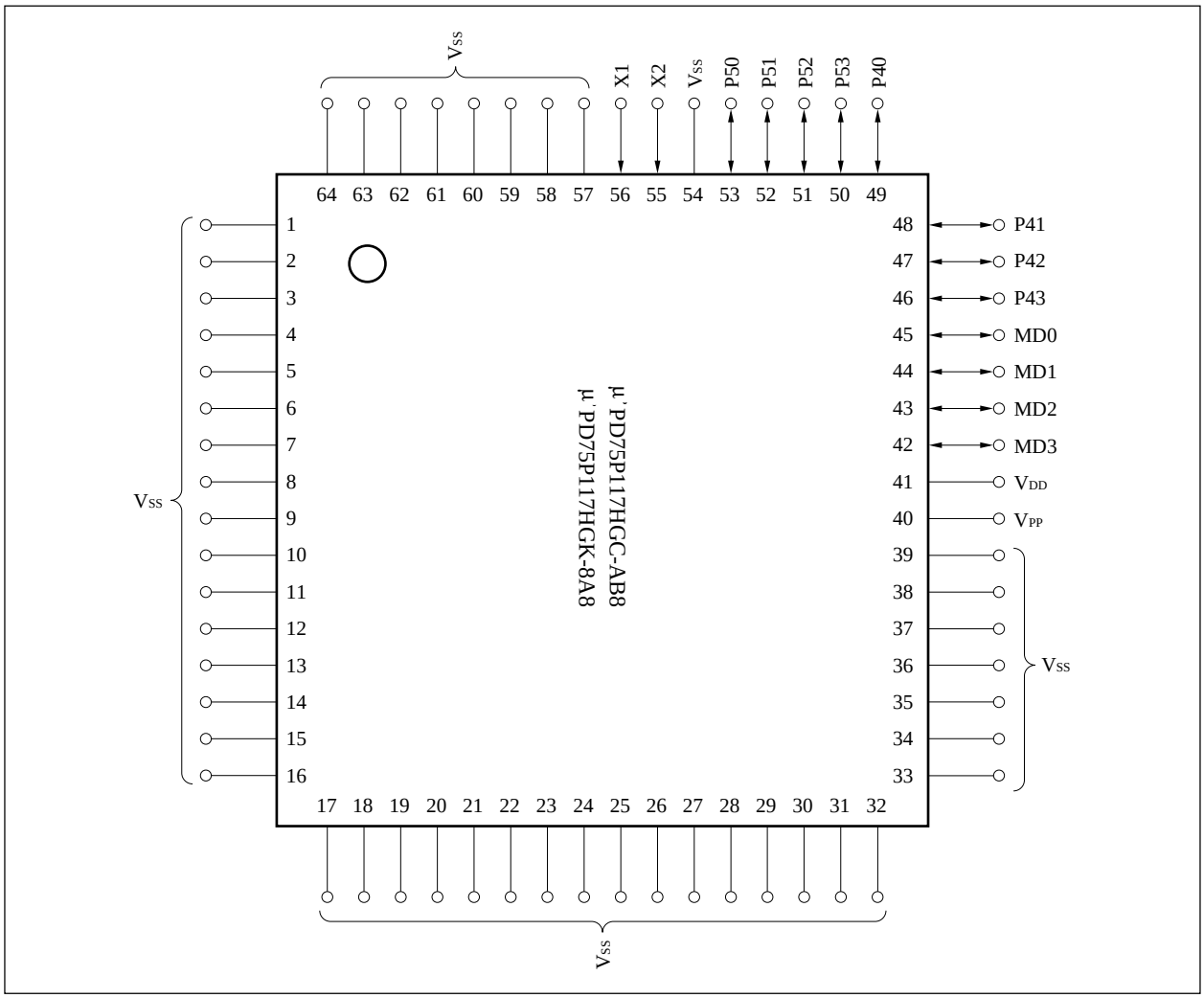
Normal Operation



Caution

Connect the V_{PP} pin directly to the V_{DD} pin.

PROM Programming Mode



Caution

V_{SS}: Connect the pin to V_{SS} pin via a pull-down resistor.

PIN IDENTIFICATION

P00 - P03 : Port 0
P10 - P13 : Port 1
P20 - P23 : Port 2
P30 - P33 : Port 3
P40 - P43 : Port 4
P50 - P53 : Port 5
P60 - P63 : Port 6
P70 - P73 : Port 7
P80 - P83 : Port 8
P90 - P93 : Port 9
P120 - P123: Port 12
P130 - P133: Port 13
P140 - P143: Port 14
TI0, TI1 : Timer Input
PTO0, PTO1: Timer Output

PCL : Clock Output
$\overline{SCK}$: Serial Clock Input/Output
SO : Serial Output
SI : Serial Input
PTH00 - PTH03: Comparator Input
INT0, INT1 : External Vectored Interrupt Input
INT2, INT3 : External Test Input
INT4 : External Vectored Interrupt Input
X1, X2 : System Clock Oscillation
$\overline{RESET}$: Reset Input
MD0 - MD3 : Write/Verify Mode Select Pin
V_{PP} : Programming Power Supply
V_{DD} : Power Supply
V_{SS} : Ground

PRODUCT OUTLINE

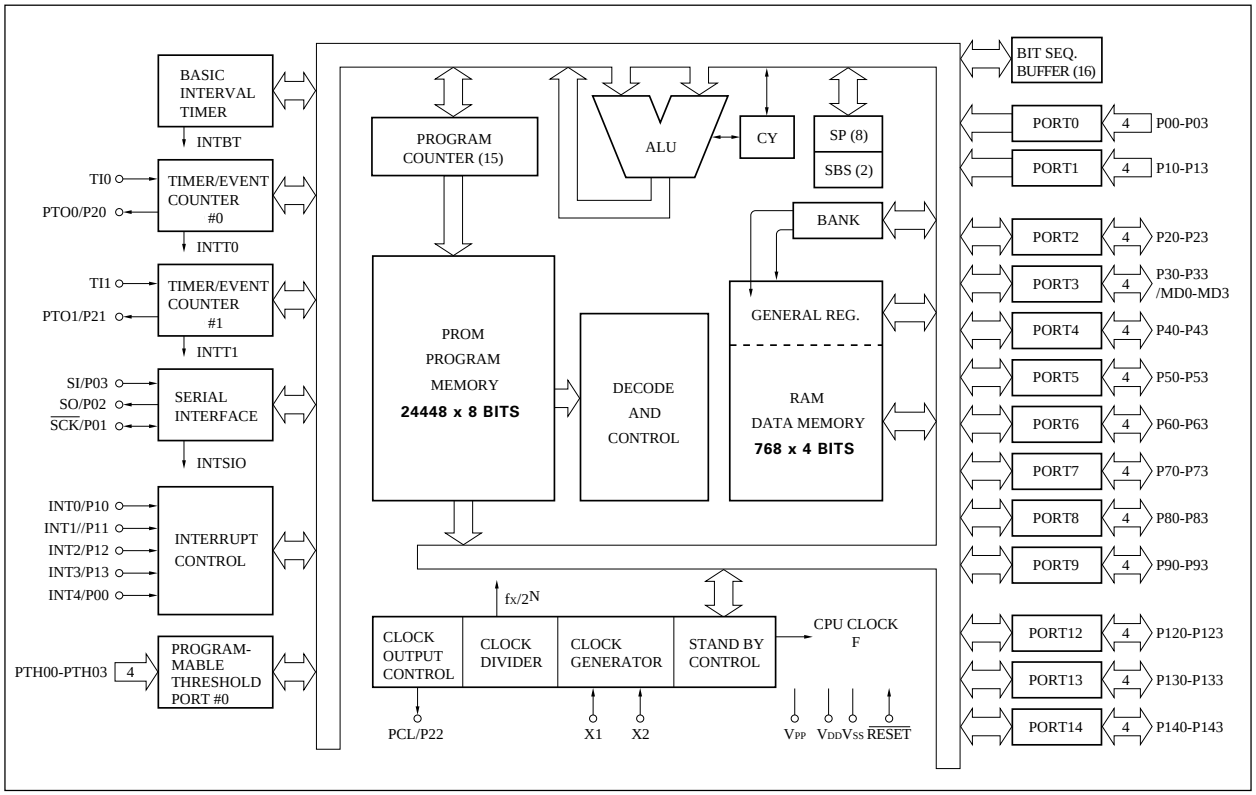
Item		Specifications
Number of instructions		43
Minimum instruction execution time		0.95 μs, 1.91 μs, 15.3 μs (at 4.19 MHz) One of three times can be selected
Internal memory	ROM	24448 × 8 bits
	RAM	768 × 4 bits
General register		4 bits × 8 × 4 banks (memory mapping)
I/O ports		Total: 58 • CMOS input pin : 10 • CMOS input/output pin : 32 (can drive LEDs directly Note 1) • N-ch open-drain input/output pin : 12 (can drive LEDs directly Note 2) • Comparator input pin (4-bit accuracy): 4
Timer/counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (applicable to watchdog timer)
Serial interface		• 8 bits • LSB or MSB can be selected as the top bit of data transfer • Two transfer modes (transmission and reception mode and reception-only mode)
Vectored interrupt		• External: 3 • Internal : 4
Test input		• External: 2
Standby function		STOP/HALT mode
Instruction set		• Diversified bit manipulation instructions (set, reset, test, Boolean operations) • 8-bit data transfer, comparison, operation, and increment and decrement instructions • 1-byte relative branch instruction • GETI instruction to enable any 2-byte or 3-byte instruction to be executed as 1-byte instruction
Others		Contains bit manipulation memory (bit sequential buffer: 16 bits)
Package		• 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic QFP (12 × 12 mm)

Notes

1. V_{DD} = 5 V, I_{OL} = 15 mA

2. V_{DD} = 5 V, I_{OL} = 10 mA

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTION

1.1 Port Pins

Pin name	Input/Output	Dual function pin	Function	8-bit I/O	When reset	Input/output circuit type Note 1
P00	Input	INT4	4-bit input port (PORT0)	×	Input	Ⓑ
P01	Input/Output	$\overline{SCK}$				Ⓕ
P02	Input/Output	SO				E
P03	Input	SI				Ⓑ
P10	Input	INT0	4-bit input port (PORT1)		Input	Ⓑ
P11		INT1				
P12		INT2				
P13		INT3				
P20	Input/Output	PTO0	4-bit input/output port (PORT2) Note 2	×	Input	E
P21		PTO1				
P22		PCL				
P23		–				
P30 to P33	Input/Output	MD0 to MD3	Programmable 4-bit input/output port (PORT3) Input or output mode can be set bit-wise. Note 2		Input	E
P40 to P43	Input/Output	–	4-bit input/output port (PORT4) Data input/output pins (lower four bits) in program memory (PROM) write/verify mode. Note 2	○	Input	E
P50 to P53	Input/Output	–	4-bit input/output port (PORT5) Data input/output pins (higher four bits) in program memory (PROM) write/verify mode. Note 2		Input	E
P60 to P63	Input/Output	–	Programmable 4-bit input/output port (PORT6) Input or output mode can be set bit-wise. Note 2	○	Input	E
P70 to P73	Input/Output	–	4-bit input/output port (PORT7) Note 2		Input	E
P80 to P83	Input/Output	–	4-bit input/output port (PORT8) Note 2	○	Input	E
P90 to P93	Input/Output	–	4-bit input/output port (PORT9) Note 2		Input	E
P120 to P123	Input/Output	–	N-ch open-drain 4-bit input/output port (PORT12). Breakdown voltage +6 V. Note 3	○	Input	M - A
P130 to P133	Input/Output	–	N-ch open-drain 4-bit input/output port (PORT13). Breakdown voltage +6 V. Note 3		Input	M - A
P140 to P143	Input/Output	–	N-ch open-drain 4-bit input/output port (PORT14). Breakdown voltage +6 V. Note 3	–	Input	M - A

Notes

1. Circled letters indicate Schmitt trigger inputs.

2. Can drive LEDs directly (V_{DD} = 5 V, I_{OL} = 15 mA)

3. Can drive LEDs directly (V_{DD} = 5 V, I_{OL} = 10 mA)

1.2 Pins Other than Port Pins

Pin name	Input/Output	Dual function pin	Function	When reset	Input/output circuit type Note 1
PTH00 to PTH03	Input	–	Threshold voltage variable 4-bit analog input port.		N
TI0	Input	–	External event pulse input to timer/event counter or edge detection vectored interrupt input. 1-bit input is also enabled.		(B)
TI1					
PTO0	Input/Output	P20	Timer/event counter output.	Input	E
PTO1		P21			
$\overline{SCK}$	Input/Output	P01	Serial clock input/output.	Input	(F)
SO	Input/Output	P02	Serial data output.	Input	E
SI	Input	P03	Serial data input.	Input	(B)
INT4	Input	P00	Edge detection vectored interrupt input (detection of either rising or falling edge).		(B)
INT0	Input	P10	Edge detection vectored interrupt input (detection edge can be selected).		(B)
INT1		P11			
INT2	Input	P12	Edge detection testable input (detection of rising edge).		(B)
INT3		P13			
PCL	Input/Output	P22	Clock output.	Input	E
X1, X2	Input	–	System clock oscillation crystal or ceramic input. To use external clock, input it to X1 and its inverted phase to X2.		
$\overline{RESET}$	Input	–	System reset input (active low).		(B)
MD0 to MD3	Input/Output	P30 to P33	Mode selection in program memory (PROM) write/verify mode.	Input	E
V_{DD}	–	–	Positive power supply. +6 V is applied in PROM write/verify mode.		
V_{SS}	–	–	GND potential.		
V_{PP} Note 2	–	–	Program voltage application in program memory (PROM) write/verify mode. Connect the pin directly to V_{DD} at normal operation. Apply +12.5 V in PROM write/verify mode.		

Notes

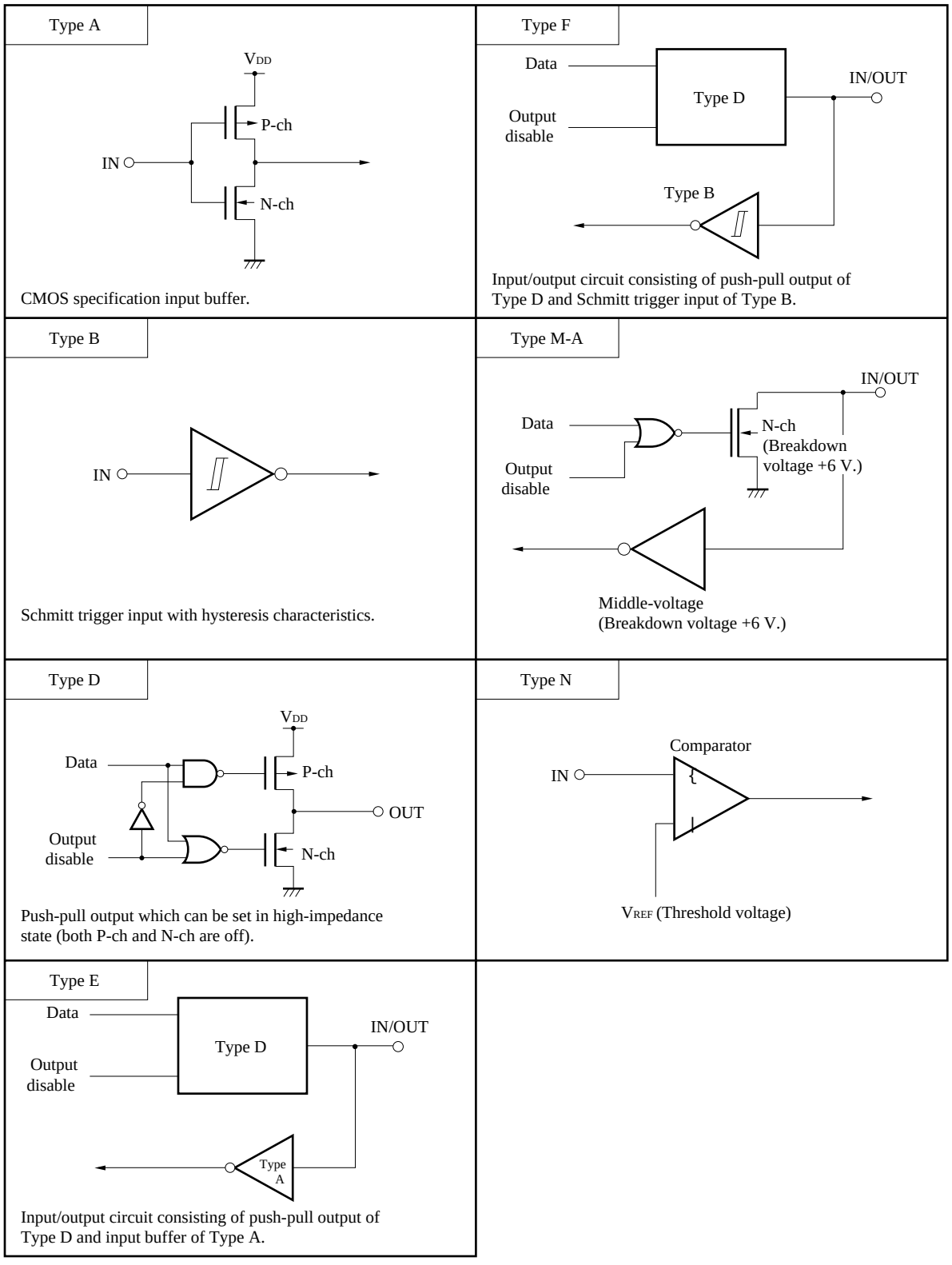
1. Circled letters indicate Schmitt trigger inputs.

2. If the V_{PP} pin is not connected directly to V_{DD} during the normal operation, normal operation is not performed.

1.3 Pin Input/Output Circuits

The pin input/output circuits of the μPD75P117H are shown schematically.

Fig. 1-1 Pin input/output circuit list



1.4 Recommended Connection for Unused Pins

Pin	Recommended Connection
PTH00 to PTH03	Connect to V_{SS} or V_{DD}
TI0	
TI1	
P00	Connect to V_{SS}
P01 to P03	Connect to V_{SS} or V_{DD}
P10 to P13	Connect to V_{SS}
P20 to P23	Input state: Connect to V_{SS} or V_{DD}
P30 to P33	Output state: No connection required
P40 to P43	
P50 to P53	
P60 to P63	
P70 to P73	
P80 to P83	
P90 to P93	
P120 to P123	
P130 to P133	
P140 to P143	
V_{PP}	Connect directly to V_{DD}

2. DIFFERENCES BETWEEN MASK PRODUCTS (μPD75116H, 75117H) AND PROM PRODUCT (μPD75P117H)

The μPD75P117H is a product containing one-time PROM (programmable read-only memory) in place of the program memory of the μPD75116H, 75117H containing mask ROM. Table 2-1 lists the differences between the μPD75116H, 75117H and the μPD75P117H. To use PROM for application system debugging and preproduction and then use mask ROM for full-scale production, fully check the differences between the products.

For detailed information on the CPU function and hardware, refer to μPD75117H User's Manual (IEU-799).

Table 2-1 Differences between μPD75116H, 75117H and μPD75P117H

Parameter		μPD75116H	μPD75117H	μPD75P117H
ROM		16256 × 8 bits (mask ROM)	24448 × 8 bits (mask ROM)	24448 × 8 bits (one-time PROM)
16K-byte mode/24K-byte mode change function		None		Available
Mask option		Available (internal pull-up resistors in PORT12 to PORT14)		None
Pin configuration	Pin 40	IC		V_{PP}
	Pins 42 to 45	P30 to P33		P30/MD0 to P33/MD3
Electrical specifications		The products differ in consumption current, operation temperature range, etc. For details, refer to the electrical characteristics listed in their Data Sheets.		
Others		The products differ in circuit scale or mask layout, and thus in noise immunity, noise radiation, etc.		

Caution

The PROM and mask ROM differ in noise immunity and noise radiation. If considering replacing the PROM product with the mask ROM product in progress ahead of shifting from preproduction to full-scale production, make sufficient evaluation with the CS product of the mask ROM product rather than the ES product.

3. 16K-BYTE MODE/24K-BYTE MODE CHANGE FUNCTION

The μPD75P117H enables the user to select the 16K-byte mode or 24K-byte mode by setting the stack bank selection register (SBS).
Therefore, the μPD75P117H can be used to evaluate both the μPD75116H and 75117H.

3.1 Differences between 16K-Byte Mode and 24K-Byte Mode

Table 3-1 Differences between 16K-byte mode and 24K-byte mode

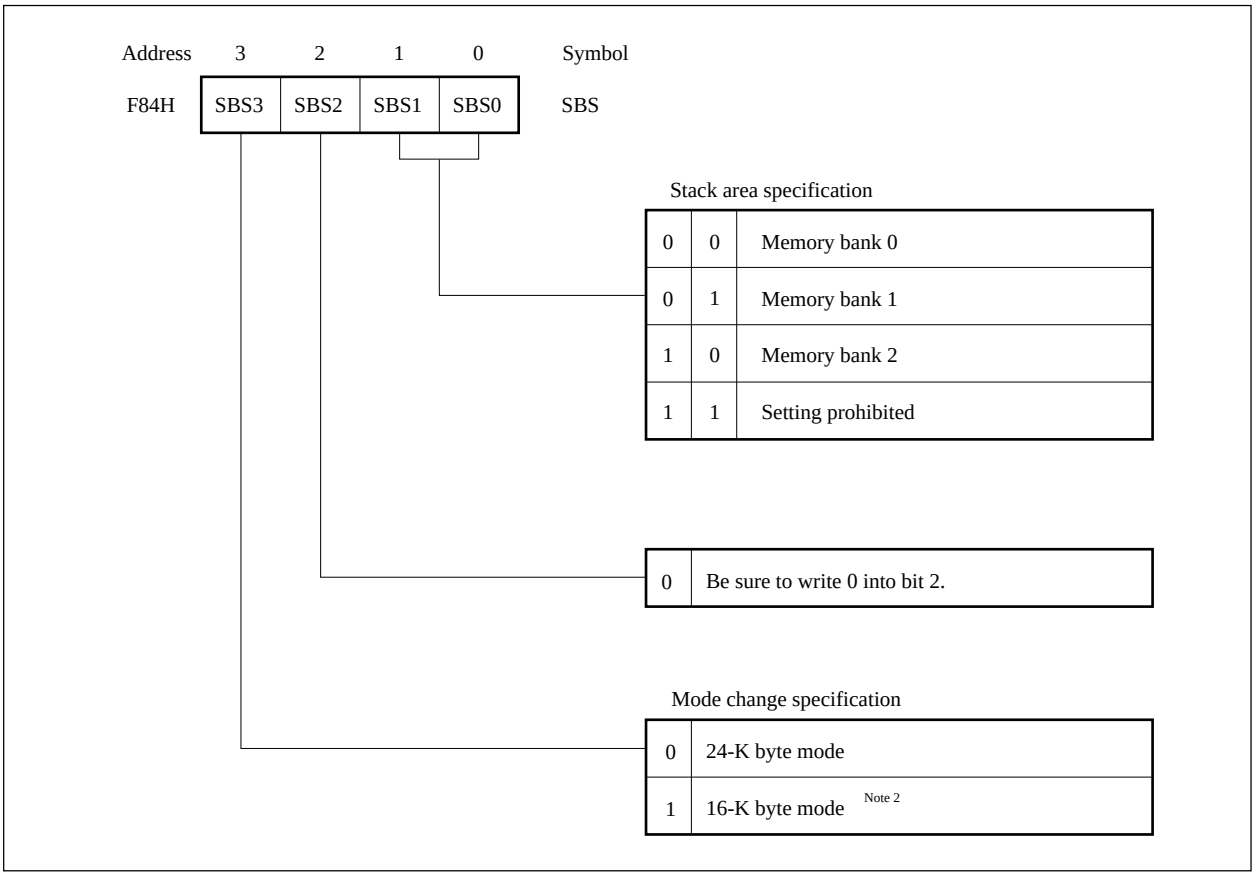
Parameter	When 16K-byte mode is selected	When 24K-byte mode is selected
Stack operation when subroutine call instruction is executed	2-byte stack	3-byte stack
Stack area	Bank 0	Banks 0 to 2
CALL instruction	3 machine cycles	4 machine cycles
TCALL instruction by GETI		
CALLF instruction	2 machine cycles	3 machine cycles
BRA instruction	Undefined operation	Normal operation
CALLA instruction		
BR BCXA		
BR BCDE		
MOVT XA, @BCXA		
MOVT XA, @BCDE		
Bit 14 of program counter	Fixed to 0	Corresponds to branch instruction, call instruction, table lookup instruction
Corresponding mask product	μPD75116H	μPD75117H

3.2 16K-Byte Mode and 24K-Byte Mode Change Method

The 16K-byte and 24K-Byte modes are changed by setting the stack bank selection register. Figure 3-1 shows the format of the stack bank selection register.

The stack bank selection register is set by executing a 4-bit memory manipulation instruction. When $\overline{\text{RESET}}$ is input, bit 3 of the stack bank selection register is set to 1, selecting the 16K-byte mode. Therefore, to use the 16K-byte mode, the stack bank selection register need not be manipulated. To use the 24K-byte mode, be sure to initialize the stack bank selection register to 00××B **Note 1** at the beginning of a program.

Figure 3-1 Format of stack bank selection register



Caution

To use the 24K-byte mode, after $\overline{\text{RESET}}$ is input, set the stack bank selection register and then execute a subroutine call instruction and an interrupt enable instruction.

Notes

1. Set any desired value in ××.
2. To use the 16K-byte mode after $\overline{\text{RESET}}$ is input, the stack bank selection register need not be manipulated.

4. PROM (PROGRAM MEMORY) WRITE AND VERIFICATION

The program memory contained in the μPD75P117H is a one-time PROM (programmable read-only memory).

To write and verify the PROM, use the pins listed in the table given below. Addresses are updated by clock input from the X1 pin rather than address input.

Pin name	Function
V_{PP}	Voltage application pin in program memory write/verify mode (normally, V_{DD} potential).
X1, X2	Address update clock input in program memory write/verify mode. Input inverted phase signal of the X1 pin to the X2 pin.
MD0 to MD3	Operation mode selection pins in program memory write/verify mode.
P40 to P43 (lower 4 bits) P50 to P53 (higher 4 bits)	8-bit data input/output pins in program memory write/verify mode.
V_{DD}	Supply voltage application pin. Apply 1.8 to 5.5 V at normal operation or 6 V in program memory write/verify mode.

Caution
Connect pins not used in the program memory write/verify mode to V_{SS} via pull-down resistors.

4.1 Operation Mode in Program Memory Write/Verify Mode

When +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin, the μPD75P117H enters the program memory write/verify mode. In this mode, the following operation modes are selected by setting the MD0 to MD3 pins:

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+ 12.5 V	+ 6 V	H	L	H	L	Program memory address clear to 0
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

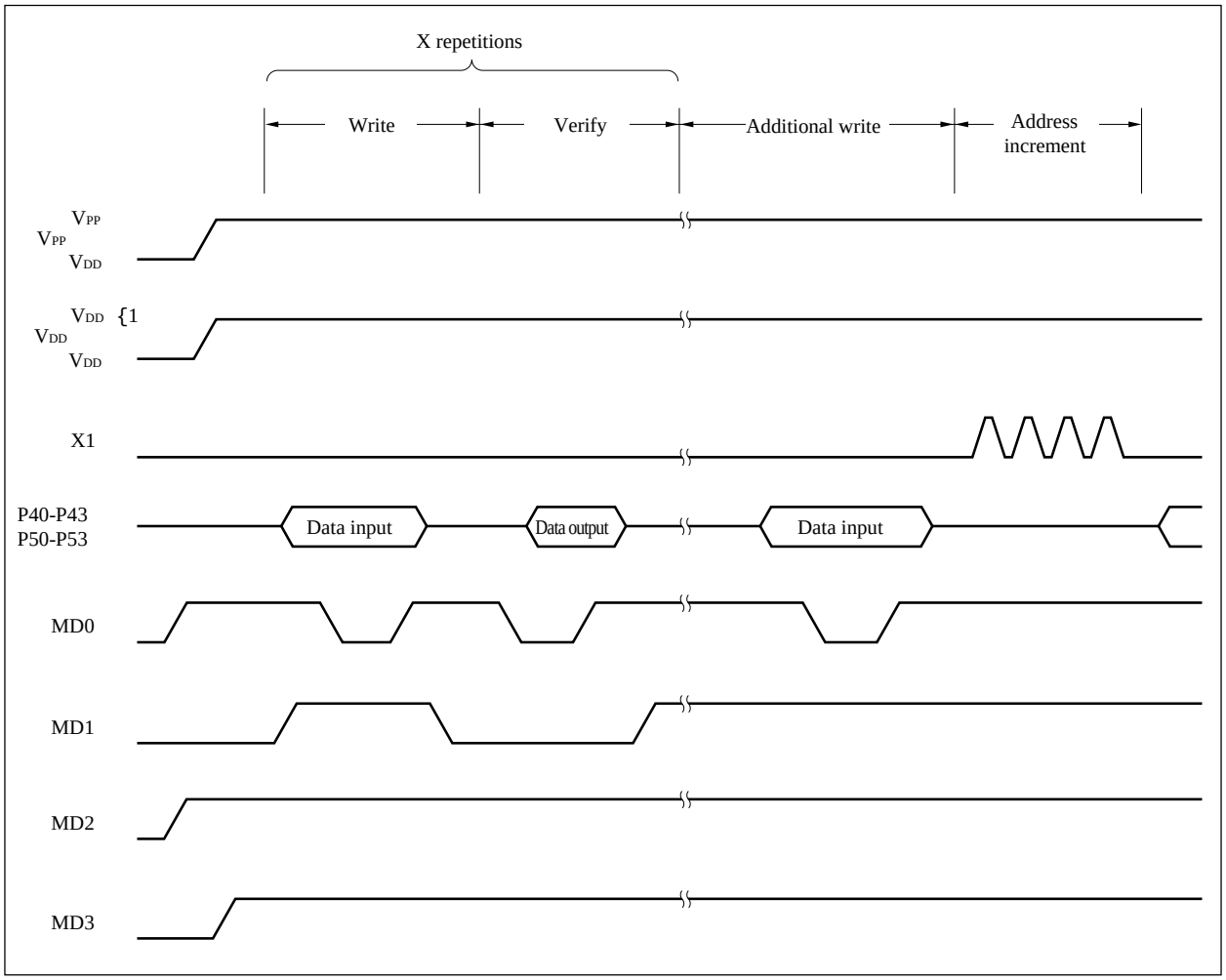
×: L (low) or H (high)

4.2 Program Memory Write Procedure

The program memory write procedure for high-speed writing is as follows:

(1) Connect unused pins to V_{SS} via pull-down resistors. Set the X1 pin low.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Program memory address clear to 0 mode.
(5) Supply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Program inhibit mode.
(9) Verify mode. If the data is written normally, go to (10); if not written, repeat (7) to (9).
(10) Additional write for (write count at (7) to (9): X) × 1 ms.
(11) Program inhibit mode.
(12) Update the program memory address (+1) by inputting four pulses to the X1 pin.
(13) Repeat (7) to (12) up to the end address.
(14) Program memory address clear to 0 mode.
(15) Change the voltages of the V_{DD} and V_{PP} pins to +5 V.
(16) Turn off the power.

The steps (2) to (12) are shown below:

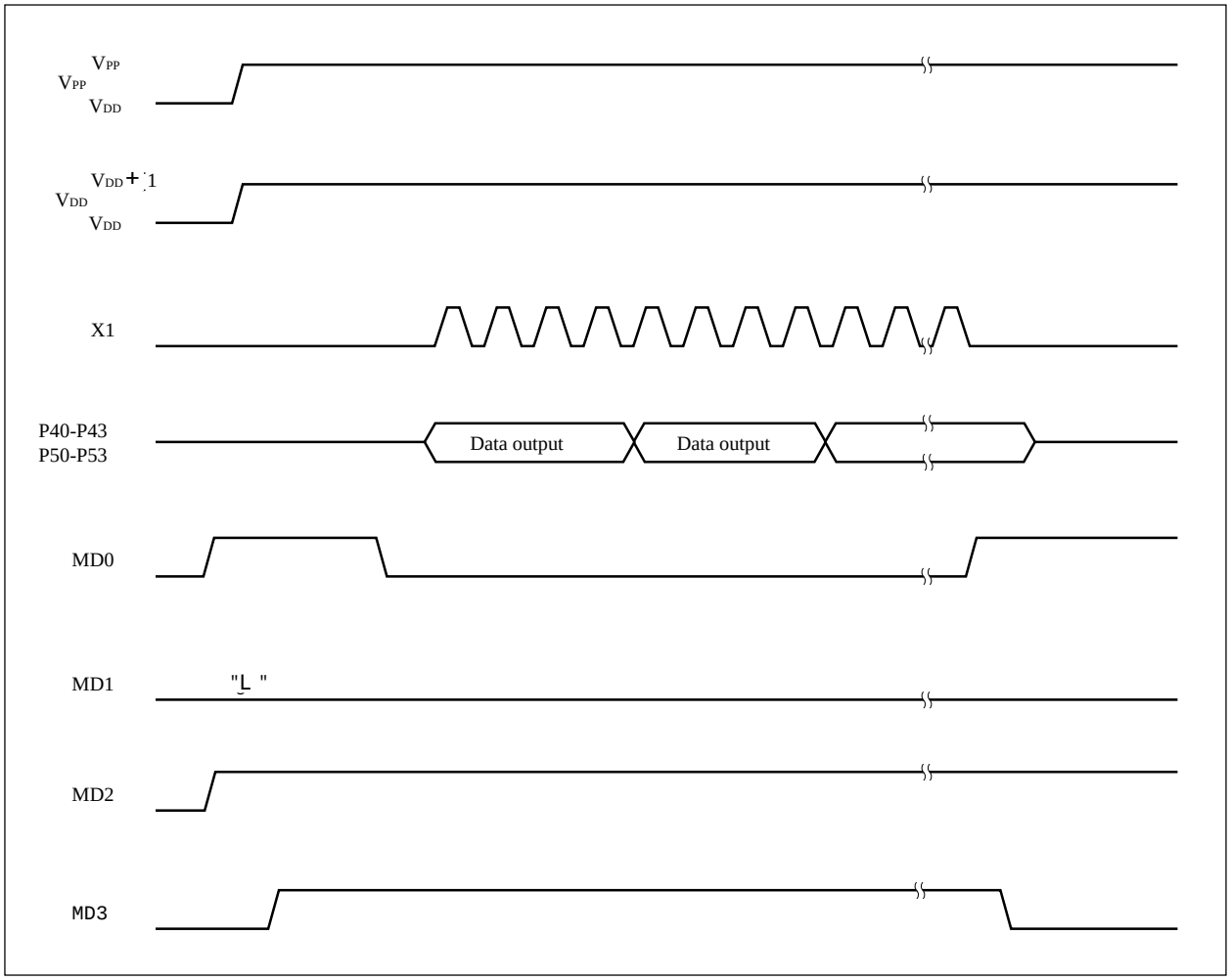


4.3 Program Memory Read Procedure

The program memory contents of the μPD75P117H can be read according to the following procedure:

(1) Connect unused pins to V_{SS} via pull-down resistors. Set the X1 pin low.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Program memory address clear to 0 mode.
(5) Supply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Verify mode. Whenever four clock pulses are input to the X1 pin, data is output in sequence at one address at a time.
(8) Program inhibit mode.
(9) Program memory address clear to 0 mode.
(10) Change the voltages of the V_{DD} and V_{PP} pins to +5 V.
(11) Turn off the power.

The steps (2) to (9) are shown below:



5. ONE-TIME PROM PRODUCT SCREENING

The one-time PROM products cannot be completely tested by NEC for shipment because of the structures. For screening, it is recommended to verify PROM after storing the necessary data under the following conditions:

Storage temperature	Storage time
125 °C	24 hours

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_a = 25 °C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to + 7.0	V
Input voltage	V_{I1}	Other than ports 12 to 14		–0.3 to V_{DD} + 0.3	V
	V_{I2} **Note 1**	Ports 12 to 14		–0.3 to +7.3	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current, high	I_{OH}	Per pin		–15	mA
		Total, all output pins		–30	mA
Output current, low	I_{OL} **Note 2**	Per pin	Peak	30	mA
			r.m.s.	15	mA
		Total of ports 0, 2, 12, 13 and 14	Peak	100	mA
			r.m.s.	60	mA
		Total of ports 3 to 9	Peak	100	mA
			r.m.s.	60	mA
Operating ambient temperature	T_{opt}			–40 to +60	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes

1. Power supply impedance (pull-up resistor) should be 50 kΩ or more when a voltage exceeding 6 V is applied to ports 12 to 14.
2. Use the following formula to calculate the r.m.s. value (Effective value).
   r.m.s. = (Peak value) × $\sqrt{\text{Duty cycle}}$

Caution

If one of the parameters exceeds the absolute maximum ratings even momentarily the product quality may be damaged. This means that the absolute maximum ratings are rated values which may physically damage the products. Preferably, use the products at values less than the absolute maximum ratings.

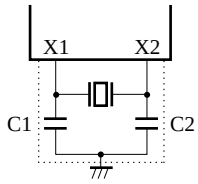
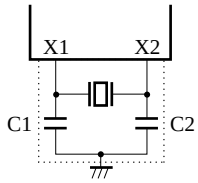
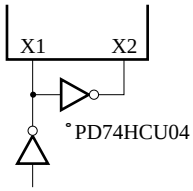
Operating Temperature Range

Parameter	Conditions	MIN.	MAX.	Unit
CPU		–40	+60	°C
Programmable threshold port (comparator input)		–10	+60	°C
Other hardware		–40	+60	°C

Capacitance (T_a = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
Input/output capacitance	C_{IO}				15	pF

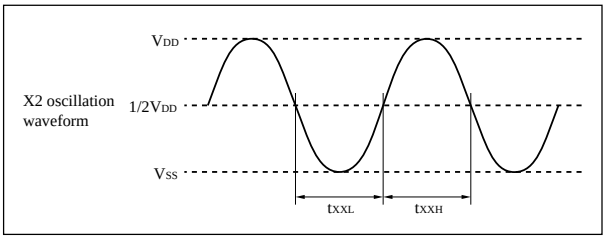
Oscillator Characteristics (Ta = –40 to +60 °C, V_{DD} = 1.8 to 5.5 V)

Source	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator **Note 1**		Oscillation frequency (f_{XX}) **Note 2**		2.0		5.0 **Note 4**	MHz
		Oscillation stabilization time **Note 3**	After V_{DD} reaches the minimum value in the oscillator operating voltage range			4	ms
Crystal resonator **Note 1**		Oscillation frequency (f_{XX}) **Note 2**		2.0	4.19	5.0 **Note 4**	MHz
		Oscillation stabilization time **Note 3**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock **Note 5**		X1 input frequency (f_X) **Note 2**	V_{DD} = 2.7 to 5.5 V	2.0		5.0 **Note 4**	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		250	ns

Notes

1. To use with V_{DD} < 2.7 V, place duty of the oscillation waveform at the X2 pin within the range of 45% to 55%.

$$\text{Duty} = \frac{t_{XXL} \text{ (or } t_{XXH})}{t_{XXL} + t_{XXH}} \times 100$$



2. The oscillation frequency and X1 input frequency shows only characteristics of the oscillation circuit. For the instruction execution time, see the AC characteristics.

3. The oscillation stablilization time is the time required for oscillation to become stable after V_{DD} reaches the minimum value in the oscillation voltage range or the STOP mode is released.

4. If the oscillation frequency is 4.19 MHz < f_{XX} = ≤ 5.0 MHz, do not set PCC to 0011 for the instruction execution time. If PCC is set to 0011, one machine cycle becomes less than 0.95 μs and the specified minimum value 0.95 μs cannot be followed.

5. External clock input cannot be used with V_{DD} < 2.7 V.

Caution

To use the system clock oscillator, wire the portions surrounded by ⋯ (dotted square) to avoid wiring capacitance affection, etc., as follows:

- **Make wiring as extremely short as possible.**
- **Do not cross the oscillator and any other signal line over each other.**
- **Do not put the oscillator near any line where high current fluctuates.**
- **Be sure to place oscillator capacitor ground point in the same potential as the V_{SS} pin. Do not connect to any ground pattern where high current flows.**
- **Do not take out any signal from the oscillator.**

Recommended Oscillator Constants

Ceramic resonator (T_a = –40 to +60 °C)

Manufacturer	Part number	Frequency (MHz)	Recommended constants (pF)		Oscillation voltage range (V)	
			C1	C2	MIN.	MAX.
KYOCERA	KBR - 2.0MS	2.00	47	47	1.8	5.5
	PBRC 2.00A					
	KBR - 4.0MSA	4.00	33	33		
	PBRC 4.00A					
	KBR - 4.0MKS		Contained	Contained		
	KBR - 4.0MWS					
	KBR - 4.19MSA	4.19	33	33		
	PBRC 4.19A					
	KBR - 4.19MKS		Contained	Contained		
	KBR - 4.19MWS					
	KBR - 5.0MSA	5.00	33	33		
	PBRC 5.00A					
	KBR - 5.0MKS		Contained	Contained		
	KBR - 5.0MWS					

DC Characteristics (T_a = –40 to +60 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Other than indicated below		V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, TI0, TI1, $\overline{\text{RESET}}$			0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 12 to 14		V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		6	V
				V_{DD} = 1.8 to 2.7 V	0.8 V_{DD}		6	V
	V_{IH4}	X1, X2		V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	V_{DD} – 0.3		V_{DD}	V
Input voltage, low	V_{IL1}	Other than indicated below		V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0		0.2 V_{DD}	V
	V_{IL2}	Ports 0, 1, TI0, TI1, $\overline{\text{RESET}}$			0		0.2 V_{DD}	V
	V_{IL3}	X1, X2		V_{DD} = 2.7 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 2.7 V	0		0.25	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} = 4.5 to 5.5 V	V_{DD} – 1.0			V
				V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.8			V
		I_{OH} = –100 μA		V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5			V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.2			V
Output voltage, low	V_{OL}	Ports 0, 2, 4 to 8	I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V		0.35	2.0	V
			I_{OL} = 1.6 mA	V_{DD} = 2.7 to 5.5 V			0.4	V
			I_{OL} = 400 μA	V_{DD} = 2.7 to 5.5 V			0.5	V
			I_{OL} = 100 μA	V_{DD} = 1.8 to 5.5 V			0.3	V
		Ports 3, 9	I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V		0.35	2.0	V
			I_{OL} = 10 mA	V_{DD} = 2.7 to 5.5 V		0.3	1.0	V
			I_{OL} = 1.6 mA	V_{DD} = 2.7 to 5.5 V			0.4	V
			I_{OL} = 400 μA	V_{DD} = 2.7 to 5.5 V			0.5	V
			I_{OL} = 100 μA	V_{DD} = 1.8 to 5.5 V			0.3	V
		Ports 12 to 14	I_{OL} = 10 mA	V_{DD} = 4.5 to 5.5 V		0.35	2.0	V
			I_{OL} = 1.6 mA	V_{DD} = 2.7 to 5.5 V			0.4	V
			I_{OL} = 400 μA	V_{DD} = 2.7 to 5.5 V			0.5	V
			I_{OL} = 100 μA	V_{DD} = 1.8 to 5.5 V			0.3	V
Input leak current, high	I_{LIH1}	V_{IN} = V_{DD}	Other than indicated below				3	μA
	I_{LIH2}		X1, X2				20	μA
	I_{LIH3}	V_{IN} = 6 V	Ports 12 to 14				15	μA
Input leak current, low	I_{LIL1}	V_{IN} = 0 V	Other than indicated below				–3	μA
	I_{LIL2}		X1, X2				–20	μA
Output leak current, high	I_{LOH1}	V_{OUT} = V_{DD}	Other than indicated below				3	μA
	I_{LOH2}	V_{OUT} = 6 V	Ports 12 to 14				20	μA
Output leak current, low	I_{LOL}	V_{OUT} = 0 V					–3	μA

DC Characteristics (T_a = –40 to +60 ˚C, V_{DD} = 1.8 to 5.5V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	4.19 MHz Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5 V ±10 % Note 2		3.5	10.0	mA
			V_{DD} = 3 V ±10 % Note 2		1.7	5.0	mA
			V_{DD} = 2 V ±10 % Note 3		0.65	2.0	mA
	I_{DD2}		HALT mode V_{DD} = 5 V ±10 %		0.8	2.5	mA
			HALT mode V_{DD} = 3 V ±10 %		0.3	1.0	mA
			HALT mode V_{DD} = 2 V ±10 %		150	450	μA
	I_{DD3}	STOP mode	V_{DD} = 5 V ±10 %		0.2	50	μA
			V_{DD} = 3 V ±10 %		0.1	20	μA
			V_{DD} = 2 V ±10 %		0.05	10	μA

Notes

1. Current flowing into the comparator circuit is not contained.

2. When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

3. When operated in the middle-speed mode with the PCC set to 0010.

Comparator Characteristics (T_a = –10 to +60 ˚C Note, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}					±100	mV
Threshold voltage	V_{TH}			0		V_{DD}	V
PTH input voltage	V_{IPTH}			0		V_{DD}	V
Comparator consumption current		Set PTHM7 to 1	V_{DD} = 5.0 V		0.7		mA
			V_{DD} = 3.0 V		0.3		mA
			V_{DD} = 2.0 V		0.1		mA

Note

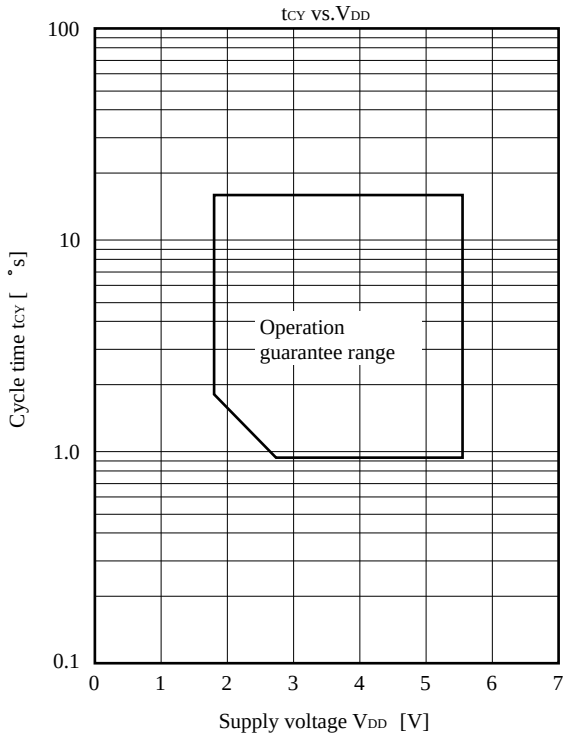
The comparator does not operate at –40 ˚C ≤ T_a < –10 ˚C. Use it in the range of –10 ˚C ≤ T_a ≤ +60 ˚C.

AC Characteristics (T_a = –40 to +60 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note (minimum instruction execution time = One machine cycle)	t_{CY}	V_{DD} = 2.7 to 5.5 V		0.95		16	μs
				1.91		16	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1	MHz
				0		275	kHz
TI0, TI1 input high/low level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 to 5.5 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
$\overline{SCK}$ high/low level width	t_{KH}, t_{KL}	V_{DD} = 4.5 to 5.5 V	Input	0.4			μs
			Output	t_{KCY}/2–50			ns
			Input	1.6			μs
			Output	t_{KCY}/2–150			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK}			100			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI}			400			ns
SO output delay time from $\overline{SCK}$ ↓	t_{KSO}	V_{DD} = 4.5 to 5.5 V		0		300	ns
				0		1000	ns
INT0 to INT4 High/low level width	t_{INTH}, t_{INTL}			5			μs
$\overline{RESET}$ low level width	t_{RSL}			5			μs

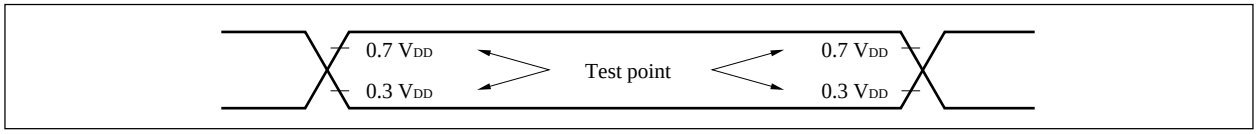
Note

The cycle time of the CPU clock (Φ) is determined by the oscillation frequency of the connected oscillator and processor clock control register setting. t_{CY} for V_{DD} is as shown in the right figure.

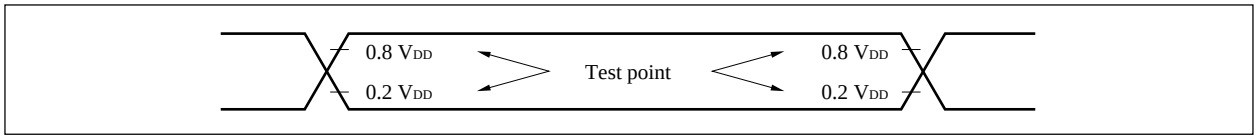


AC Timing Measurement Points (Except ports 0, 1, TI0, TI1, X1, X2 and $\overline{\text{RESET}}$)

(1) V_{DD} = 2.7 to 5.5 V

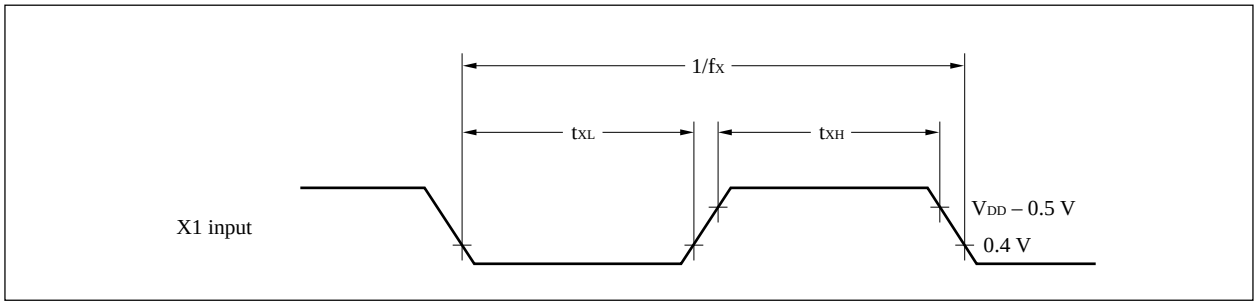


(2) V_{DD} = 1.8 to 2.7 V

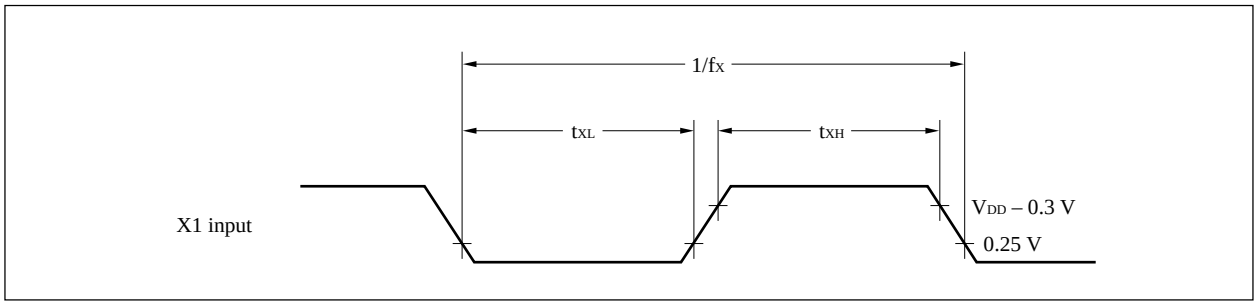


Clock Timing

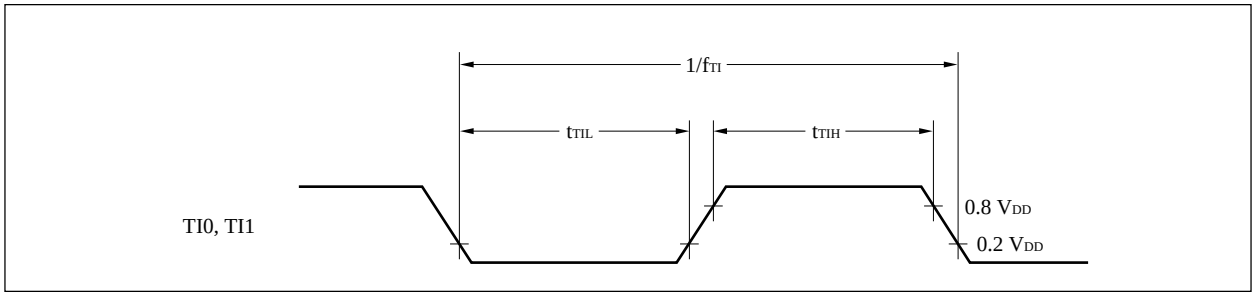
(1) V_{DD} = 2.7 to 5.5 V



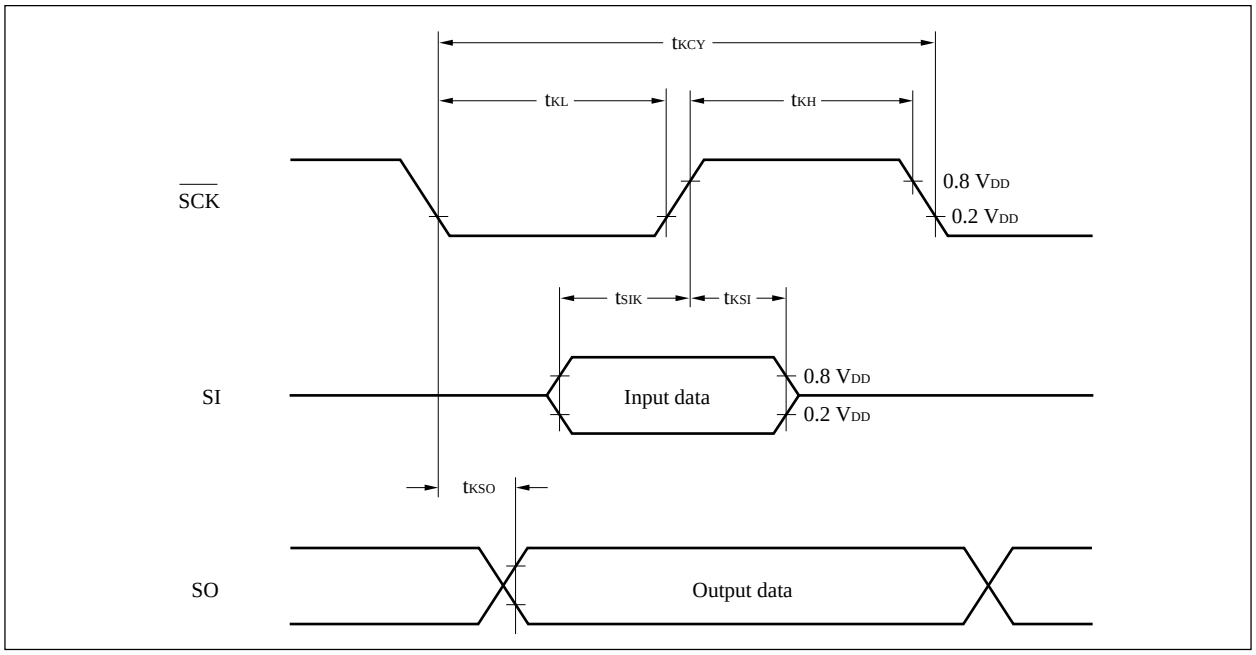
(2) V_{DD} = 1.8 to 2.7 V



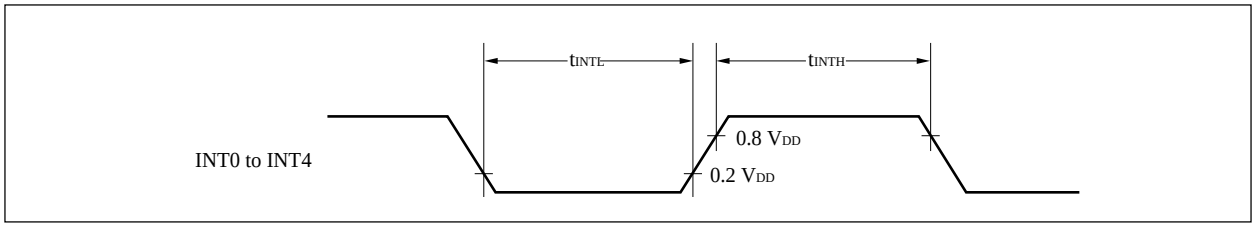
TI0, TI1 Input Timing



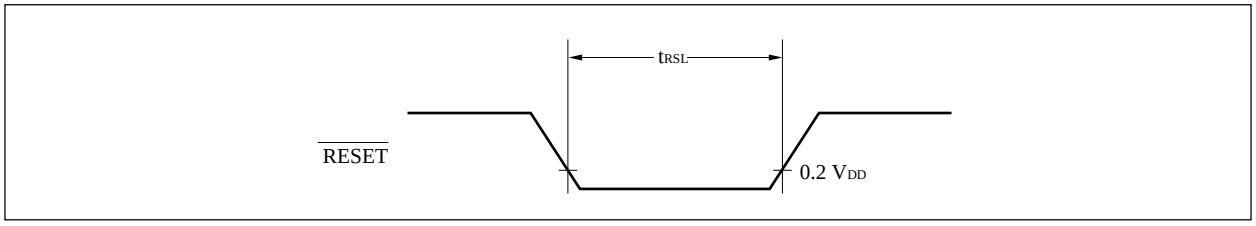
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Data Memory STOP Mode Low Voltage Data Retention Characteristics (T_a = –40 to +60 ˚C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		1.8		5.5	V
Data retention current Note 1	I_{DDDR}	V_{DDDR} = 2.0 V		0.05	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 2	t_{WAIT}	Release by $\overline{RESET}$ input		$2^{17}/f_{XX}$		ms
		Release by interrupt request		Note 3		ms

Notes

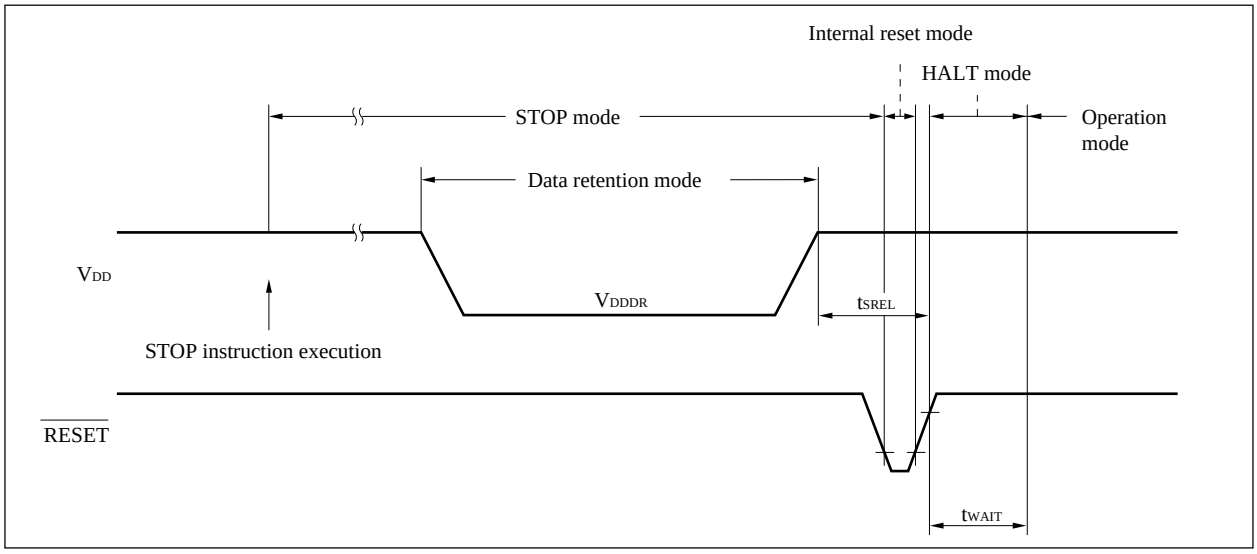
1. Current in the internal pull-up resistors is not included.

2. The oscillation stabilization wait time is the time required before beginning CPU operation in order to prevent unstable CPU operation when oscillation is initiated.

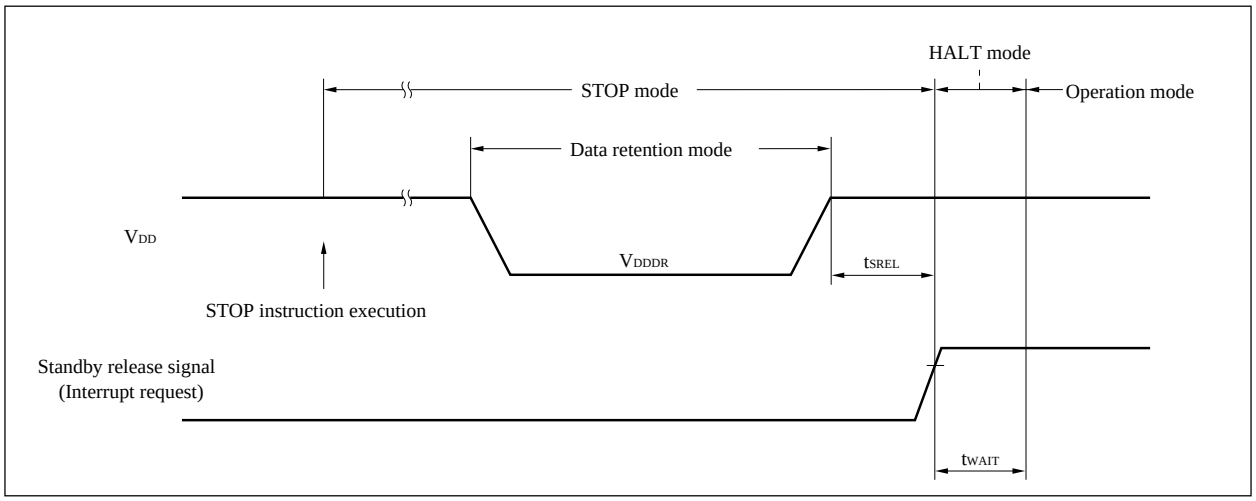
3. Depends on the setting of the basic interval timer mode register (BTM) (refer to the table below).

BTM3	BTM2	BTM1	BTM0	WAIT time ( ) indicates f_{XX} = 4.19 MHz
–	0	0	0	$2^{20}/f_{XX}$ (Approximately 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (Approximately 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (Approximately 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (Approximately 1.95 ms)

Data Retention Timing (when STOP mode is released by $\overline{RESET}$ input)

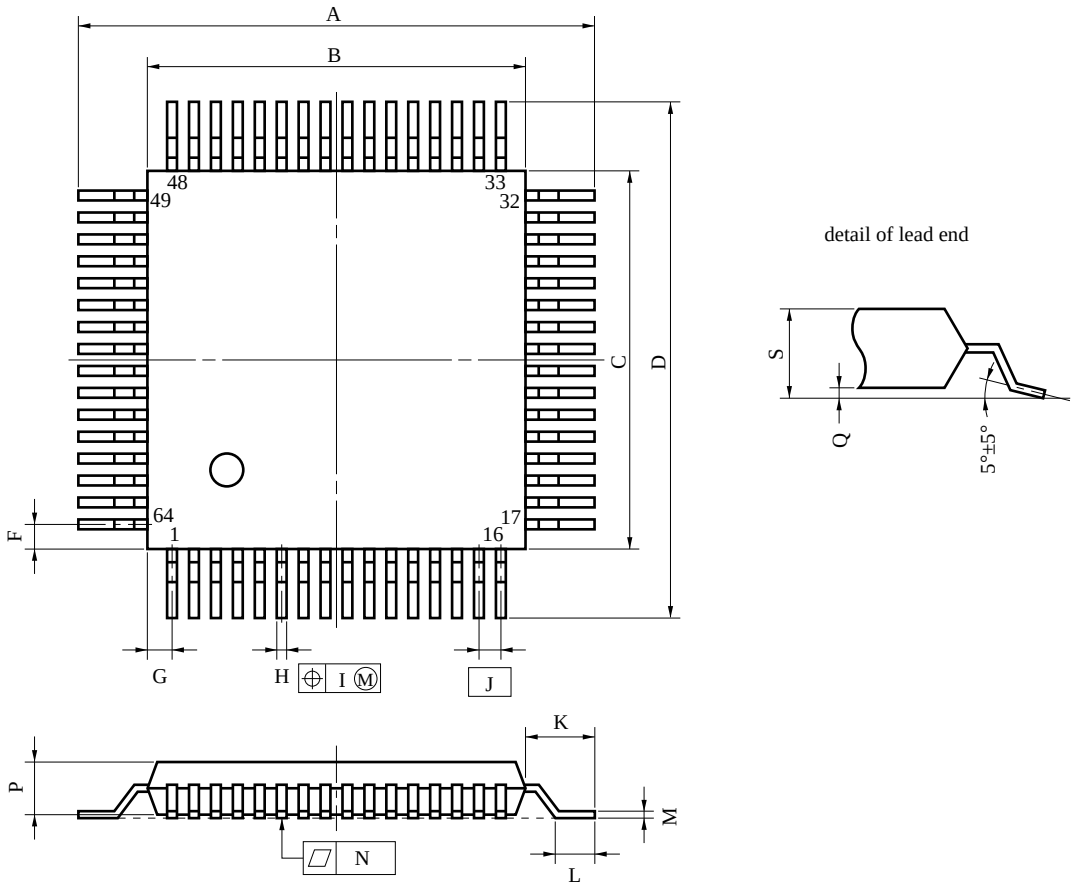


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



7. PACKAGE DRAWINGS

64 PIN PLASTIC QFP (□14)



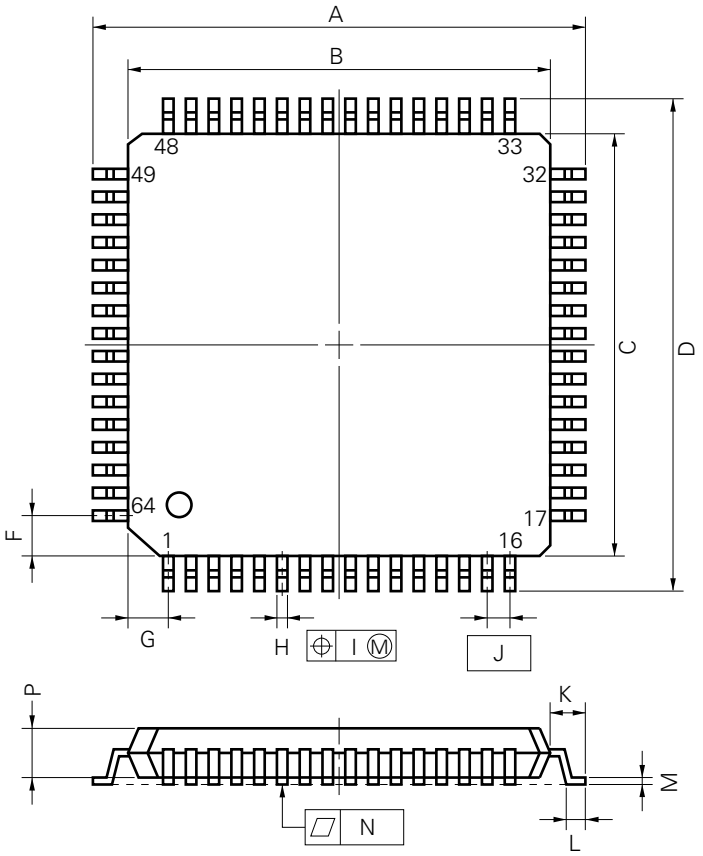
P64GC-80-AB8-3

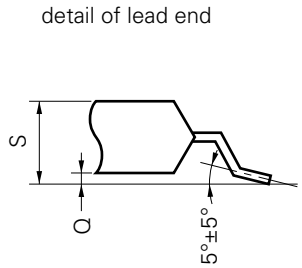
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

64 PIN PLASTIC QFP (□12)





P64GK-65-8A8

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	1.4	0.055
Q	0.1±0.1	0.004±0.004
S	1.7 MAX.	0.067 MAX.

8. RECOMMENDED SOLDERING CONDITIONS

Solder the product under the recommended conditions listed below.

For details of the recommended conditions for soldering, refer to the Information: Semiconductor Device Mount Technology Manual (IEI-1207).

Consult the NEC sales person about soldering methods and soldering conditions other than those listed below.

Table 8-1 Recommended Condition for Surface Mount Type

(1) μPD75P117HGC-AB8: 64-pin plastic QFP (14 × 14 mm)

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C, Reflow time: Within 30 s (at 210 °C or higher), Number of processes: Two	IR35-00-2
VPS	Peak temperature of package surface: 215 °C, Reflow time: Within 40 s (at 200 °C or higher), Number of processes: Two	VP15-00-2
Partial heating	Pin temperature: 300 °C or less, Time: Within 3 s (one side of device)	–

(2) μPD75P117HGK-8A8: 64-pin plastic QFP (12 × 12 mm)

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C, Reflow time: Within 30 s (at 210 °C or higher), Number of processes: Two, Exposure limit: 7 days **Note** (past the limit, prebake is required at 125 °C for 10 hours)	IR35-107-2
VPS	Peak temperature of package surface: 215 °C, Reflow time: Within 40 s (at 200 °C or higher), Number of processes: Two, Exposure limit: 7 days **Note** (past the limit, prebake is required at 125 °C for 10 hours)	VP15-107-2
Wave soldering	Solder temperature: 260 °C or less, Reflow time: Within 10 s, Number of process: One, Preheating temperature: 120 °C MAX. (package surface temperature), Exposure limit: 7 days **Note** (past the limit, prebake is required at 125 °C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300 °C or less, Time: Within 3 s (one side of device)	–

Note

It is the number of storage days Storage conditions of 25 °C and 65 % RH or less after the dry pack is opened.

Caution

Do not combine soldering methods together (except the partial heating method).

APPENDIX A DIFFERENCES AMONG μPD751×× SUBSERIES PRODUCTS

Item \ Part No.		μPD75104/106/108/112/116	μPD75104A/108A	μPD75108F/112F/116F
ROM (byte)		4K/6K/8K/12K/16K (Mask ROM)	4K/8K (Mask ROM)	8K/12K/16K (Mask ROM)
RAM (× 4 bits)		320/320/512/512/512	320/512	512
Instruction Set		75X High-End		
Input/ output port	Total	58 lines		
	CMOS input	10 lines	10 lines (pull-up resistor mask option: 4 lines)	10 lines
	CMOS input/output	32 lines (can drive LEDs directly Note 2)	32 lines (pull-up resistor mask option: 24 lines, can drive LEDs directly)	32 lines (can drive LEDs directly Note 2)
	N-ch open-drain output	12 lines (can drive LEDs directly Note 2)		
	Voltage	+12 V		+10 V
	Pull-up resistor	Pull-up resistor can be contained by mask option		
	Analog input	4 lines (4-bit accuracy)		
Power-on reset circuit		Internal (mask option)		None
Power-on flag				
Operating supply voltage		2.7 to 6.0 V		2.7 to 5.0 V (T_a = –40 to +50 ˚C) 2.8 to 5.0 V
Operating ambient temperature		–40 to +85 ˚C		–40 to +60 ˚C
Minimum instruction execution time		0.95 μs (V_{DD} = 4.5 to 6.0 V) 3.8 μs (V_{DD} = 2.7 V)		0.95 μs (V_{DD} = 4.5 to 5.0 V) 1.91 μs (V_{DD} = 2.7 V)
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic QFP (14 × 14 mm) (resin thickness: 2.55 mm) • 64-pin plastic QFP (14 × 14 mm) (resin thickness: 1.5 mm)	64-pin plastic QFP (14 × 20 mm)

Notes

1. Can be used as 75X High-End by the 16K-byte/24K-byte mode change function.

2. For details, refer to the electrical specifications of individual Data Sheet.

μPD75116H/117H	μPD75P108B	μPD75P116	μPD75P117H
16K/24K (Mask ROM)	8K (One-time PROM, EPROM)	16K (One-time PROM)	24K (One-time PROM)
768	512		768
75X High-End/Expansion High-End	75X High-End		75X Expansion High-End Note 1
58 lines			
10 lines			
32 lines (can drive LEDs directly Note 2)			
12 lines (can drive LEDs directly Note 2)			
+6 V	+12 V		+6 V
Pull-up resistor that can be contained by mask option	None		
4 lines (4-bit accuracy)			
None			
1.8 to 5.5 V	2.7 to 6.0 V	5 V ±10 %	1.8 to 5.5 V
–40 to +60 ˚C	–40 to +85 ˚C		–40 to +60 ˚C
0.95 μs (V_{DD} = 2.7 V) 1.91 μs (V_{DD} = 1.8 V)	0.95 μs (V_{DD} = 4.5 to 6.0 V) 3.8 μs (V_{DD} = 2.7 V)	0.95 μs (V_{DD} = 4.75 to 5.5 V)	0.95 μs (V_{DD} = 2.7 V) 1.91 μs (V_{DD} = 1.8 V)
• 64-pin plastic QFP (12 × 12 mm) • 64-pin plastic QFP (14 × 14 mm) (resin thickness: 2.55 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin ceramic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic QFP (12 × 12 mm) • 64-pin plastic QFP (14 × 14 mm) (resin thickness: 2.55 mm)

APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD75P117H.

Hardware	IE-75000-R [Note 1] IE-75001-R		In-circuit emulators for 75X series
	IE-75000-R-EM [Note 2]		Emulation board for IE-75000-R and IE-75001-R
	EP-75108AGC-R	EV-9200GC-64	μPD75P117HGC emulation probe common to the μPD75108A, 64-pin conversion socket EV-9200GC-64 is attached.
	EP-75117GK-R	EV-9500GK-64	μPD75P117HGK emulation probe, 64-pin conversion adapter EV-9500GK-64 is attached.
	PG-1500		PROM programmer
	PA-75P117GC		μPD75P117HGC PROM programmer adapter which is connected to PG-1500.
	PA-75P117GK		μPD75P117HGK PROM programmer adapter which is connected to PG-1500.
Software	IE control program		Host machine PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A [Note 3]) IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller		
	RA75X relocatable assembler		

Notes

1. Maintenance product

2. Not contained in IE-75001-R.

3. Although Ver. 5.00/5.00A provides the task swap function, the function cannot be used under this software.

APPENDIX C RELATED DOCUMENTS

Documents Related to Device

Title	Doc. No.
User's Manual	IEU-1340
Instruction Quick Reference	–
75X Series Selection Guide	IF-1027

Documents Related to Development Tool

Title			Doc. No.
Hard-ware	IE-75000-R/IE-75001-R User's Manual		EEU-1416
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75117GK-R User's Manual		EEU-1421
	PG-1500 User's Manual		EEU-1335
Soft-ware	RA75X Assembler Package User's Manual	Operation	EEU-1346
		Language	EEU-1343
	PG-1500 Controller User's Manual		EEU-1291

Other Related Documents

Title	Doc. No.
Package Manual	IEI-1213
Semiconductor Mount Technology Manual	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability/ Quality Control System	–
Electrostatic Discharge (ESD) Test	–
Guide to Quality Assurance for Semiconductor Devices	MEI-1202
Microcomputer-Related Product Guide - Third Party Products	–

Caution

The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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