NEC

MOS INTEGRATED CIRCUIT

μPD78P014Y

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78P014Y is a member of the μPD78014Y subseries of 78K/0 series products. It uses a one-time programmable (OTP) ROM or EPROM instead of the mask ROM of the μPD78014Y.

Because the μPD78P014Y can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

Detailed information about product features and specifications can be found in the following document. Please make sure to read this document before starting design.

μPD78014, 78014Y Series User's Manual: IEU-1343

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Internal PROM: 32K bytes[Note]
  - μPD78P014YDW : Reprogrammable (ideal for system evaluation)
  - μPD78P014YCW, 78P014YGC-AB8 : Programmable once only (ideal for small-scale production)
- Internal high-speed RAM: 1024 bytes[Note]
- Buffer RAM: 32 bytes
- Connectable to I^2C bus interface
- Operable over same supply voltage range as mask ROM version (2.7 to 6.0 V)
- Available for the QTOP™ microcomputer ★

Note The internal PROM and internal high-speed RAM capacity can be changed by using the internal memory switching register.

Remark The QTOP microcomputer is the general term for a single-chip microcomputer with on-chip one-time PROM. NEC supports its program writing, marking, screening, and verification.

Differences from mask ROM versions are as follows:

- The same memory mapping as on a mask ROM version is possible by setting the internal memory switching register.
- There is no function for incorporating pull-up resistors by means of a mask option in P60 to P63 pins.

ORDERING INFORMATION

Part No.	Package	Internal ROM
μPD78P014YCW	64-pin plastic shrink DIP (750 mil)	One-time PROM
μPD78P014YDW	64-pin ceramic shrink DIP (with window) (750 mil)	EPROM
μPD78P014YGC-AB8	64-pin plastic QFP (14 × 14 mm)	One-time PROM

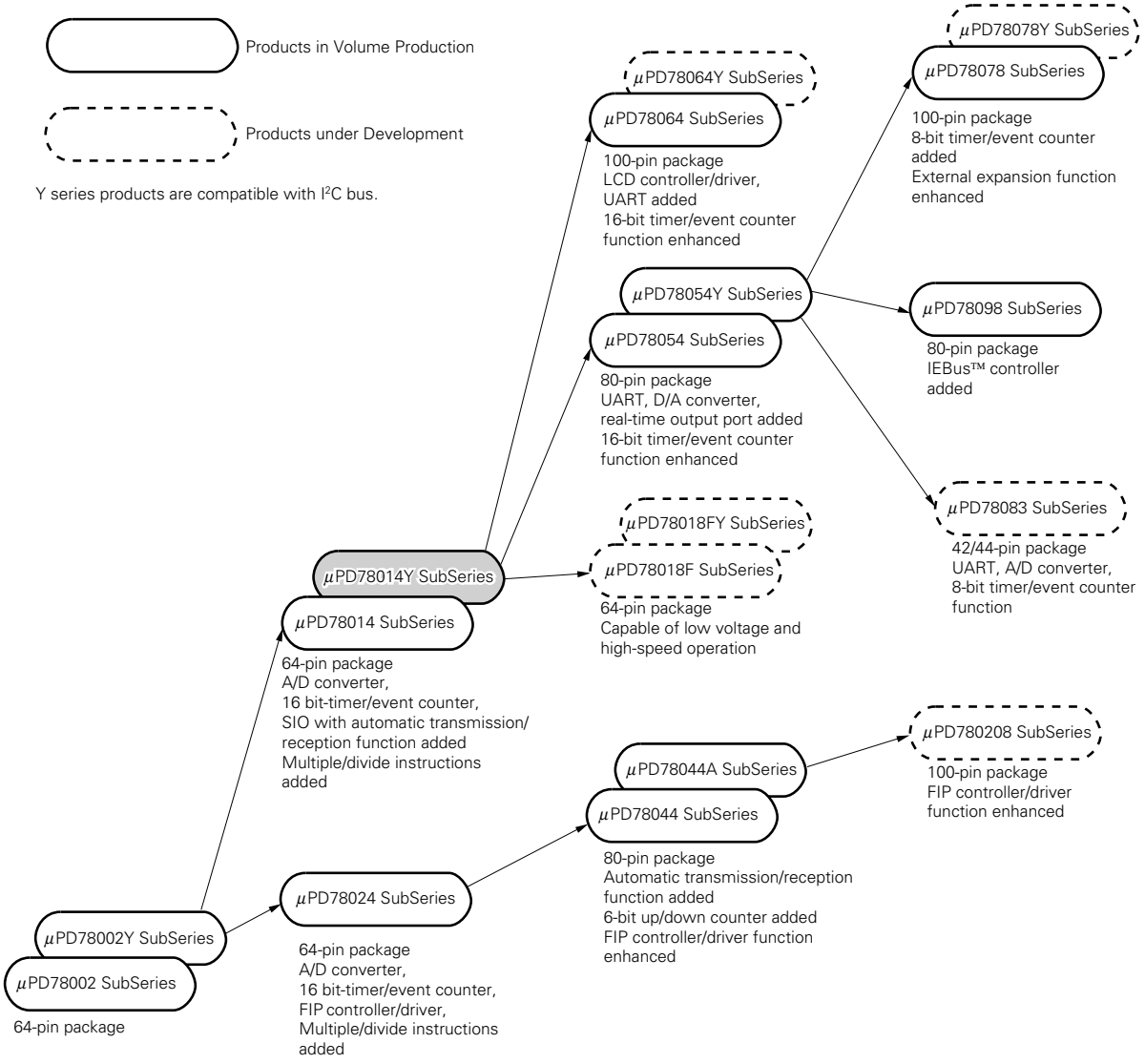
In this manual, PROM indicates the features common to the one-time PROM versions and the EPROM versions.

The information in this document is subject to change without notice.

Document No. IC-3180B
(O. D. No. IC-8572B)
Date Published January 1995 P
Printed in Japan

The mark ★ shows revised points.

★ DEVELOPMENT OF 78K/0 SERIES



FUNCTIONAL OUTLINE

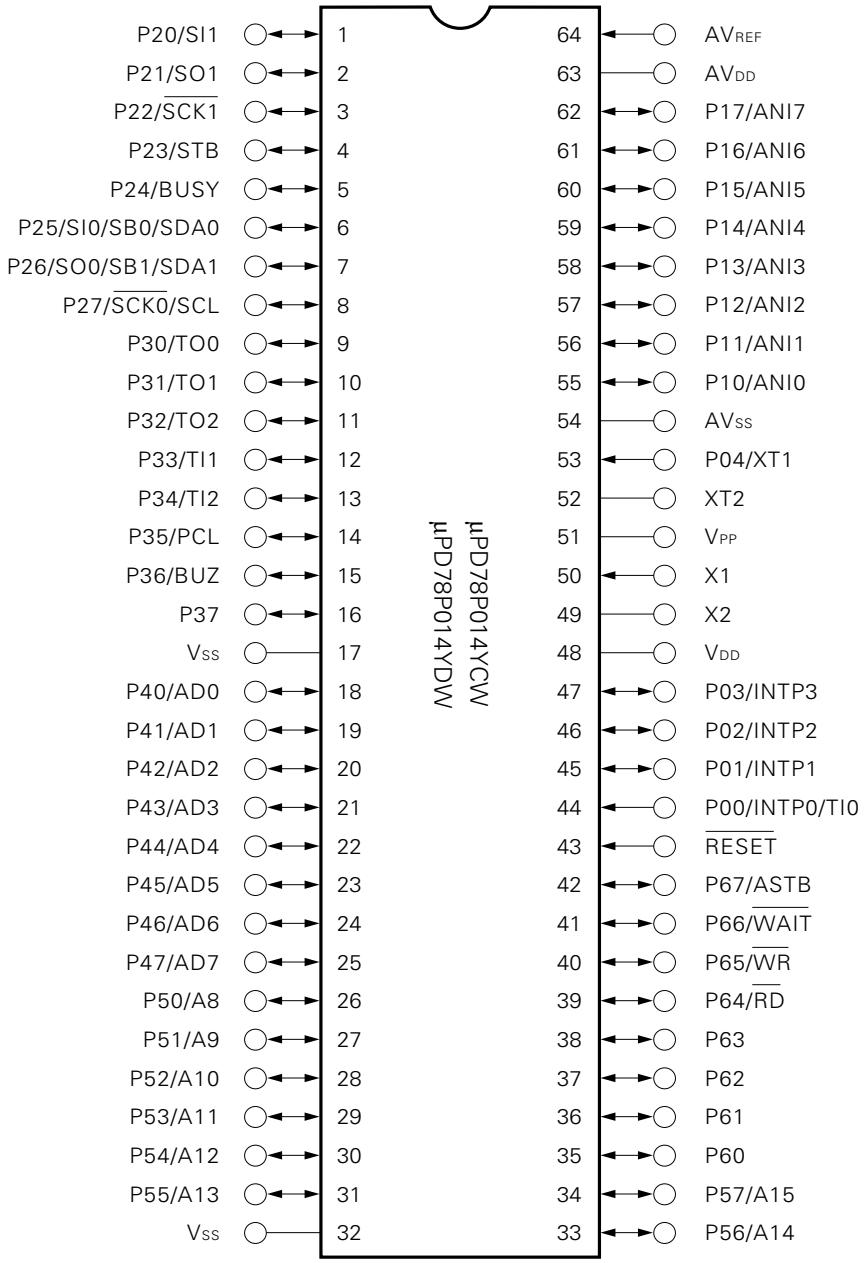
Item		Function
Internal memory		• PROM: 32K bytes[Note] • RAM Internal high-speed RAM: 1024 bytes[Note] Buffer RAM: 32 bytes
Memory space		64K bytes
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time cycle modification function
	Main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 10.0 MHz operation)
	Subsystem clock selected	122 μs (@ 32.768 kHz operation)
Instruction set		• 16-bit operation • Multiple/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total : 53 • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4
A/D converter		• 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: V_{DD} = 2.7 to 6.0 V
Serial interface		• 3-wire/SBI/2-wire/I²C bus mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		3 (14-bit PWM output × 1)
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (@ 10.0 MHz operation with main system clock) 32.768 kHz (@ 32.768 kHz operation with subsystem clock)
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (@ 10.0 MHz operation with main system clock)
Vectored interrupts	Maskable interrupts	Internal: 8, External: 4
	Non-maskable interrupt	Internal: 1
	Software interrupt	Internal: 1
Test input		Internal: 1, External: 1
Operating voltage range		V_{DD} = 2.7 to 6.0 V
Operating temperature range		–40 to +85 °C
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm) • 64-pin ceramic shrink DIP (with window) (750 mil)

Note The capacity of the internal PROM and internal high-speed RAM can be set by means of the internal memory switching register.

PIN CONFIGURATION (Top View)

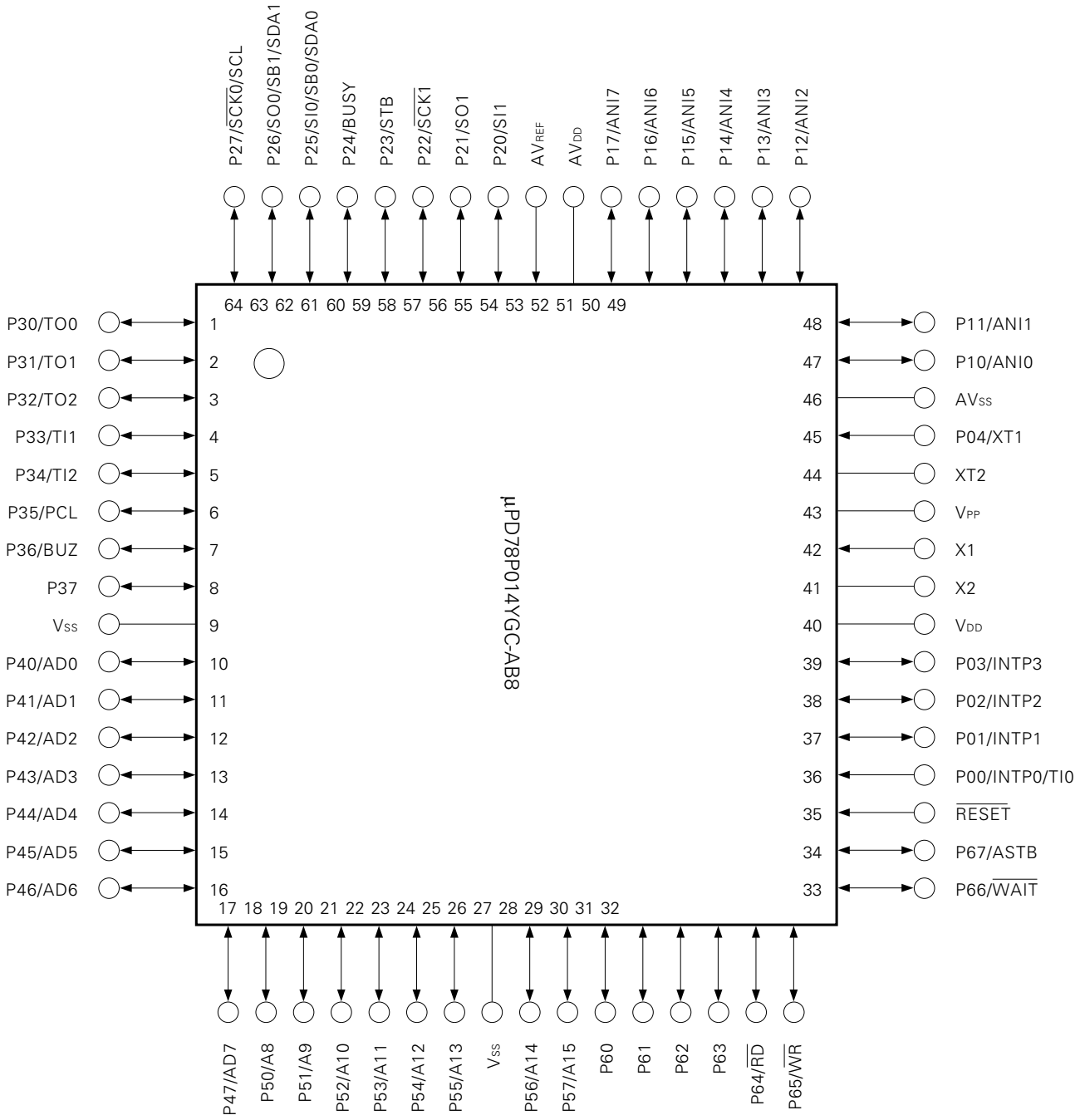
(1) Normal Operating Mode

64-pin plastic shrink DIP (750 mil)
64-pin ceramic shrink DIP (with window) (750 mil)



Cautions 1. Directly connect the V_{PP} pin to V_{SS}.
2. Connect the AV_{DD} pin to V_{DD}.
3. Connect the AV_{SS} pin to V_{SS}.

64-pin plastic QFP (14 × 14 mm)



Cautions 1. Directly connect the V_{PP} pin to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

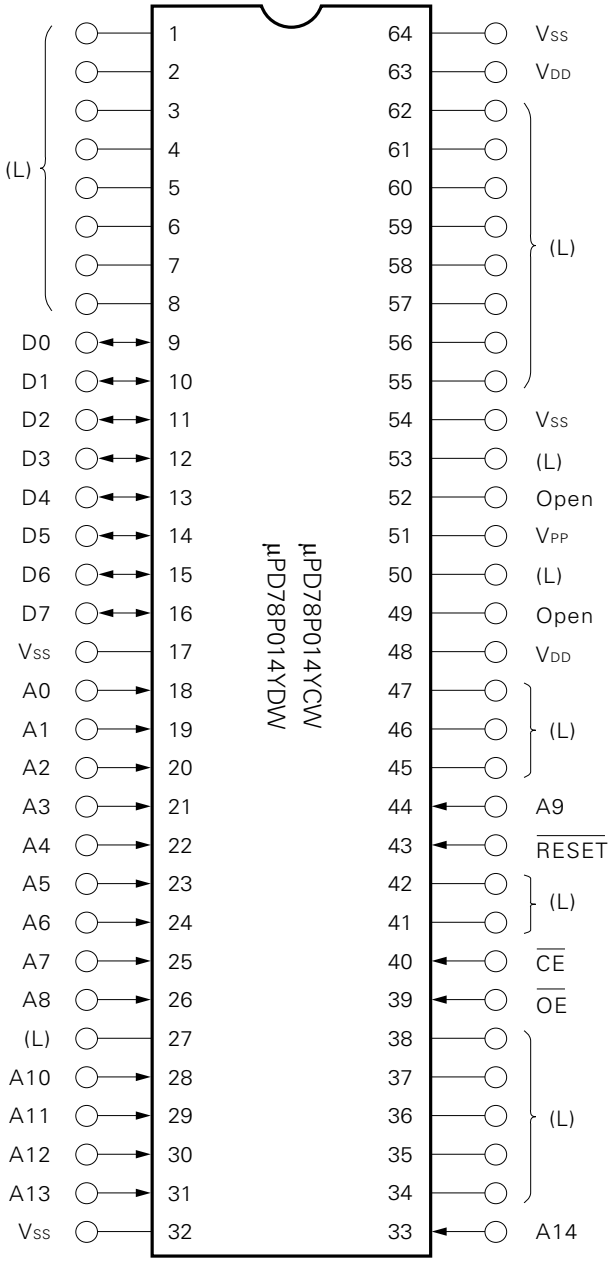
3. Connect the AV_{SS} pin to V_{SS}.

P00 to P04	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
INTP0 to INTP3	:	Interrupt From Peripherals
TI0 to TI2	:	Timer Input
TO0 to TO2	:	Timer Output
SB0, SB1	:	Serial Bus
SI0, SI1	:	Serial Input
SO0, SO1	:	Serial Output
$\overline{SCK0}$, $\overline{SCK1}$	:	Serial Clock
SCL	:	Serial Clock
SDA0, SDA1	:	Serial Data
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock

STB	:	Strobe
BUSY	:	Busy
AD0 to AD7	:	Address/Data Bus
A8 to A15	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground

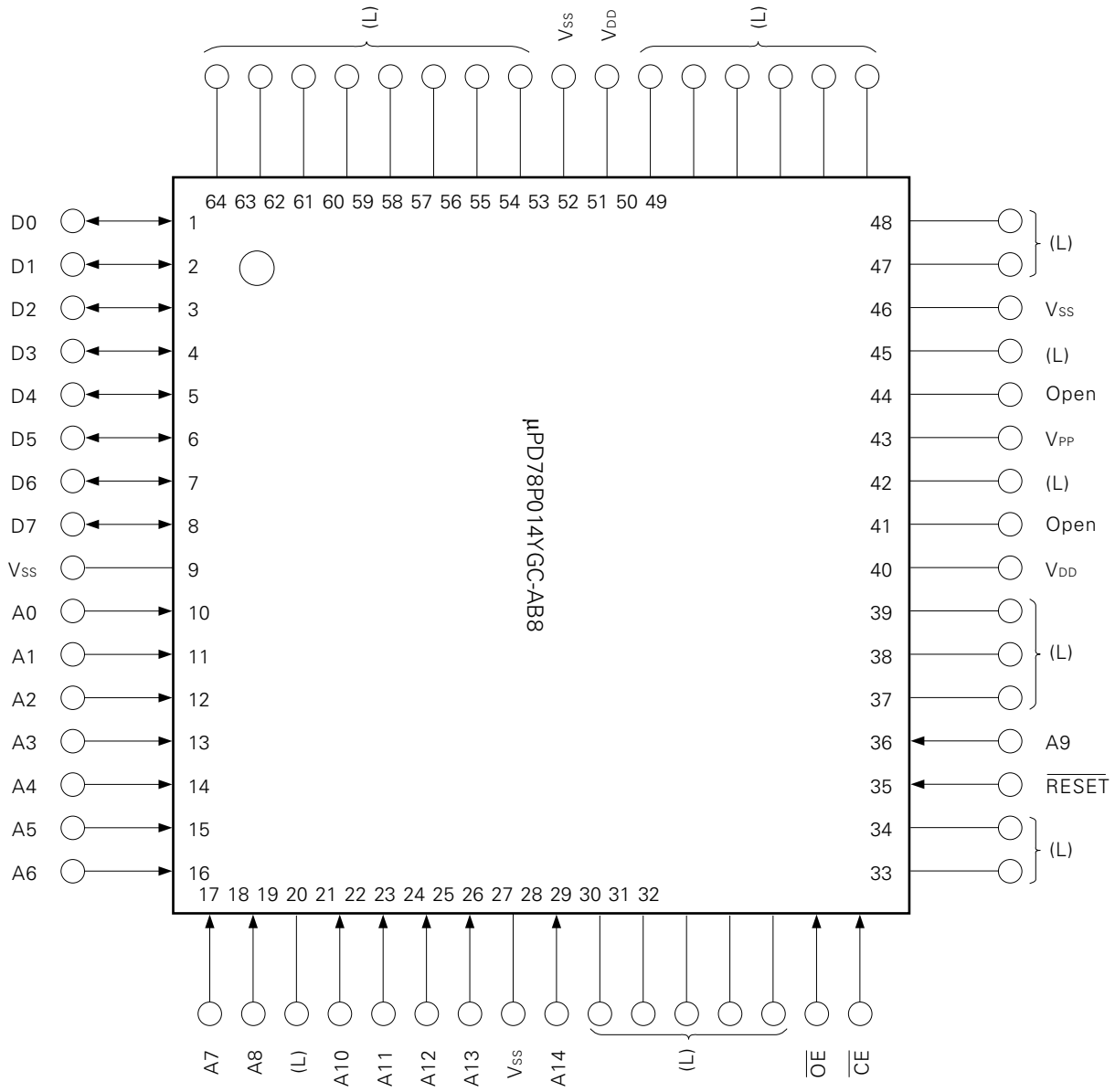
(2) PROM Programming Mode

64-pin plastic shrink DIP (750 mil)
64-pin ceramic shrink DIP (with window) (750 mil)



Cautions 1. (L) : Connect to VSS via individual pull-down resistors.
2. VSS : Connect to ground.
3. RESET : Set to low level.
4. Open : Do not connect.

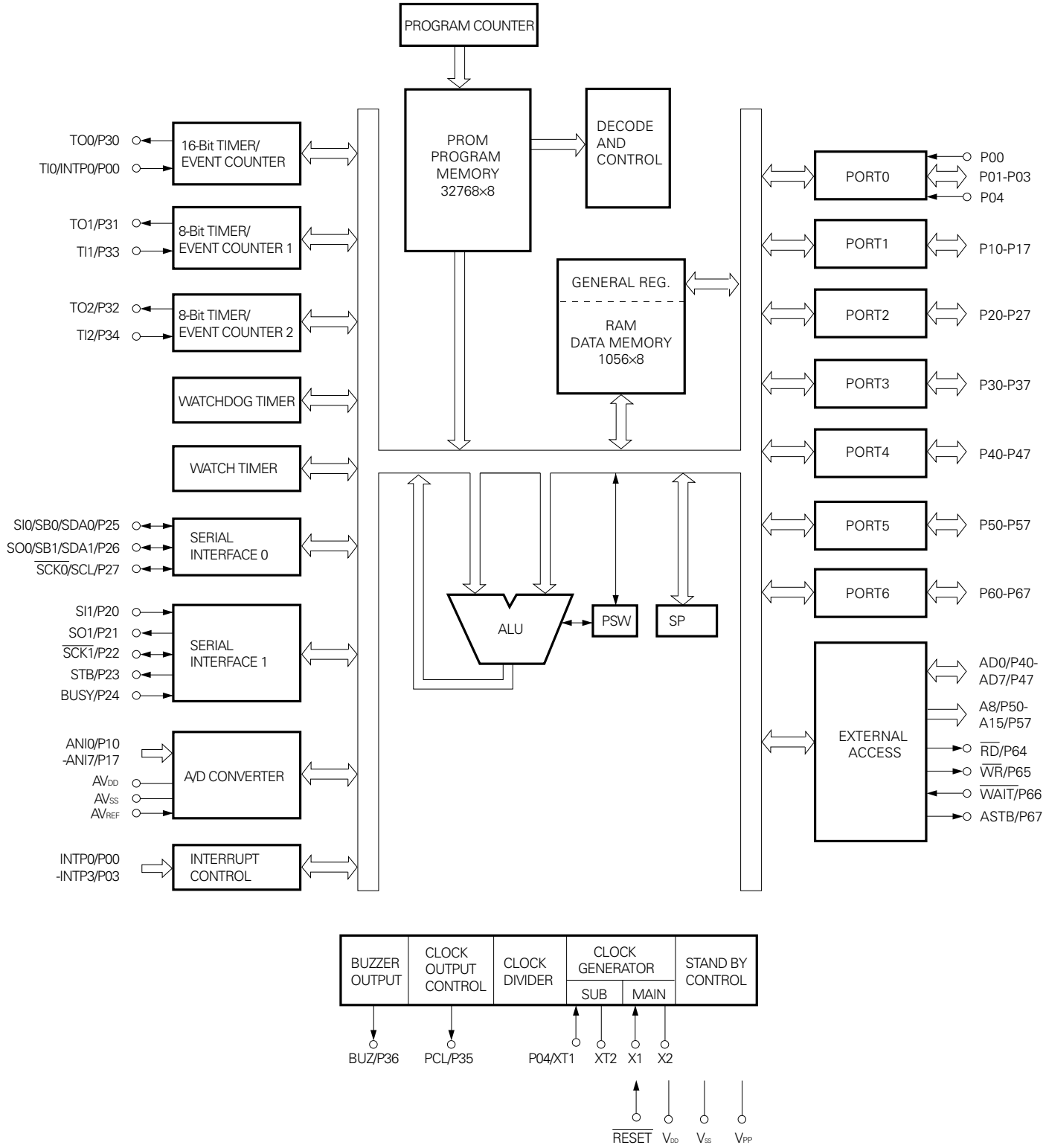
64-pin plastic QFP (14 × 14 mm)



Cautions 1. (L) : Connect to VSS via individual pull-down resistors.
2. VSS : Connect to ground.
3. RESET : Set to low level.
4. Open : Do not connect.

A0 to A14	: Address Bus	RESET	: Reset
D0 to D7	: Data Bus	VDD	: Power Supply
CE	: Chip Enable	VPP	: Programming Power Supply
OE	: Output Enable	VSS	: Ground

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P014Y AND MASK ROM VERSION

The μPD78P014Y incorporates one-time PROM which can be written to once only, or EPROM to which programs can be written, erased and rewritten.

By setting the internal memory switching register it is possible to make the functions of this device, except for the PROM specification and mask option for pins P60 to P63, identical to those of a mask ROM version.

The differences between the μPD78P014Y and mask ROM versions are shown in Table 1-1.

Table 1-1. Differences Between The μPD78P014Y and Mask ROM Version

Item	μPD78P014Y	Mask ROM Version
IC pin	No	Yes
V_{PP} pin	Yes	No
Mask option for pins P60 to P63	No mask option for incorporation of pull-up resistor	Pull-up resistor incorporation possible by means of mask option

Caution In the μPD78P014Y, the capacity of the internal PROM and internal high-speed RAM can be changed by means of the internal memory switching register.
After $\overline{\text{RESET}}$ input, the internal PROM capacity is 32K bytes, and the internal high-speed RAM capacity is 1024 bytes.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port Pins (1/2)

Pin name	I/O	Function		After reset	Alternate function
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software[Note 2].		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK0}}$/SCL
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified bit wise. When used as an input port, pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be used by software. (Test input flag (KRIF) is set to 1 by falling edge detection.)		Input	AD0 to AD7

Notes 1. When using the P04/XT1 pin as an input port, processor clock control register bit 6 (FRC) should be set to 1 (The feedback resistor of the subsystem clock oscillator should not be used.).

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, pull-up resistor is automatically disconnected.

(1) Port Pins (2/2)

Pin name	I/O	Function		After reset	Alternate function
P50 to P57	Input/ output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/ output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/ output port. Direct LED drive capability.	Input	—
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be used by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB

(2) Non-Port Pins (1/2)

Pin name	I/O	Function	After reset	Alternate function
INTP0	Input	Valid edge specification possible (rising edge, falling edge, or both rising edge and falling edges). External interrupt input.	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt input.	Input	P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0/SDA0
SI1				P20
SO0	Output	Serial interface serial data output.	Input	P26/SB1/SDA1
SO1				P21
SB0	Input/ output	Serial interface serial data input/output.	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{\text{SCK0}}$	Input/ output	Serial interface serial clock input/output.	Input	P27/SCL
SCL				P27/$\overline{\text{SCK0}}$
$\overline{\text{SCK1}}$				P22
STB	Output	Serial interface automatic transmission/reception strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmission/reception busy input.	Input	P24
TI0	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (also used as 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock and subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input/ output	Low address/data bus when memory is expanded externally.	Input	P40 to P47
A8 to A15	Output	High address bus when memory is expanded externally.	Input	P50 to P57
$\overline{\text{RD}}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{\text{WR}}$		External memory write operation strobe signal output.	Input	P65
$\overline{\text{WAIT}}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Output of strobe which externally latches address data to be output to ports 4 and 5 when accessing external memory.	Input	P67

(2) Non-Port Pins (2/2)

Pin name	I/O	Function	After reset	Alternate function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal input.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal input.	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{PP}	—	(High voltage application for program write/verify. Directly connected to V_{SS} in normal operating mode.)	—	—
V_{SS}	—	Ground potential.	—	—

2.2 Pins in PROM Programming Mode

Pin name	I/O	Function
$\overline{RESET}$	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal to the $\overline{RESET}$ pin, the PROM programming mode is set.
V_{PP}	Input	PROM programming mode setting and high voltage application for program write/verify.
A0 to A14	Input	Address bus.
D0 to D7	Input/ Output	Data bus.
$\overline{CE}$	Input	PROM enable input/program pulse input.
$\overline{OE}$	Input	PROM read strobe input.
V_{DD}	—	Positive power supply.
V_{SS}	—	Ground potential.

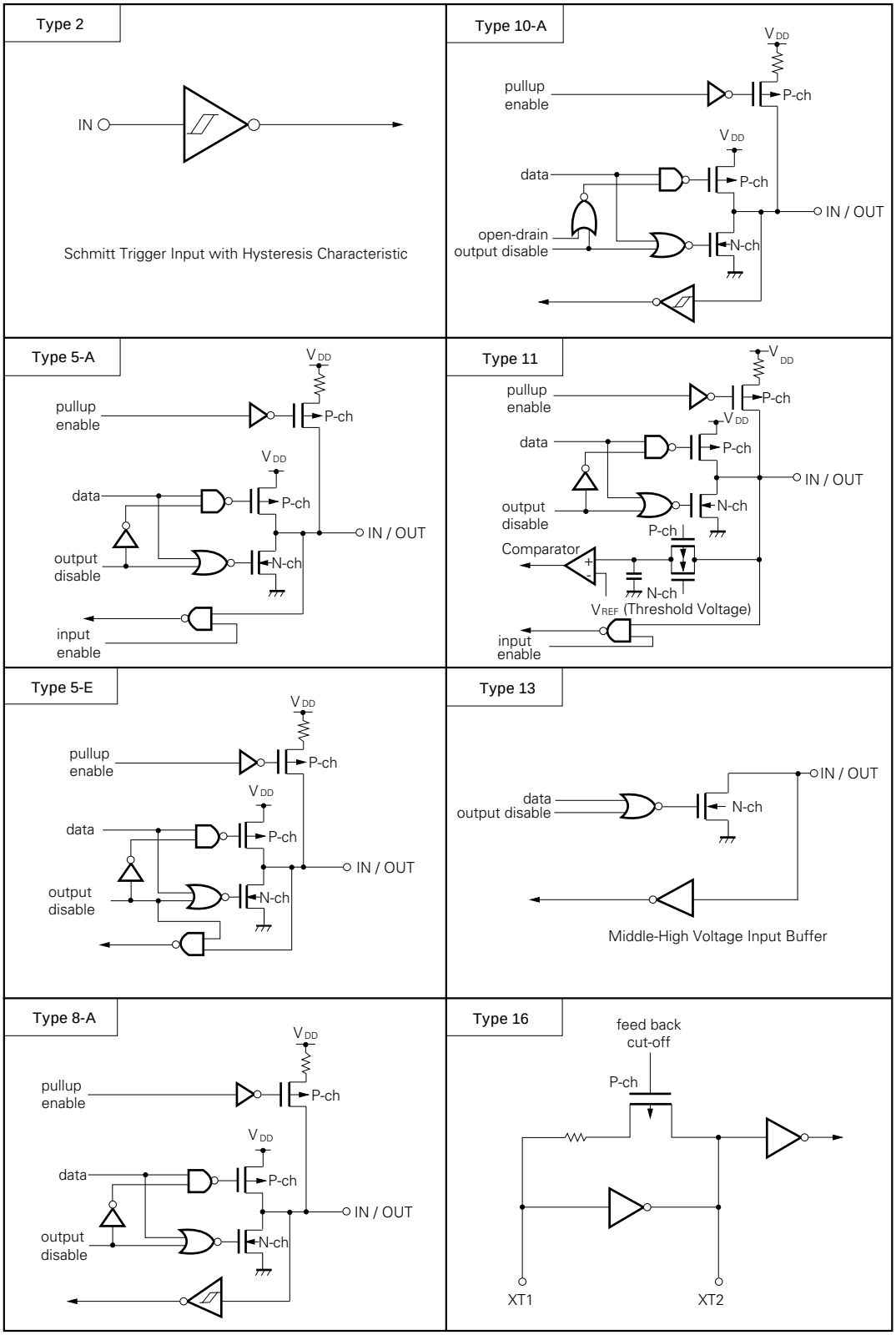
2.3 Pin I/O Circuits and Unused Pin Connections

Table 2-1 lists the I/O circuit type for all pins and the recommended connections for all unused pins.
Figure 2-1 shows the configuration of the Pin I/O Circuits.

Table 2-1. Types of Pin I/O Circuits

Pin name	I/O circuit type	I/O	Recommended connection for unused pins
P00/INTP0/TI0	2	Input	Connected to Vss .
P01/INTP1	8-A	Input/output	Input : Connected to Vss . Output: Leave open.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connected to Vss .
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connected to VDD or Vss . Output: Leave open.
P20/SI1	8-A	Input/output	Input : Connected to VDD or Vss . Output: Leave open.
P21/SO1	5-A		
P22/$\overline{\text{SCK1}}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{\text{SCK0}}$/SCL			
P30/TO0	5-A	Input/output	Input : Connected to VDD or Vss . Output: Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/output	Input : Connected to VDD or Vss . Output: Leave open.
P50/A8 to P57/A15	5-A	Input/output	Input : Connected to VDD or Vss . Output: Leave open.
P60 to P63	13		
P64/$\overline{\text{RD}}$	5-A		
P65/$\overline{\text{WR}}$			
P66/$\overline{\text{WAIT}}$			
P67/ASTB			
$\overline{\text{RESET}}$	2	Input	—
XT2	16	—	Leave open.
AVREF	—		Connected to Vss .
AVDD			Connected to VDD.
AVss			Connected to Vss.
VPP			Directly connected to Vss.

Figure 2-1. Pin I/O Circuits



3. INTERNAL MEMORY SWITCHING REGISTER (IMS)

This register is used to prevent part of the memory from being used by software. Setting the internal memory switching register enables memory mapping identical to that of a mask ROM version with different internal memory (ROM and RAM) to be used.

The IMS register is set by an 8-bit memory operation instruction.

$\overline{\text{RESET}}$ input sets this register to C8H.

Figure 3-1. Internal Memory Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	At Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	W

ROM3	ROM2	ROM1	ROM0	Internal ROM Capacity Selection
0	0	0	1	4 K bytes
0	0	1	0	8 K bytes
0	1	0	0	16 K bytes
0	1	1	0	24 K bytes
1	0	0	0	32 K bytes
Other than the above				Setting prohibited

RAM2	RAM1	RAM0	Internal High-Speed RAM Capacity Selection
0	0	0	768 bytes
0	0	1	640 bytes
0	1	0	512 bytes
0	1	1	384 bytes
1	0	0	256 bytes
1	0	1	Setting prohibited
1	1	0	1024 bytes
1	1	1	896 bytes

Table 3-1 lists IMS register settings for memory mapping equivalent to mask ROM versions.

Table 3-1. Examples of IMS Register Settings

Target Mask ROM Version	IMS Set Value	Target Mask ROM Version	IMS Set Value
μPD78001BY	82H	μPD78012BY	44H
μPD78002BY	64H	μPD78013Y	C6H
μPD78011BY	42H	μPD78014Y	C8H

4. PROM PROGRAMMING

The μPD78P014Y incorporates a 32K-byte PROM as program memory. When programming the μPD78P014Y, the PROM programming mode is set by means of the V_{PP} and $\overline{RESET}$ pins. For the connection of unused pins, see **"PIN CONFIGURATION, (2) PROM Programming Mode"**.

4.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{RESET}$ pin, the μPD78P014Y enters the programming mode. This mode can be set to operation mode by setting the $\overline{CE}$ pin and $\overline{OE}$ pin as shown in Table 4-1 below.

In addition, the PROM contents can be read by setting the read mode.

Table 4-1. PROM Programming Operating Modes

Operating Mode \ Pins	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	D0 to D7
Program write	L	+12.5 V	+6 V	L	H	Data input
Program verify				H	L	Data output
Program inhibit				H	H	High-impedance
Read		+5 V	+5 V	L	L	Data output
Output disable				L	H	High-impedance
Standby				H	L/H	High-impedance

4.2 PROM Writing Procedure

The PROM writing procedure is as shown below, allowing high-speed writing.

(1) Fix the $\overline{\text{RESET}}$ pin low. Supply +5 V to the V_{PP} pin. Unused pins should be handled as shown in **"PIN CONFIGURATION, (2) PROM Programming Mode"**.
(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(3) Provide the initial address.
(4) Provide the write data.
(5) Provide a 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Verify mode. If written, go to (8); if not written, repeat (4) to (6). When the write operation has been repeated 25 times, go to (7).
(7) Halt write operation due to defective device.
(8) Provide write data (times repeated in (4) to (6)) x 3 ms program pulse (additional write).
(9) Increment the address.
(10) Repeat (4) to (9) until the final address.

Timing for steps (2) to (8) above is shown in Figure 4-1.

Figure 4-1. PROM Write/Verify Timing

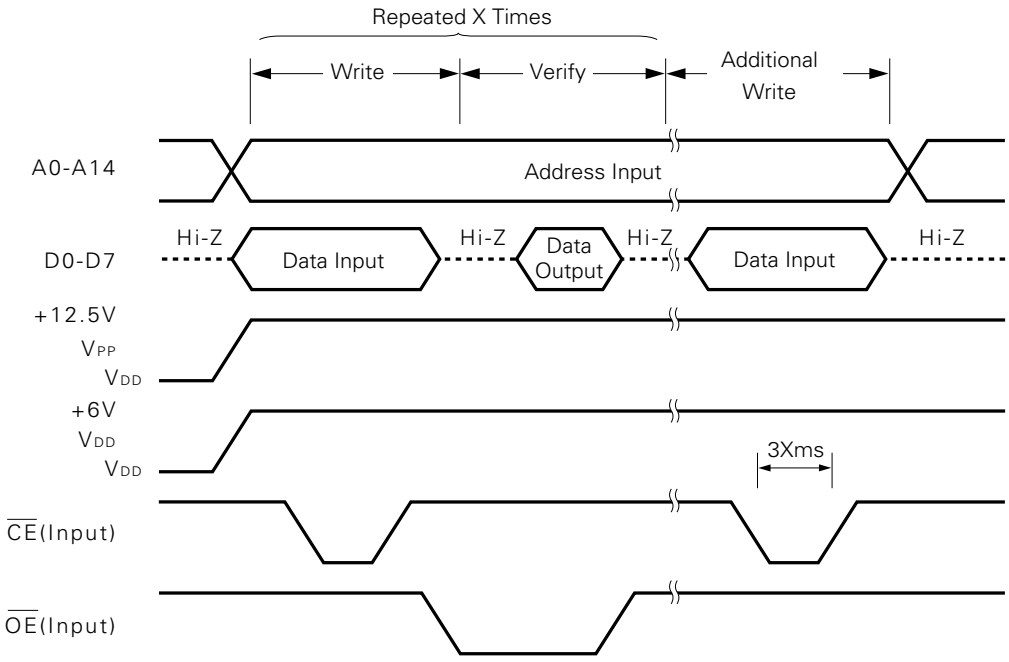
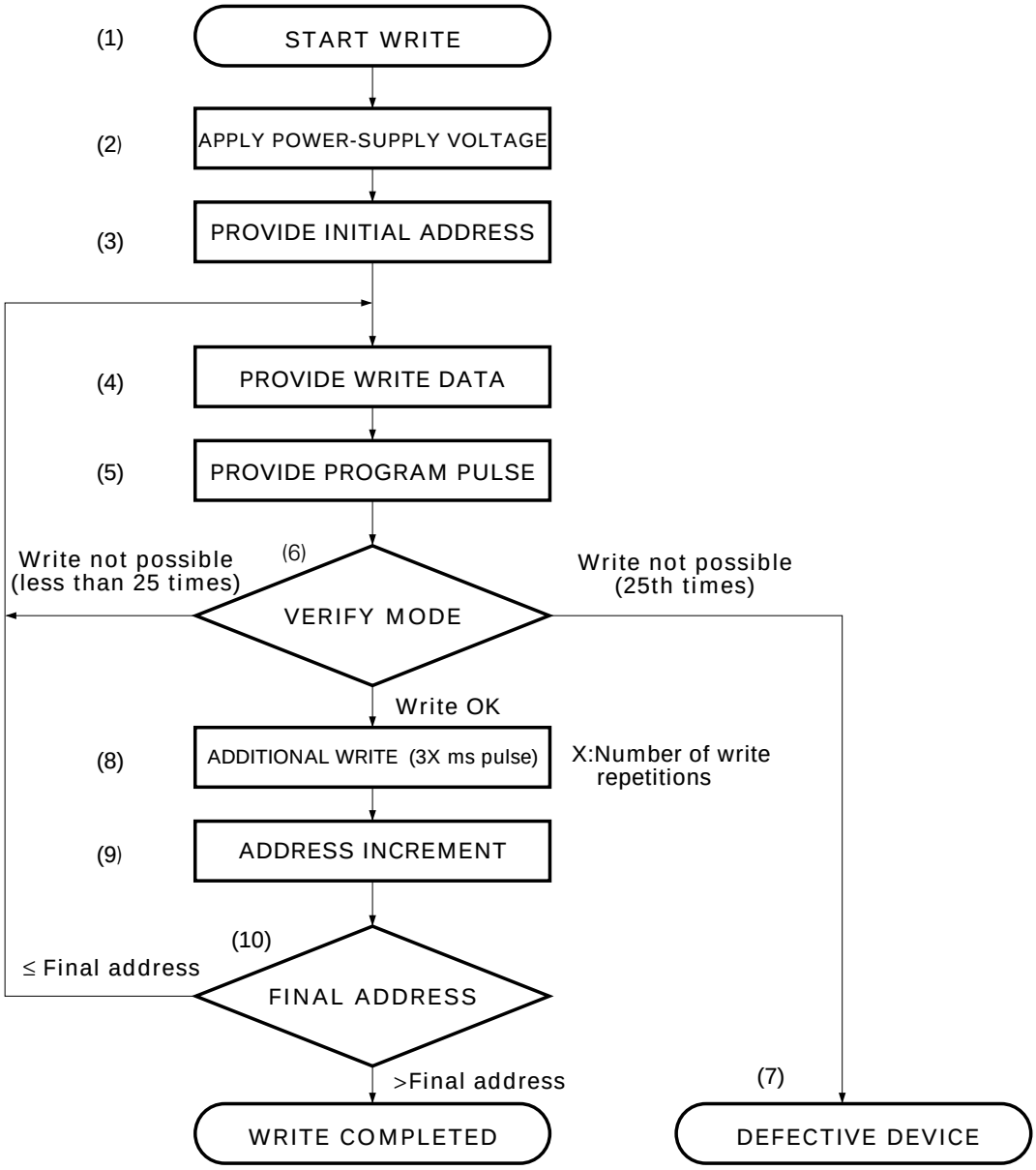


Figure 4-2. Write Procedure Flowchart



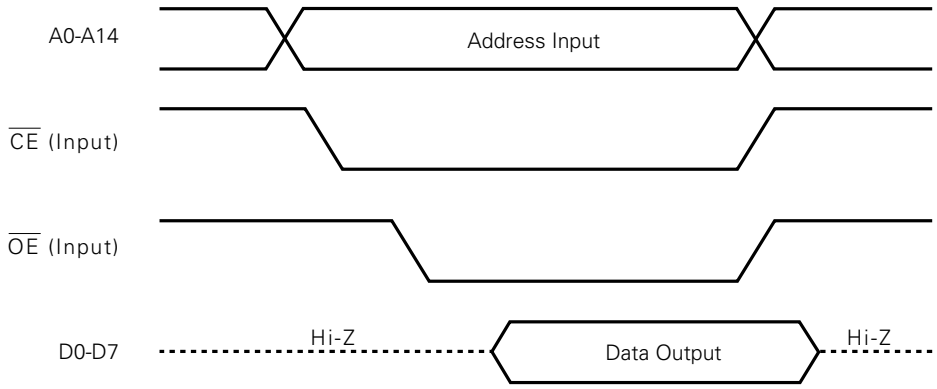
4.3 PROM Reading Procedure

PROM contents can be read onto the external data bus (D0 to D7) using the following procedure.

(1) Fix the $\overline{\text{RESET}}$ pin low. Supply +5 V to the V_{PP} pin. Unused pins should be handled as shown in **"PIN CONFIGURATION, (2) PROM Programming Mode"**.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of data to be read to pins A0 to A14.
(4) Read mode.
(5) Output data to pins D0 to D7.

Timing for steps (2) to (5) above is shown in Figure 4-3.

Figure 4-3. PROM Read Timing



5. ERASURE PROCEDURE (μPD78P014YDW ONLY)

With the μPD78P014YDW, it is possible to erase (set to FFH) data written to the program memory, and rewrite the memory.

The data can be erased by exposing the window to light with a wavelength of approximately 400 nm or shorter. Usually, exposure is performed with ultraviolet light with a wavelength of 254 nm. The amount of exposure required for complete erasure is shown below.

- UV intensity × erasure time: 15 W•s/cm^2 or more
- Erasure time: 15 to 20 minutes (using a 12,000 μW/cm^2 ultraviolet lamp. A longer erasure time may be required in case of deterioration of the ultraviolet lamp or dirt on the package window).

Erasure should be carried out with the ultraviolet lamp placed at a distance of 2.5 cm or less from the window. If the ultraviolet lamp is fitted with a filter, this should be removed before performing exposure.

6. OPAQUE FILM FOR ERASURE WINDOW (μPD78P014YDW ONLY)

To protect from unintentional erasure by light sources other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by light sources, stick an opaque film on the erasure window except when erasing the EPROM contents.

7. ONE-TIME PROM VERSIONS SCREENING

The one-time PROM version (μPD78P014YCW, μPD78P014YGC-AB8) can not be tested completely by NEC before it is shipped, because of its structure.

It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125 °C	24 hours

NEC provides charged services for one-time PROM writing, marking, screening, and verification, under the name "QTOP Microcomputer". Contact NEC for details. ★

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_a = 25 °C)

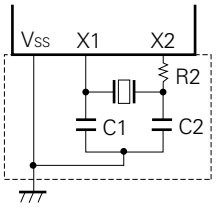
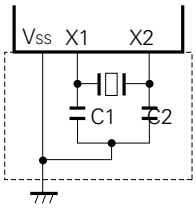
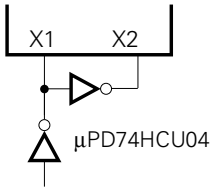
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P04, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	Open-drain	–0.3 to +16	V
	V_{I3}	A9	In PROM programming mode	–0.3 to +13.5	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} –0.3 to AV_{REF} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		P10 to P17, P20 to P27, P30 to P37 total		–15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		–15	mA
Output current low	I_{OL}**Note**	1 pin	Peak value	30	mA
			Effective value	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			Effective value	20	mA
		P10 to P17, P20 to P27 P30 to P37 total	Peak value	50	mA
			Effective value	20	mA
Operating temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The effective value should be calculated as follows: [Effective value] = [Peak value] $\times\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute ratings are not exceeded.

Remark Unless otherwise specified, the dual-function pin characteristics are the same as the port pin characteristics.

Main System Clock Oscillator Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X)**Note 1**	V_{DD} = oscillation voltage range	1		10	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reached the MIN. of the oscillation voltage range.			4	ms
Crystal resonator		Oscillator frequency (f_X)**Note 1**		1	8.38	10	MHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X)**Note 1**		1.0		10.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		42.5		500	ns

Notes 1. Shows the oscillator characteristics only. For the instruction execution time, see the AC characteristics.

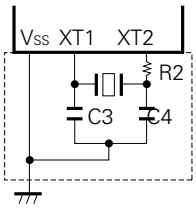
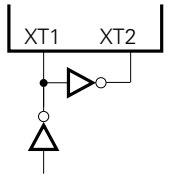
2. Time necessary for oscillation to stabilize after reset or STOP mode released.

Cautions 1. When the main system clock oscillator is used, the area inside dotted lines in the figure should be wired as follows to prevent influence from the wiring capacitance.

- **Wiring should be as short as possible.**
- **Do not cross other signal lines.**
- **Do not place the oscillator close to line in which varying high current flows.**
- **Potential at the oscillator capacitor connecting point should be always the same as V_{SS}.**
- **Do not ground to the ground pattern in which high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})**Note 1**		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Shows the oscillator characteristics only. For the instruction execution time, see the AC characteristics.

2. Time necessary for oscillation to stabilize after V_{DD} reaches MIN. of the oscillation voltage range.

Cautions 1. When the subsystem clock oscillator is used, the area inside dotted lines in the figure should be wired as follows to prevent influence from the wiring capacitance.

- **Wiring should be as short as possible.**
- **Do not cross other signal lines.**
- **Do not place the oscillator close to line in which varying high current flows.**
- **Potential at the oscillator capacitor connecting point should be always the same as V_{SS}.**
- **Do not ground to the ground pattern in which high current flows.**
- **Do not fetch signals from the oscillator.**

2. In the subsystem clock oscillator, which is designed to be a circuit with low amplification ratio to suppress current consumption, misoperation due to noise occurs more often than in the main system clock oscillator. Therefore, when using the subsystem clock, special care should be taken in wiring.

RECOMMENDED OSCILLATOR CONSTANT

Main System Clock: Ceramic Resonator (T_a = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg.	CSB1000J	1.00	100	100	6.8	2.8	6.0
	CSB××××J	1.01 to 1.25	100	100	4.7	2.8	6.0
	CSA×.×××MK	1.26 to 1.79	100	100	0	2.8	6.0
	CSA×.××MG093	1.80 to 2.44	100	100	0	2.7	6.0
	CST×.××MG093		On-chip	On-chip	0	2.7	6.0
	CSA×.××MG	2.45 to 4.18	30	30	0	2.7	6.0
	CST×.××MGW		On-chip	On-chip	0	2.7	6.0
	CSA×.××MGU	4.19 to 6.00	30	30	0	2.7	6.0
	CST×.××MGWU		On-chip	On-chip	0	2.7	6.0
	CSA×.××MT	6.01 to 10.0	30	30	0	3.0	6.0
	CST×.××MTW		On-chip	On-chip	0	3.0	6.0

Remark ×.××, ×.×××, and ×××× indicate the frequency.

Subsystem Clock: Crystal Resonator (T_a = –40 to +60 °C)

Manufacturer	Product Name	Frequency (kHz)	Recommended Oscillator Constant			Oscillation Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN.(V)	MAX.(V)
Daishinku Corporation	DT-38 (1TA632E00, load capacitance 6.3 pF)	32.768	10	10	100	2.7	6.0

Capacitance (T_a = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f=1 MHz unmeasured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	f=1 MHz unmeasured pins returned to 0 V.	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	pF
			P60 to P63			20	pF

Remark Unless otherwise specified, the dual-function pin characteristics are the same as the port pin characteristics.

DC Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63	Open-drain	0.7 V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	V_{DD} = 4.5 to 6.0 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.3		V_{DD}	V
Input voltage low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67		0		0.3 V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	P60 to P63	V_{DD} = 4.5 to 6.0 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P04, XT2	V_{DD} = 4.5 to 6.0 V	0		0.4	V
				0		0.3	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 6.0 V, open-drain, pulled-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			–20	μA

Remark Unless otherwise specified, the dual-function pin characteristics are the same as the port pin characteristics.

DC Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R_2	V_{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ
Supply current[Note3]	I_{DD1}	8.38 MHz Crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 %[Note 1]		9	27	mA
			V_{DD} = 3.0 V ± 10 %[Note 2]		1	3	mA
	I_{DD2}	8.38 MHz Crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10 %		550	1650	μA
	I_{DD3}	32.768 kHz Crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 %		90	180	μA
			V_{DD} = 3.0 V ± 10 %		50	100	μA
	I_{DD4}	32.768 kHz Crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		25	50	μA
			V_{DD} = 3.0 V ± 10 %		5	10	μA
	I_{DD5}	XT1 = 0 V STOP mode When feedback resistor is used	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode When feedback resistor is not used	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA

Notes 1. Operating in high-speed mode (when the processor clock control register is set to 00H).

2. Operating in slow-speed mode (when the processor clock control register is set to 04H).

3. Excluding AV_{REF} current and port current.

Remark Unless otherwise specified, the dual-function pin characteristics are the same as the port pin characteristics.

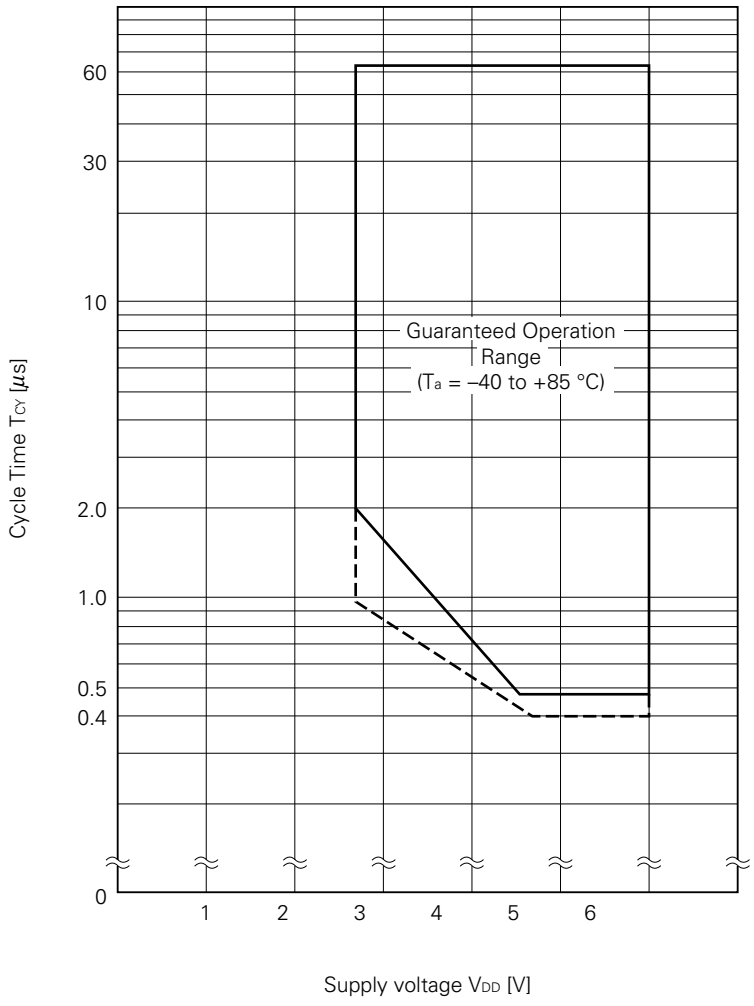
AC CHARACTERISTICS

(1) Basic Operation (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.48		64	μs
				1.91		64	μs
			T_a = –40 to +40 °C V_{DD} = 4.75 to 6.0 V	0.4		64	μs
			T_a = –40 to +40 °C	0.96		64	μs
		Operating on subsystem clock		40	122	125	μs
TI input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		4	MHz
				0		275	kHz
TI input high-/low-level width	t_{TIH}	V_{DD} = 4.5 to 6.0 V		100			ns
	t_{TIL}			1.8			μs
Interrupt input high-/low-level width	t_{INTH}	INTP0		$8/f_{sam}$ **Note**			μs
	t_{INTL}	INTP1 to INTP3		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Note In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of f_{sam} is possible between $f_X/2^{N+1}$, $f_X/64$ and $f_X/128$ (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock operation)



Caution When T_a = –40 to +40 °C, the guaranteed operation range is extended to the broken line.

(2) Read/Write Operation (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		$0.5t_{CY}$ – 30		ns
Address hold time	t_{ADH}	Load resistor ∞5 kΩ	10		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 50	ns
	t_{ADD2}		5	$(3 + 2n)t_{CY}$ – 100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			$(1 + 2n)t_{CY}$ – 25	ns
	t_{RDD2}			$(2.5 + 2n)t_{CY}$ – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 20		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			$0.5t_{CY}$	ns
	t_{RDWT2}			$1.5t_{CY}$	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			$0.5t_{CY}$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}		5		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.5 + 2n)t_{CY}$ – 20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		$0.5t_{CY}$ – 30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		$1.5t_{CY}$ – 30		ns
ASTB∞ delay time from $\overline{RD}$∞ in external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 40	ns
Address hold time from $\overline{RD}$∞ in external fetch	t_{RDADH}		t_{CY}	t_{CY} + 50	ns
Write data output time from $\overline{RD}$∞	t_{RDWD}		10		ns
$\overline{WR}$↓ delay time from write data	t_{WDWR}	V_{DD} = 4.5 to 6.0 V	$0.5t_{CY}$ – 120	$0.5t_{CY}$	ns
			$0.5t_{CY}$ – 170	$0.5t_{CY}$	ns
Address hold time from $\overline{WR}$∞	t_{WRADH}	V_{DD} = 4.5 to 6.0 V	t_{CY}	t_{CY} + 60	ns
			t_{CY}	t_{CY} + 100	ns
$\overline{RD}$∞ delay time from $\overline{WAIT}$∞	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 80	ns
$\overline{WR}$∞ delay time from $\overline{WAIT}$∞	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 80	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates number of waits.

3. C_L = 100 pF(C_L means the load capacitance of P40/AD0 to P47/AD7, P50/A8 to P57/A15, P64/$\overline{RD}$, P65/$\overline{WR}$, P66/$\overline{WAIT}$ and P67/ASTB pins.)

(3) Serial Interface (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2$ – 50			ns
	t_{KL1}			$t_{KCY1}/2$ – 150			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}			100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO1}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

Note C is the load capacitance of SO output line.

(b) 3-wire serial I/O mode ($\overline{SCK}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns	
				3200			ns	
$\overline{SCK}$ high-/low-level width	t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns	
	t_{KL2}			1600			ns	
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns	
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns	
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns	
						1000	ns	
$\overline{SCK}$ rise and fall times (For serial interface channel 0)	t_{R2} t_{F2}	When using the external device expansion function				160	ns	★
		When not using the external device expansion function	When using the 16-bit timer output function			700	ns	★
			When not using the 16-bit timer output function			1000	ns	★
$\overline{SCK}$ rise and fall times (For serial interface channel 1)	t_{R2}	When using the external device expansion function				160	ns	★
	t_{F2}	When not using the external device expansion function				1000	ns	★

Note C is the load capacitance of SO output line.

(c) SBI mode ($\overline{SCK}$...Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2$ - 50			ns
	t_{KL3}			$t_{KCY3}/2$ - 150			ns
SB0, SB1 setup time (to $\overline{SCK}\infty$)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK}\infty$)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK}\downarrow$	t_{KSO3}	R = 1 kΩ ,	V_{DD} = 4.5 to 6.0 V	0		250	ns
		C = 100 pF**Note**		0		1000	ns
SB0, SB1↓ from $\overline{SCK}\infty$	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance respectively of the SB0 and SB1 output line.

(d) SBI mode ($\overline{SCK}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns	
				3200			ns	
$\overline{SCK}$ high-/low-level width	t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns	
	t_{KL4}			1600			ns	
SB0, SB1 setup time (to $\overline{SCK}\infty$)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns	
				300			ns	
SB0, SB1 hold time (from $\overline{SCK}\infty$)	t_{KSI4}			$t_{KCY4}/2$			ns	
SB0, SB1 output delay time from $\overline{SCK}\downarrow$	t_{KSO4}	R = 1 kΩ ,	V_{DD} = 4.5 to 6.0 V	0		300	ns	
		C = 100 pF**Note**		0		1000	ns	
SB0, SB1↓ from $\overline{SCK}\infty$	t_{KSB}			t_{KCY4}			ns	
$\overline{SCK}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns	
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns	
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns	
$\overline{SCK}$ rise and fall times	t_{R4} t_{F4}	When using the external device expansion function				160	ns	★
		When not using the external device expansion function	When using the 16-bit timer output function			700	ns	★
			When not using the 16-bit timer output function			1000	ns	★

Note R and C are the load resistance and load capacitance respectively of the SB0 and SB1 output line.

(e) 2-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY5}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-level width	t_{KH5}	R = 1 kΩ, C = 100 pF**Note**		$t_{KCY5}/2 - 50$			ns
$\overline{SCK}$ low-level width	t_{KL5}			$t_{KCY5}/2 - 50$			ns
SB0, SB1 setup time (to $\overline{SCK}\uparrow$)	t_{SIK5}			300			ns
SB0, SB1 hold time (from $\overline{SCK}\uparrow$)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK}\downarrow$	t_{KSO5}	R = 1 kΩ,	V_{DD} = 4.5 to 6.0 V	0		250	ns
		C = 100 pF**Note**		0		1000	ns

Note R and C are the load resistance and load capacitance respectively of the $\overline{SCK0}$, SB0 and SB1 output line.

(f) 2-wire serial I/O mode ($\overline{SCK}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-level width	t_{KH6}			650			ns
$\overline{SCK}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK}\uparrow$)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK}\uparrow$)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK}\downarrow$	t_{KSO6}	R = 1 kΩ,	V_{DD} = 4.5 to 6.0 V	0		300	ns
		C = 100 pF**Note**		0		1000	ns
★ $\overline{SCK}$ rise and fall times	t_{R6} t_{F6}	When using the external device expansion function				160	ns
★		When not using the external device expansion function	When using the 16-bit timer output function			700	ns
★			When not using the 16-bit timer output function			1000	ns

Note R and C are the load resistance and load capacitance respectively of the $\overline{SCK0}$, SB0 and SB1 output line.

(g) I²C bus interface

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
SCL input clock frequency	f_{SCL}			0		100	kHz	
Bus release time before start of transfer	t_{BUF}			4.7			μs	
Start condition hold time	t_{HDSTA}			4.0			μs	
SCL low-level time	t_{LOW}			4.7			μs	
SCL high-level time	t_{HIGH}			4.0			μs	
Start condition setup time	t_{SUSTA}			4.7			μs	
Data hold time	t_{HDDAT}	SCL fall time: data retention		0			μs	
Data setup time	t_{SUDAT}	V_{DD} = 4.5 to 6.0 V		250			ns	
				700			ns	
SDA0, SDA1, SCL signal rise time	t_R Note 1	R = 2 kΩ, C = 100 pF Note 3				1000	ns	★
	t_R Note 2	When using the external device expansion function				160	ns	★
		When not using the external device expansion function	When using the 16-bit timer output function			700	ns	★
			When not using the 16-bit timer output function			1000	ns	★
SDA0, SDA1, SCL signal fall time	t_F	R = 2 kΩ, C = 100 pF Note 3				300	ns	
Stop condition setup time	t_{SUSTO}			4.7			μs	

Notes 1. When using the serial clock of the internal clock output.

2. When using the serial clock of the external clock input.

3. R and C are the load resistance and load capacitance respectively of the SCL, SDA0 and SDA1 output line.

(h) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK}$...Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KH7}	V_{DD} = 4.5 to 6.0 V		$t_{KCY7}/2 - 50$			ns
	t_{KL7}			$t_{KCY7}/2 - 150$			ns
SI setup time (to $\overline{SCK}\infty$)	t_{SIK7}			100			ns
SI hold time (from $\overline{SCK}\infty$)	t_{KSI7}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO7}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
STB∞ from $\overline{SCK}\infty$	t_{SBD}			400		t_{KCY7}	ns
Strobe signal high-level width	t_{SBW}			$t_{KCY7} - 30$		$t_{KCY7} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}			100			ns
$\overline{SCK}\downarrow$ from busy inactive	t_{SPS}					$2t_{KCY7}$	ns

Note C is the load capacitance of the SO output line.

(i) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
$\overline{SCK}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 6.0 V		800			ns	
				3200			ns	
$\overline{SCK}$ high-/low-level width	t_{KH8}	V_{DD} = 4.5 to 6.0 V		400			ns	
	t_{KL8}			1600			ns	
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK8}			100			ns	
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI8}			400			ns	
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO8}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns	
						1000	ns	
$\overline{SCK}$ rise and fall times	t_{R8}	When using the external device expansion function				160	ns	★
	t_{F8}	When not using the external device expansion function				1000	ns	★

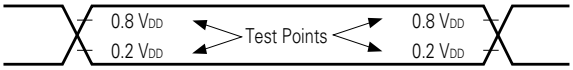
Note C is the load capacitance of the SO output line.

A/D Converter Characteristics (T_a = –40 to +85 °C, AV_{DD} = V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

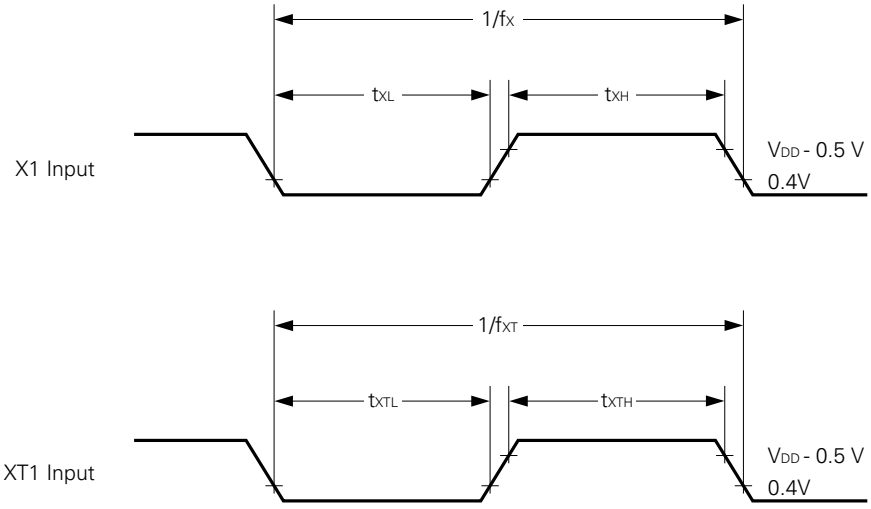
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]					0.6	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		24/f_x			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
AV_{REF} current	I_{REF}			0.5	1.5	mA

Note Overall error excluding quantization errors (±1/2 LSB). This represents a ratio to the full scale value.

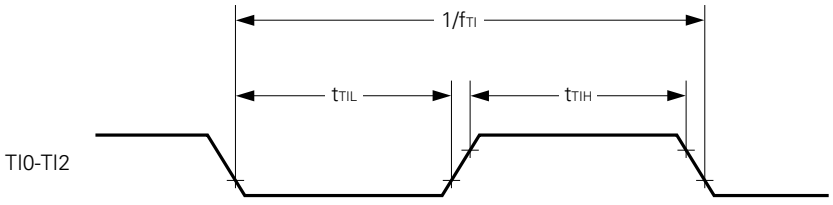
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

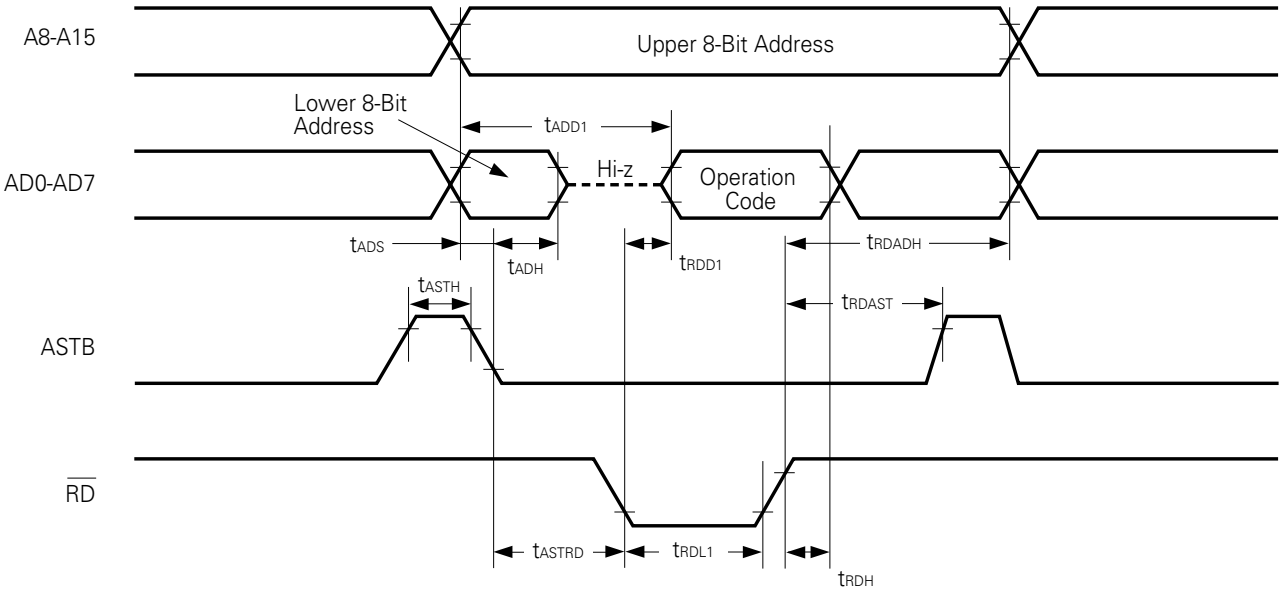


TI Timing

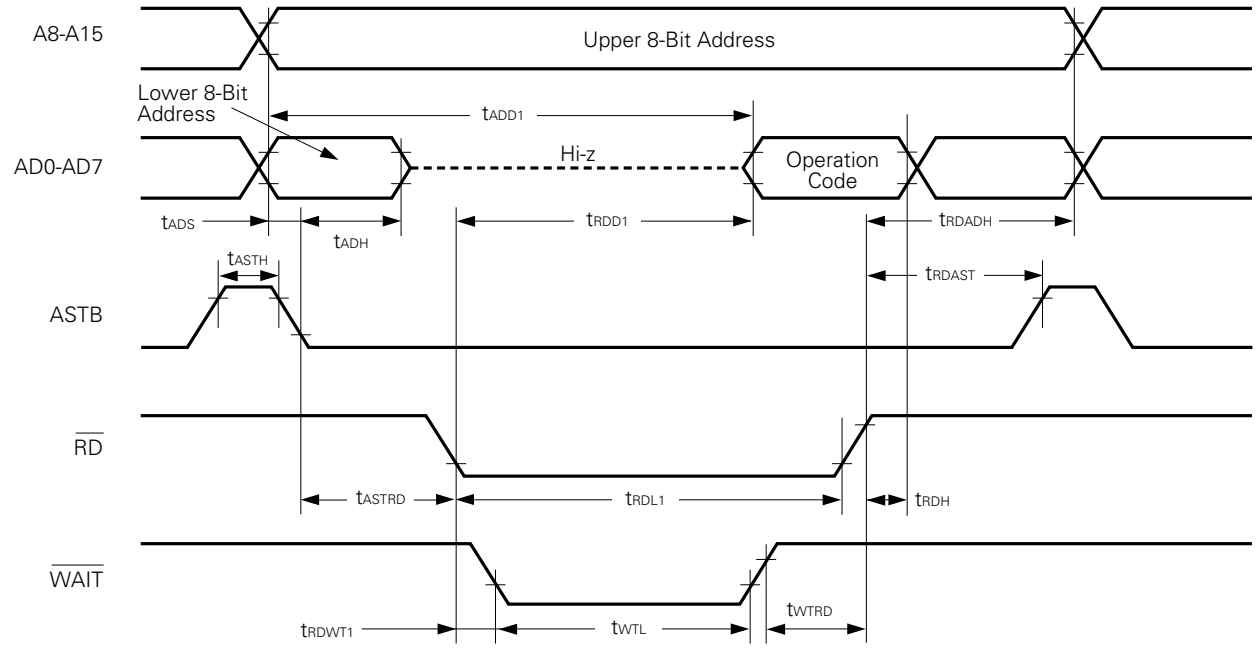


Read/Write Operation

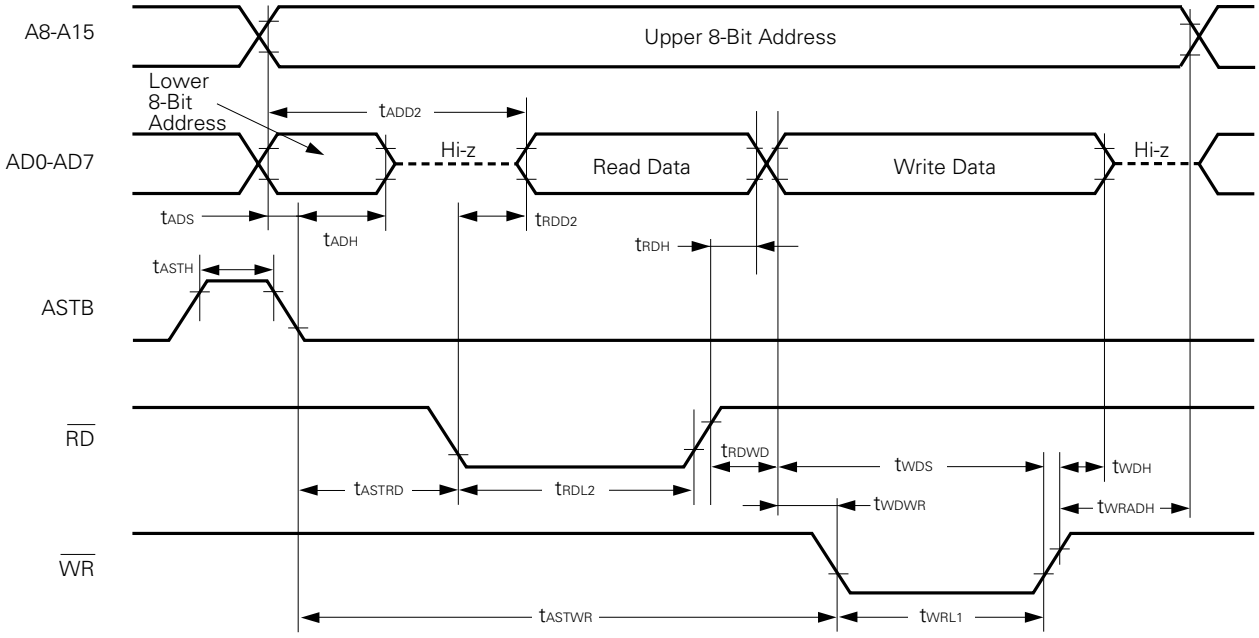
External fetch (no wait):



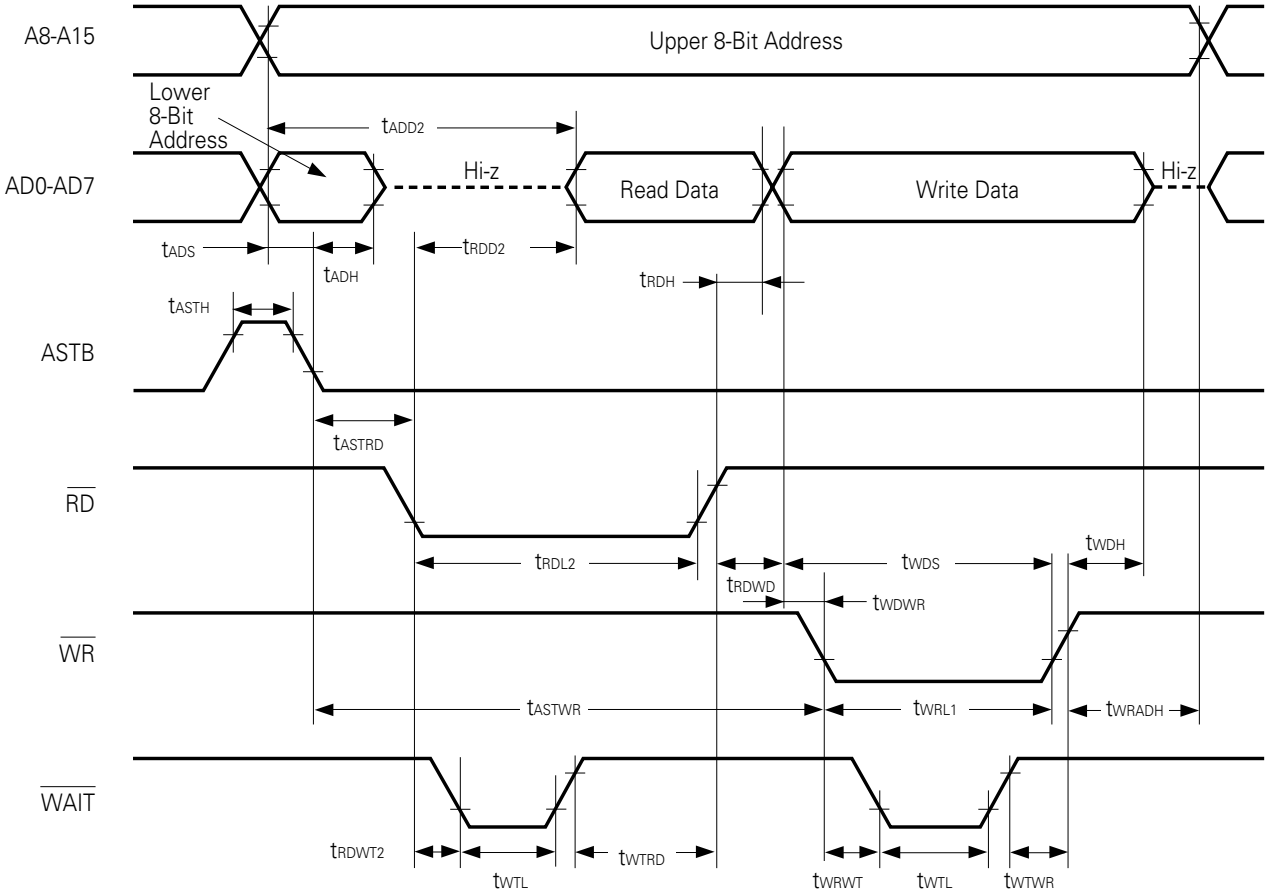
External fetch (wait insertion):



External data access (no wait):

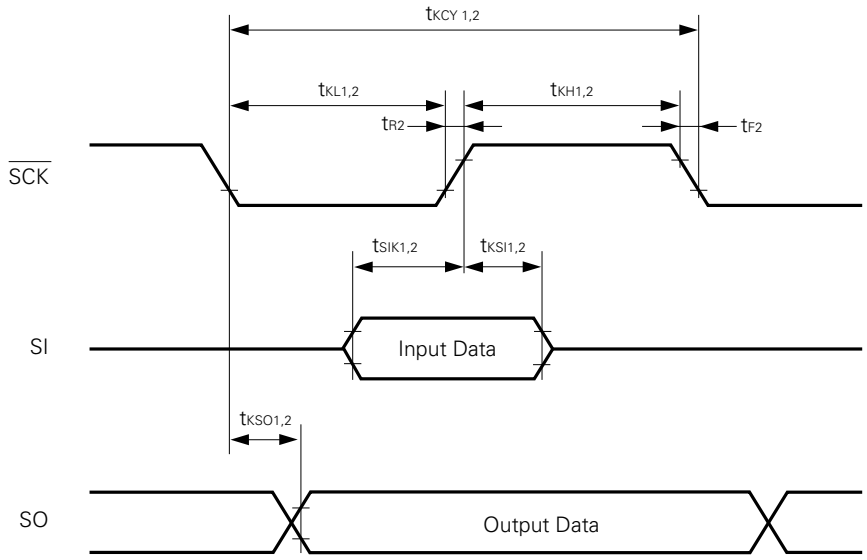


External data access (wait insertion):



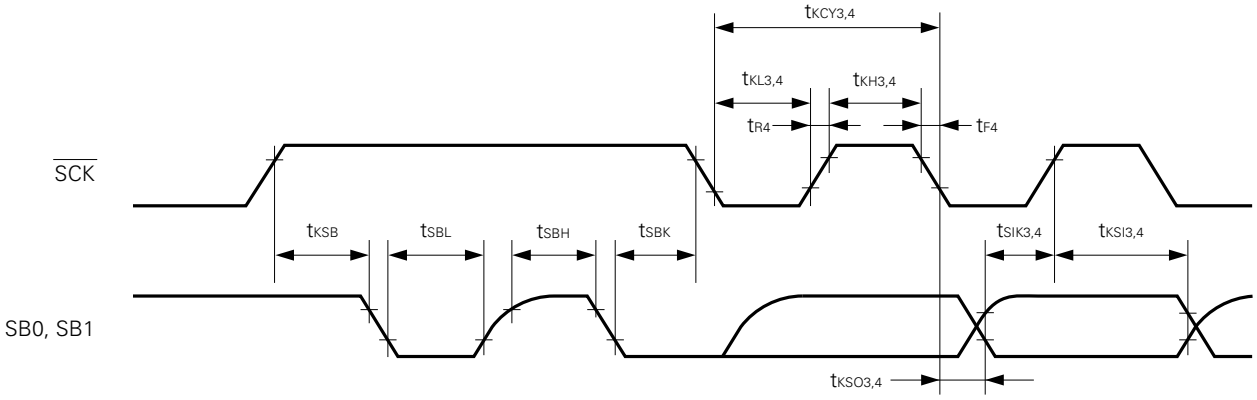
Serial Transfer Timing

3-wire serial I/O mode:



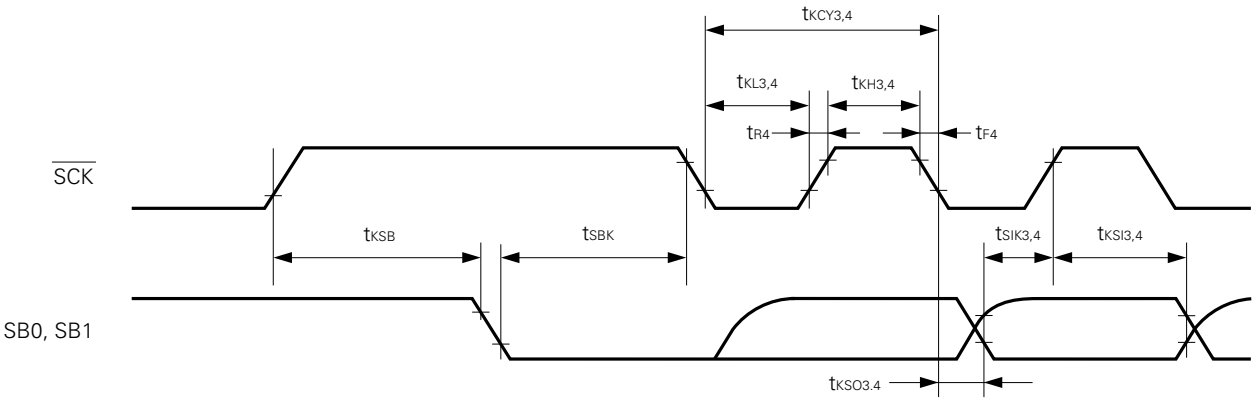
★

SBI mode (bus release signal transfer):



★

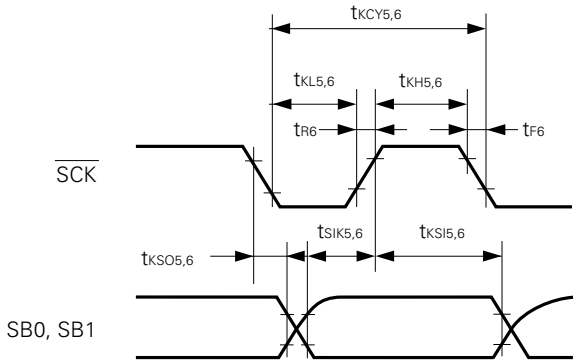
SBI mode (command signal transfer):



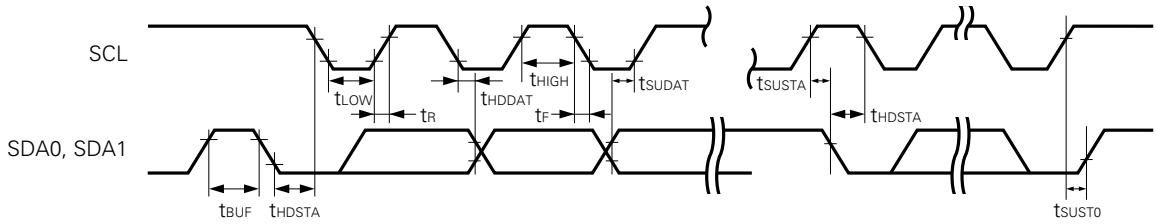
★

2-wire serial I/O mode:

★

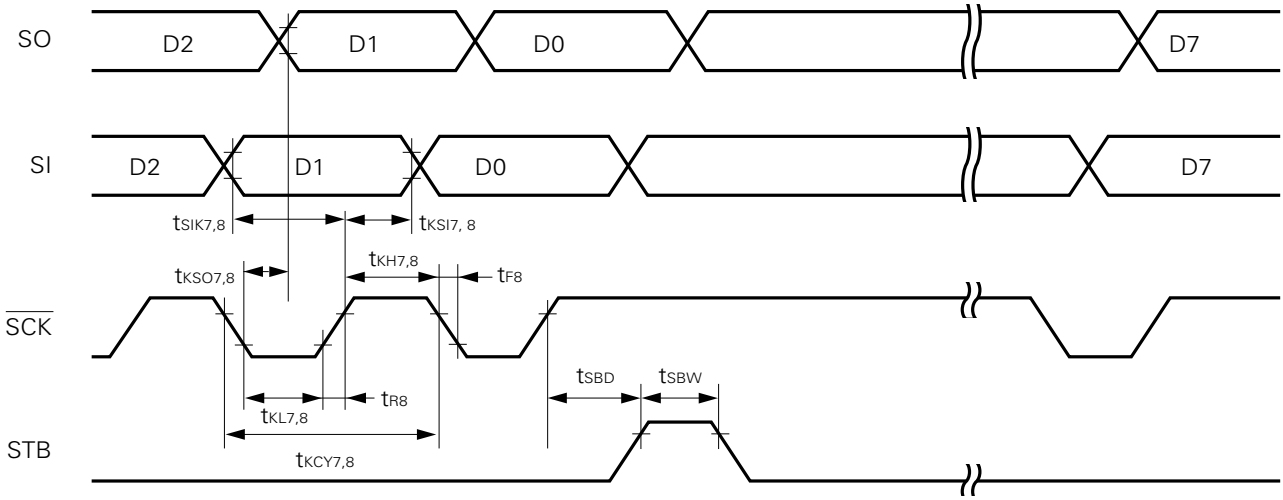


I²C bus mode:

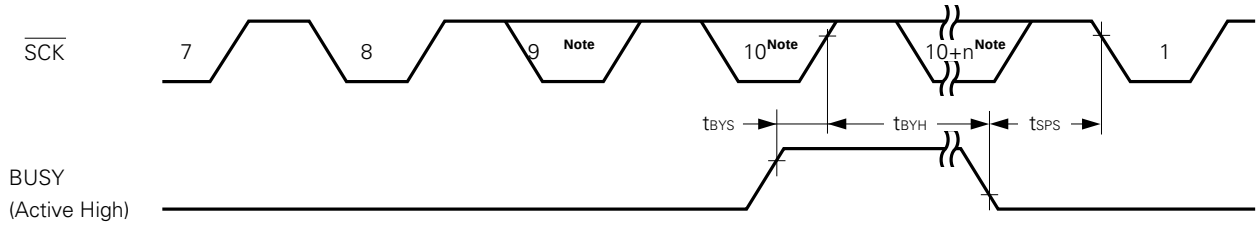


3-wire serial I/O mode with automatic transmit/receive function:

★



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



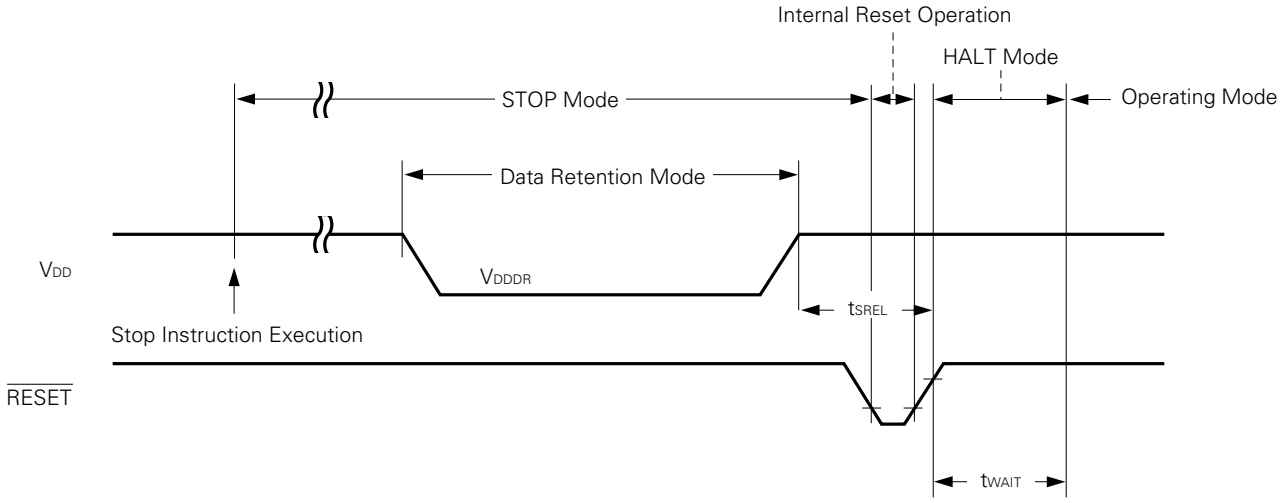
Note These portions of the signal are actually not low but are so described due to the timing specification.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_a = –40 to +85 °C)

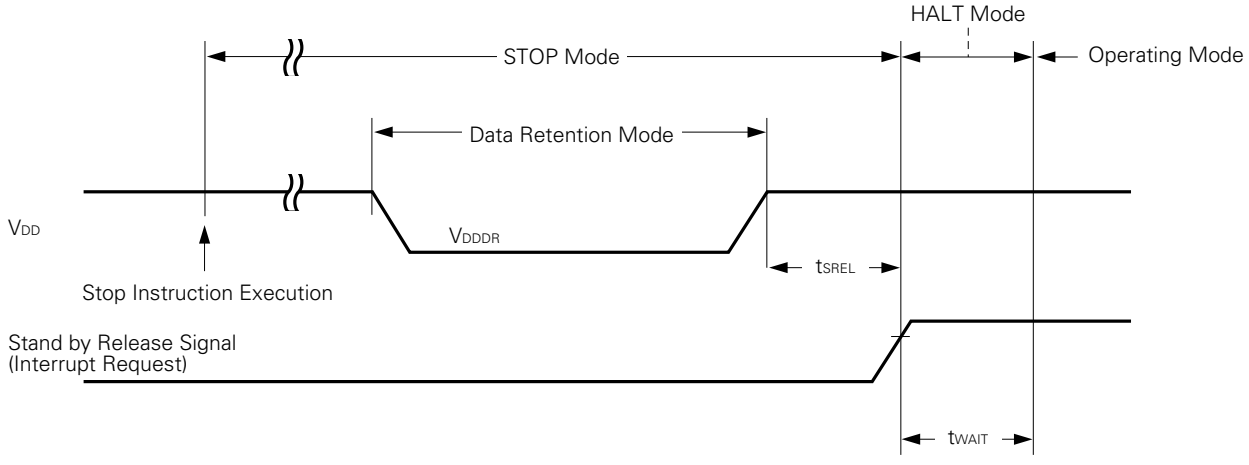
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stop and feedback resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{18}/f_x$		ms
		Release by interrupt		**Note**		ms

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of $2^{13}/fx$ and $2^{15}/fx$ to $2^{18}/fx$ is possible.

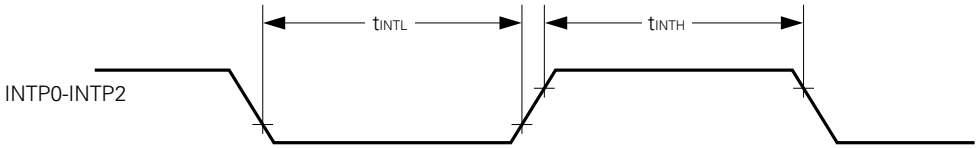
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

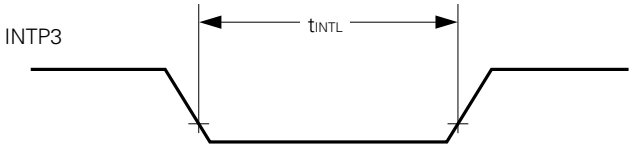


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

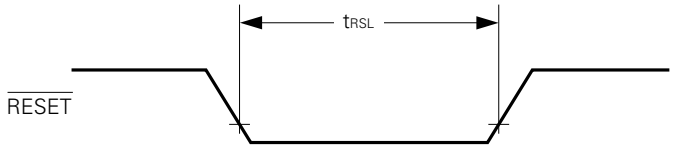


Interrupt Input Timing





$\overline{\text{RESET}}$ Input Timing



DC Programming Characteristics (T_a = 25 ± 5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7 V_{DDP}		V_{DDP}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3 V_{DDP}	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$			10	μA
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = −400 μA	2.4			V
	V_{OH2}	V_{OH2}	I_{OH} = −100 μA	V_{DD} − 0.7			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{LO}	—	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.5	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			
V_{DDP} supply current	I_{DD}	I_{CC}	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}		5	30	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		5	30	mA
			Program memory read mode		1	100	μA

Note Corresponding μPD27C256A symbol.

PROGRAM OPERATION

AC Characteristics (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{CE}\downarrow$)	t_{SAC}	t_{AS}		2			μs
$\overline{OE}\downarrow$ delay time from data	t_{DDOO}	t_{OES}		2			μs
Input data setup time (to $\overline{CE}\downarrow$)	t_{SIDC}	t_{DS}		2			μs
Address hold time (from $\overline{CE}\infty$)	t_{HCA}	t_{AH}		2			μs
Input data hold time (from $\overline{CE}\infty$)	t_{HCID}	t_{DH}		2			μs
Output data hold time (from $\overline{OE}\infty$)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (to $\overline{CE}\downarrow$)	t_{SVPC}	t_{VPS}		1			ms
V_{DDP} setup time (to $\overline{CE}\downarrow$)	t_{SVDC}	t_{VDS}		1			ms
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulsewidth	t_{WL2}	t_{OPW}		2.85		78.75	ms
Data output time from $\overline{OE}\downarrow$	t_{DOOD}	t_{OE}				1	μs

Note Corresponding μPD27C256A symbol.

READ OPERATION

AC Characteristics (T_a = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Data output time from address	t_{DAOD}	t_{ACC}				200	ns
Data output time from $\overline{CE}\downarrow$	t_{DCOD}	t_{CE}				200	ns
Data output time from $\overline{OE}\downarrow$	t_{DOOD}	t_{OE}				75	ns
Data hold time (from $\overline{OE}\infty$)	t_{HCOD}	t_{DF}		0		60	ns
Data hold time (from address)	t_{HAOD}	t_{OH}		0			ns

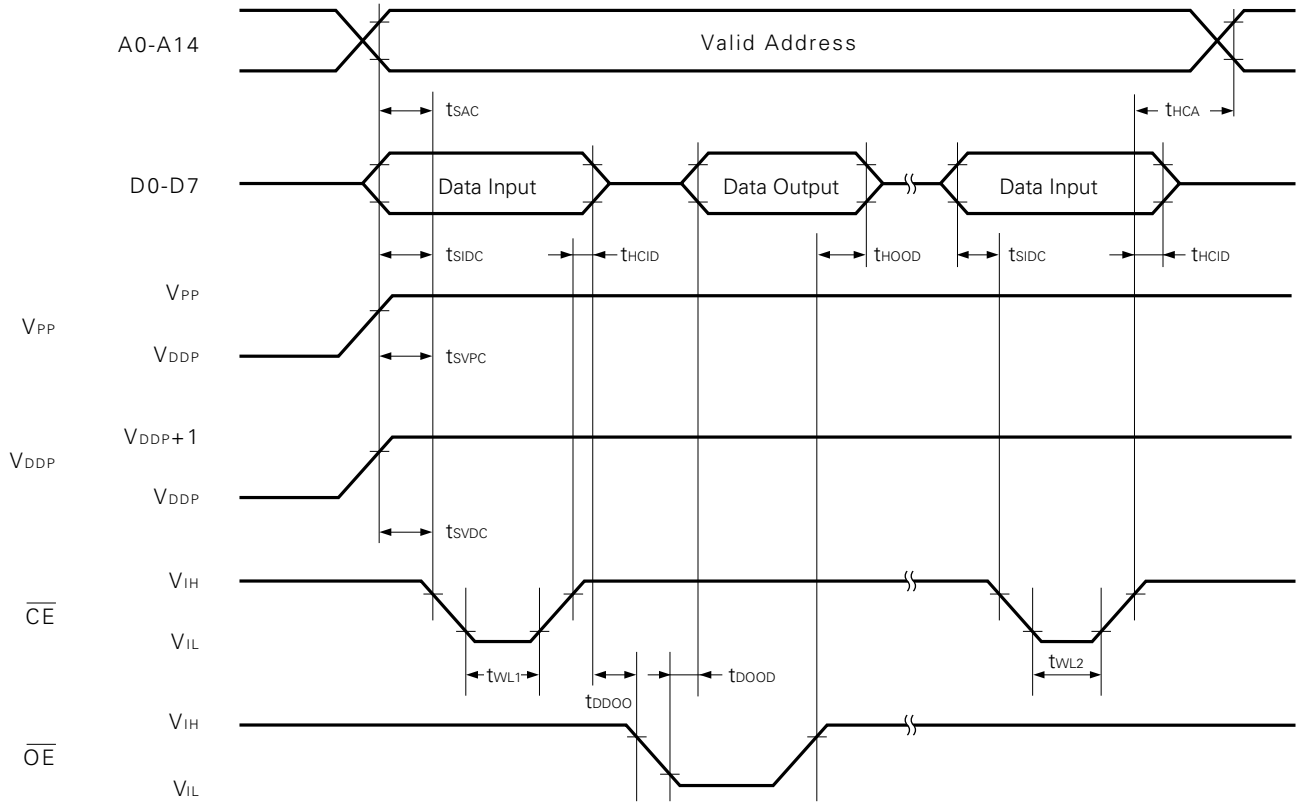
Note Corresponding μPD27C256A symbol.

PROM MODE SETTING

AC Characteristics (T_a = 25 ± 5 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PROM mode setup time	t_{SMA}		10			μs

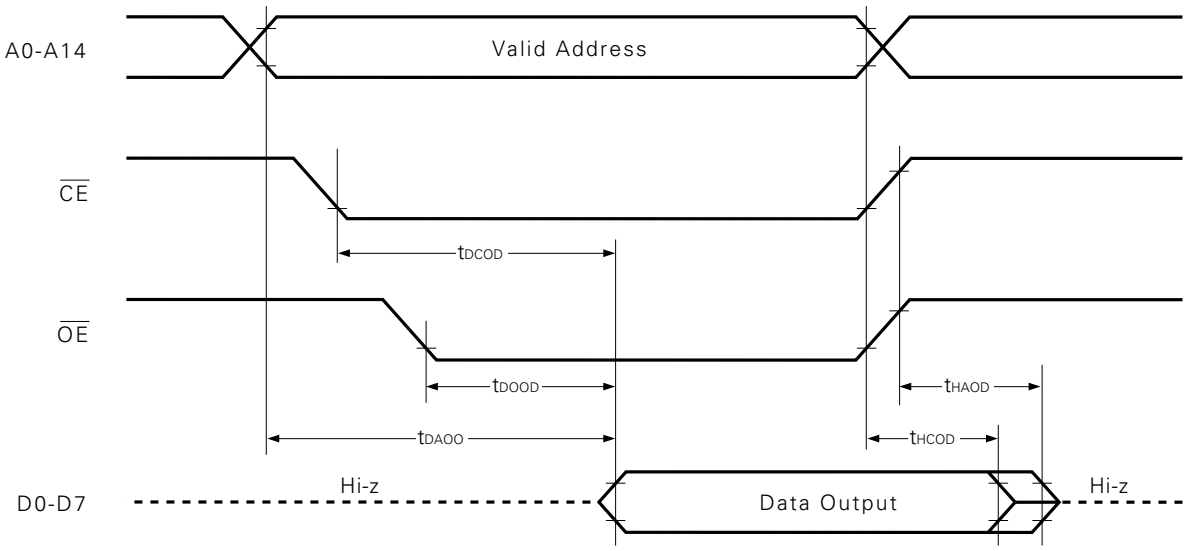
PROM Write Mode Timing



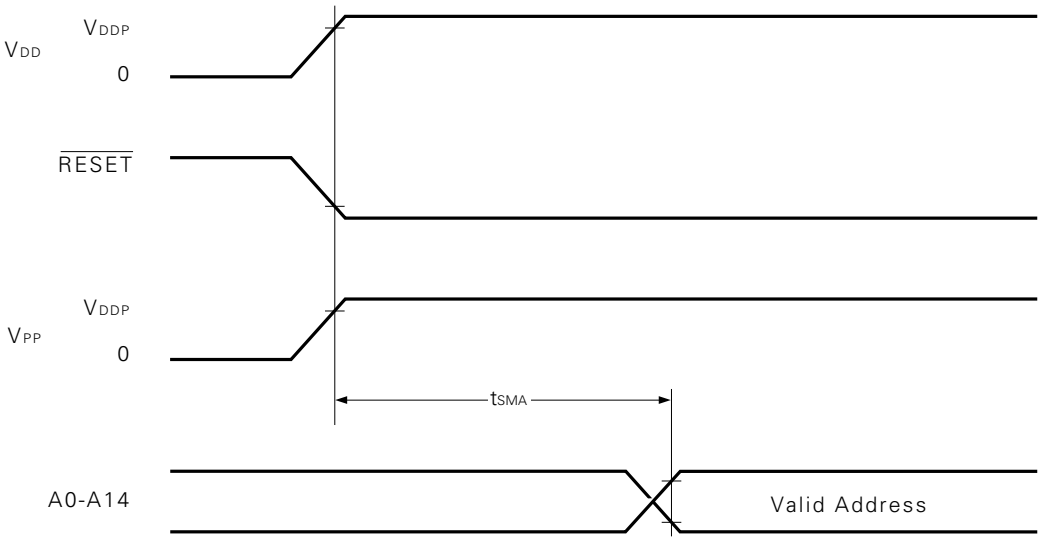
Cautions 1. V_{DDP} must be applied before applying V_{PP}. It should be removed after removing V_{PP}.

2. Do not allow V_{PP} to exceed +13V, including overshoot.

PROM Read Mode Timing

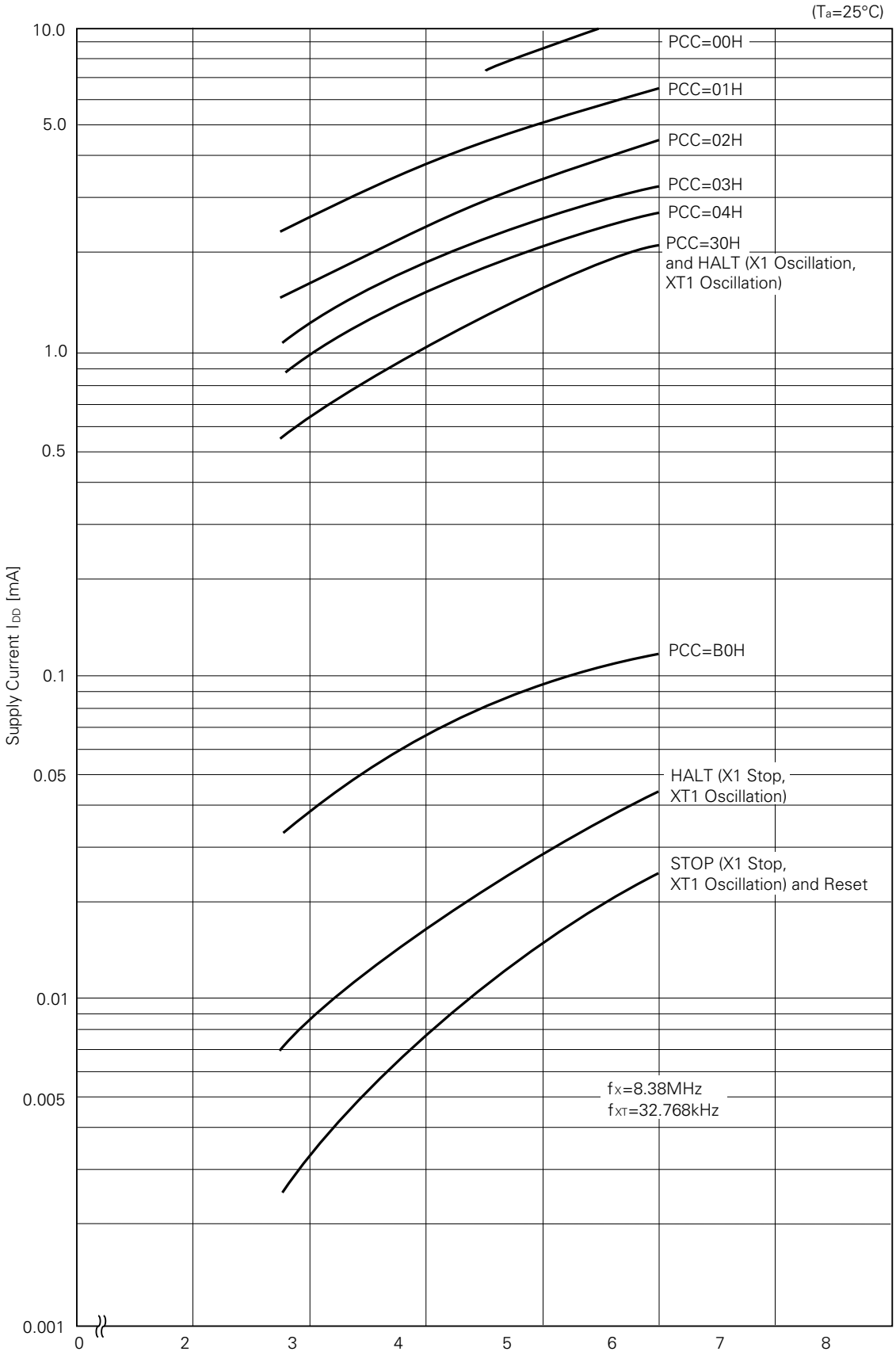


PROM Mode Setting Timing

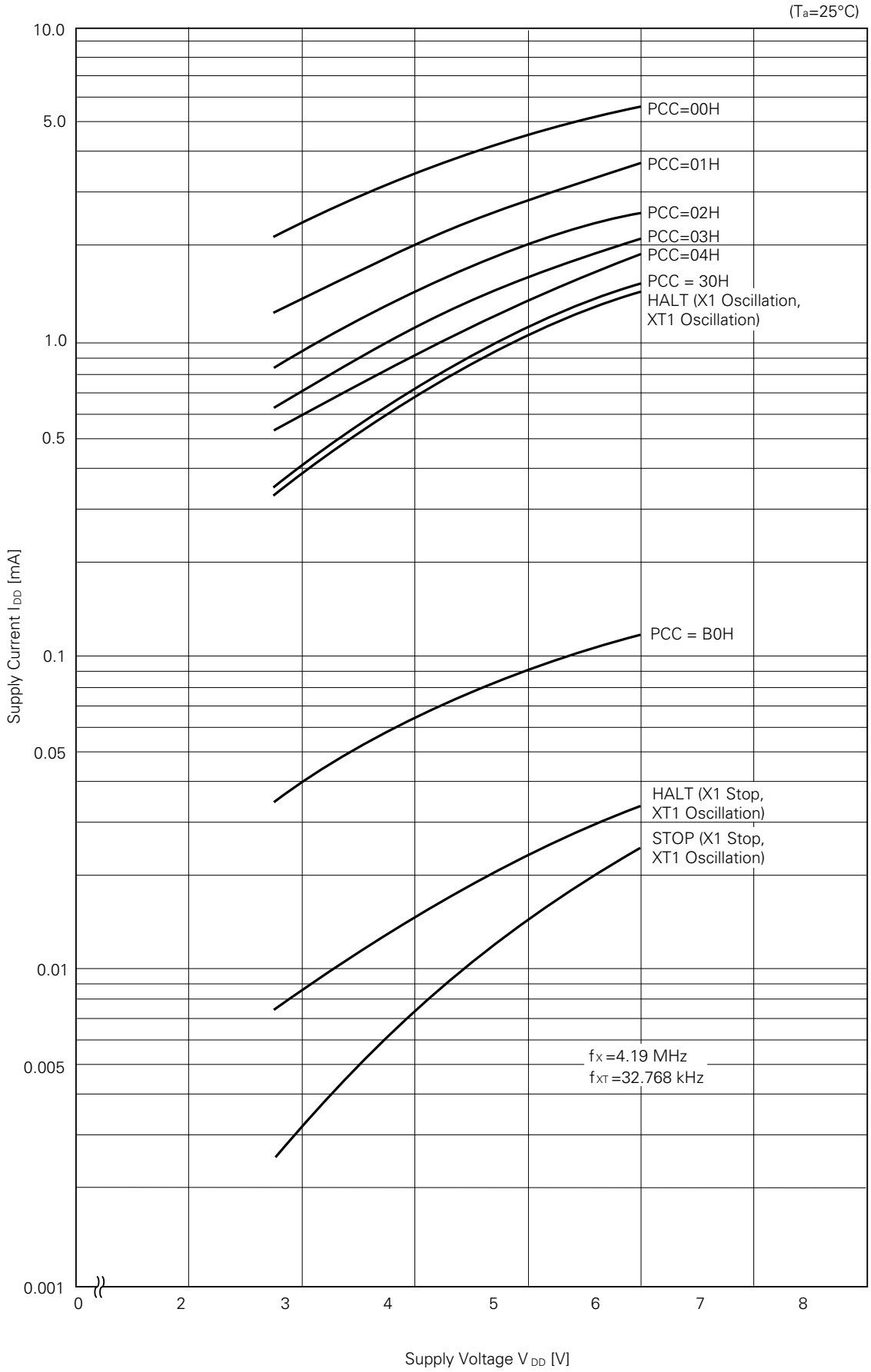


9. CHARACTERISTIC CURVE (REFERENCE VALUES)

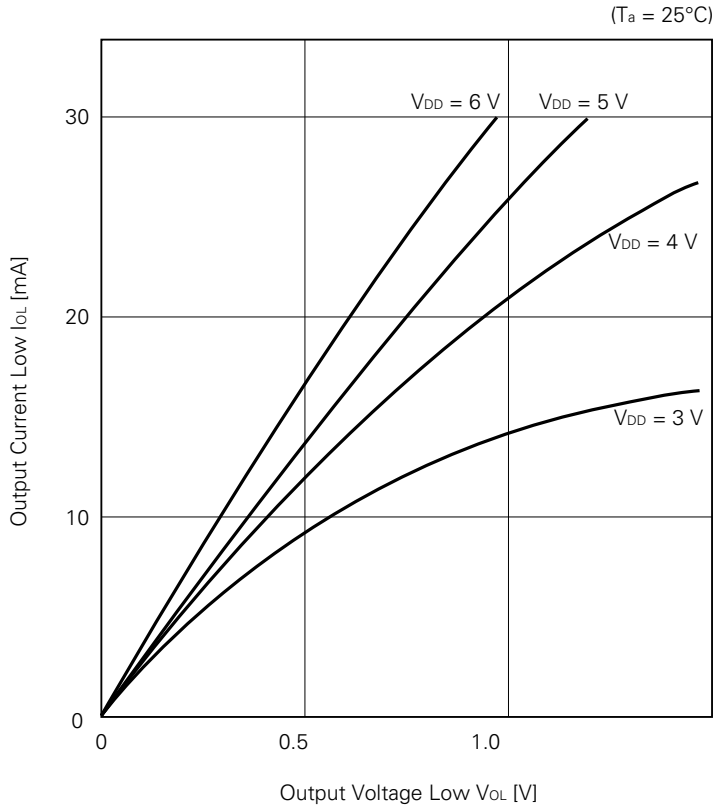
I_{DD} vs V_{DD} (Main System Clock : 8.38 MHz)



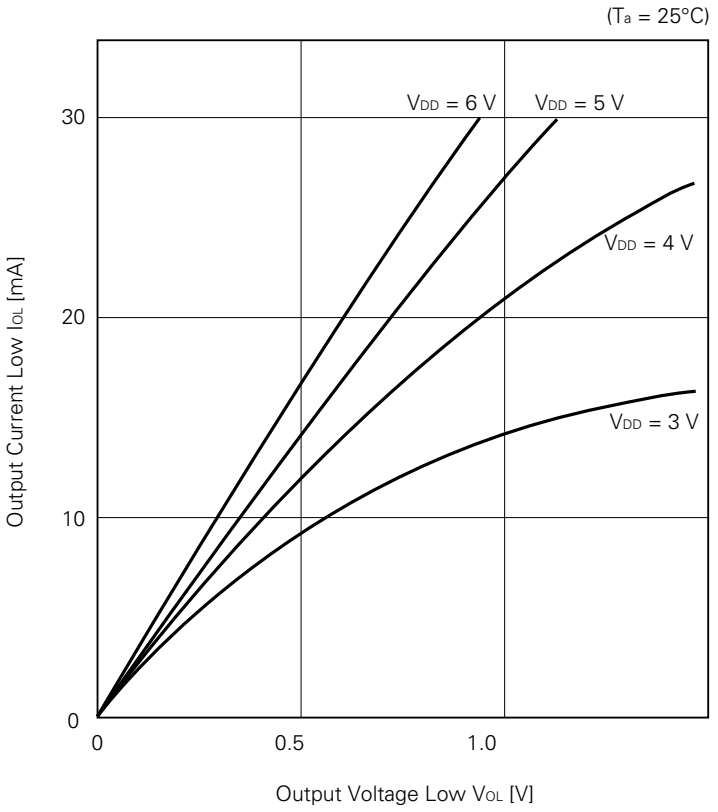
I_{DD} vs V_{DD} (Main System Clock : 4.19 MHz)



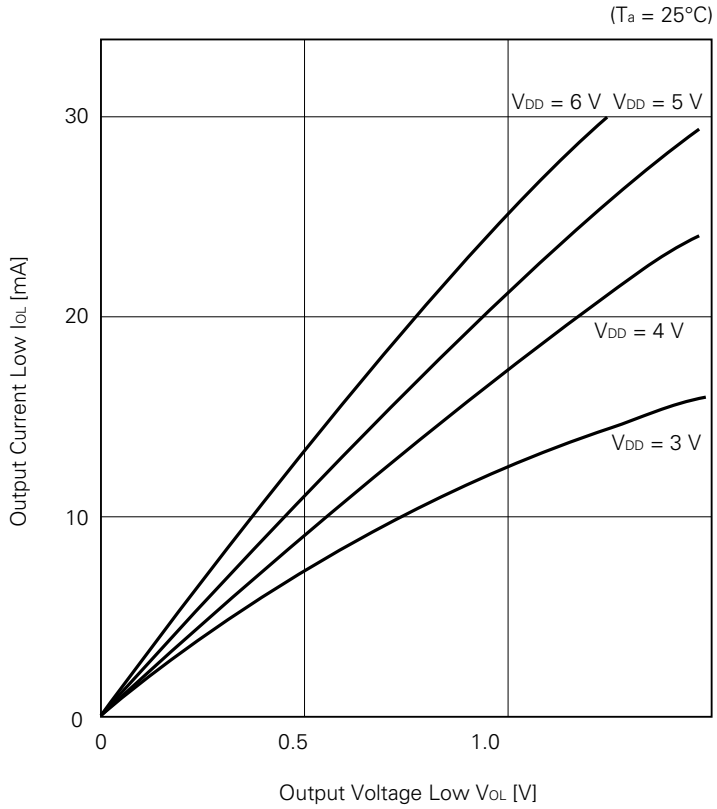
V_{OL} vs I_{OL} (Port 0, 2 to 5, P64 to P67)



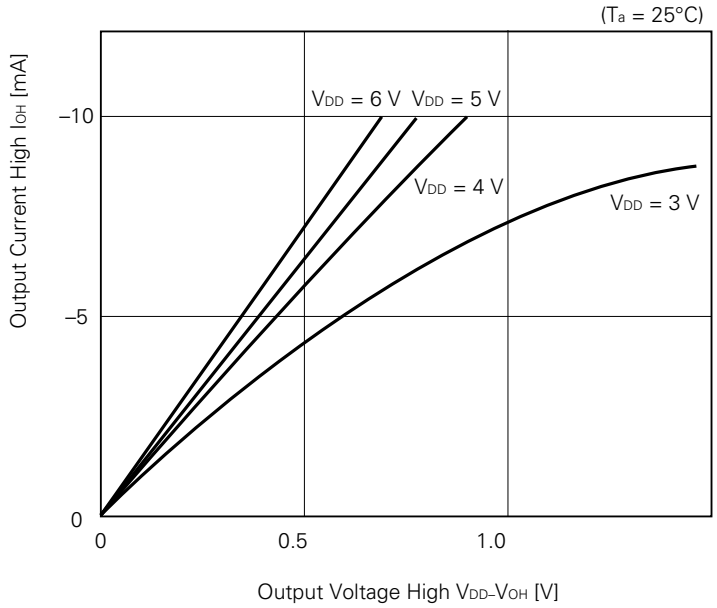
V_{OL} vs I_{OL} (Port 1)



V_{OL} vs I_{OL} (P60 to P63)

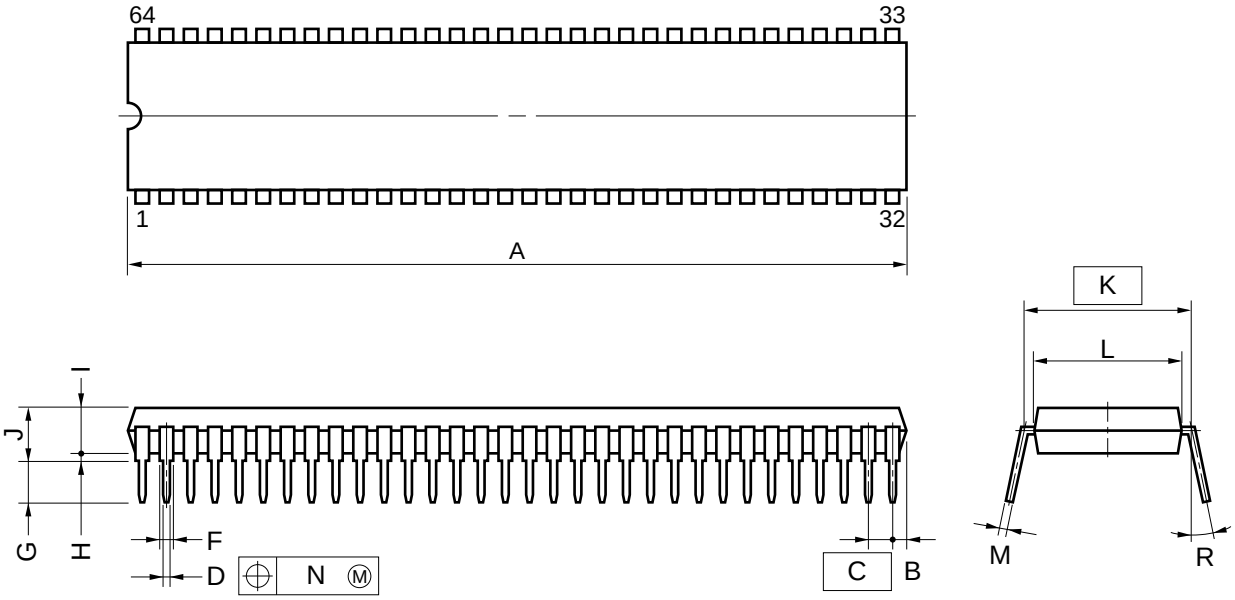


V_{OH} vs I_{OH} (Port 0 to 5, P64 to P67)



10. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



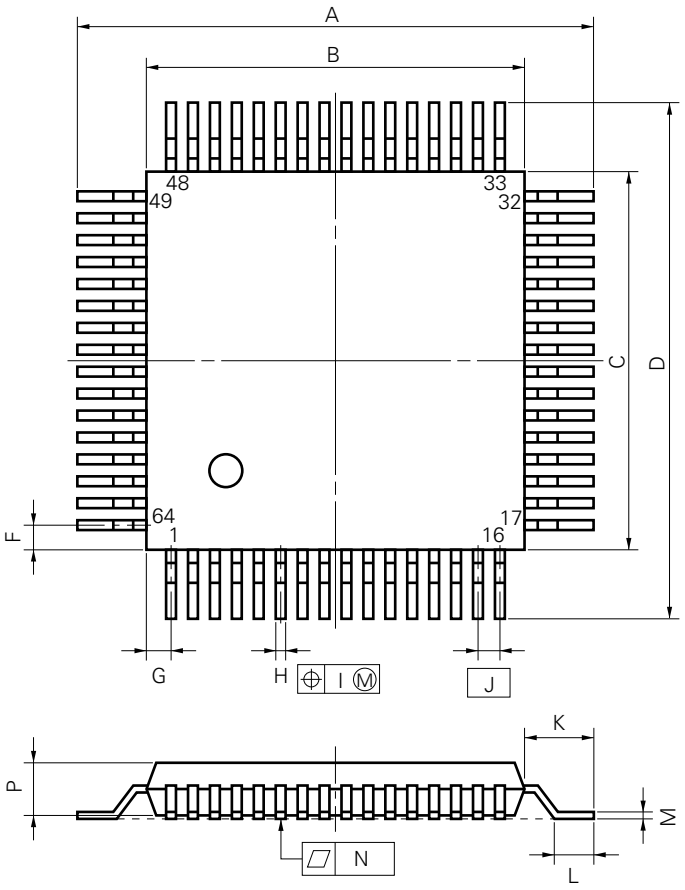
NOTE

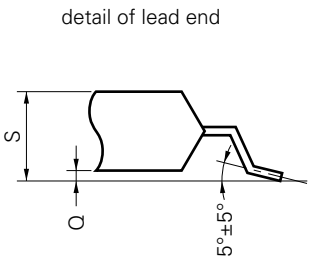
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)





P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

11. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the document **"Semiconductor Device Mounting Technology Manual" (IEI-1207).**

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 11-1. Surface Mounting Type Conditions

μPD78P014YGC-AB8: 64-Pin Plastic QFP (14 x 14 mm)

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Package peak temperature: 230 °C, Time: 30 sec. max. (at 210 °C or above), Number of times: Once, Exposure limit: 2 days[Note] (thereafter 20 hours prebaking required at 125 °C)	IR30-202-1
VPS	Package peak temperature: 215 °C, Time: 40 sec. max. (at 200 °C or above), Number of times: Once, Exposure limit: 2 days[Note] (thereafter 20 hours prebaking required at 125 °C)	VP15-202-1
Partial heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

Note For the storage period after dry-pack decompression storage conditions are max. 25 °C, 65% RH.

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

Table 11-2. Insertion Type Soldering Conditions

μPD78P014YCW: 64-Pin Plastic Shrink DIP (750 mil)

μPD78P014YDW: 64-Pin Ceramic Shrink DIP (with window) (750 mil)

Soldering method	Soldering conditions
Wave soldering (pin only)	Solder bath temperature: 260 °C max., Time: 10 sec. max.
★ Partial heating	Pin temperature: 300 °C max., Time: 3 sec. max (per 1 pin).

Caution Ensure that the application of wave soldering is limited to the pin and no solder touches the main unit directly.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78P014Y.

Language Processor

RA78K/0[Notes 1, 2, 3]	Assembler package for the 78K/0 product line	
CC78K/0[Notes 1, 2, 3]	C compiler package for the 78K/0 product line	
DF78014[Notes 1, 2, 3]	Device file in common with μPD78014 subseries	★
CC78K/0-L[Notes 1, 2, 3]	C compiler library source file for the 78K/0 product line	

PROM Writing Tools

PG-1500	PROM programmer
PA-78P014CW PA-78P014GC	Programmer adapter connected with PG-1500
PG-1500 controller[Notes 1, 2]	PG-1500 control program

Debugging Tools

IE-78000-R	In-circuit emulator for the 78K/0 product line	
IE-78000-R-BK	Break board for the 78K/0 product line	
IE-78014-R-EM	Emulation board for evaluation in common with μPD78002, 78014 subseries	
EP-78240CW-R EP-78240GC-R	Emulation probe in common with μPD78244 subseries	
EV-9200GC-64	Socket mounted on the user system board made for 64-pin plastic QFP	
SD78K/0[Notes 1, 2]	Screen debugger for the IE-78000-R	
SM78K/0[Notes 3, 4, 5, 6]	System simulator for the 78K/0 product line	★
DF78014[Notes 1, 2, 3, 4, 5]	Device file in common with μPD78014 subseries	

Real-Time OS

RX78K/0[Notes 1, 2, 3]	Real-time OS for the 78K/0 product line	
MX78K/0[Notes 1, 2, 3, 6]	OS for the 78K/0 product line	★

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 5]	Fuzzy knowledge data generation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Notes 1, 2]	Fuzzy inference module
FD78K0[Notes 1, 2]	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ (PC DOS™) based
★ **3.** HP9000 series 300™, HP9000 series 700™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series (EWS-UX/V) based
4. PC-9800 series (MS-DOS + Windows™) based
5. IBM PC/AT (PC DOS + Windows) based
6. Under development

Remarks 1. For third party development tools, see the **78K/0 Series Selection Guide (IF-1185)**.
★ **2.** RA78K/0, CC78K/0, SD78K/0, and SM78K/0 are used together with the DF78014.

APPENDIX B. RELATED DOCUMENTS ★

Device Related Documents

Document Name		Document No. (Japanese)	Document No. (English)
μPD78014, 78014Y Series User's Manual		IEU-780	IEU-1343
78K/0 Series Application Note	Basic I	IEA-715	IEA-1288
	Basic II	IEA-740	IEA-1299
	Floating Point Arithmetic Program	IEA-718	IEA-1289

Development Tools Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78014-R-EM		EEU-805	EEU-1400
SD78K/0 Screen Debugger	Introductory	EEU-852	EEU-1414
	Reference	EEU-816	EEU-1413

Related Documents for Embedded Software (User's Manuals)

Document Name	Document No. (Japanese)	Document No. (English)
Fuzzy Knowledge Data Generation Tool	EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System: Translator	EEU-862	EEU-1444

Other Documents

Document Name	Document No. (Japanese)	Document No. (English)
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
NEC Semiconductor Device Quality Grades	IEI-620	IEI-1209
Semiconductor Device Quality Assurance Guide	MEI-603	MEI-1202

Caution The information in these related documents is subject to change without notice. Be sure to use the latest documents for purposes such as design works.

NOTES FOR CMOS DEVICES

①PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

M4 92.6