NEC

MOS INTEGRATED CIRCUIT
μPD75P048

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P048 is a One-Time PROM version of the μPD75048. The μPD75P048 is suitable for small-scale production or experimental production in system development.

Detailed functions are described in the following user's manual. Read this manual when designing your system.

μPD75048 User's Manual: IEU-1278

FEATURES

- The μPD75048 compatible
  - The μPD75P048 for evaluation/pre-production, while the μPD75048 for mass-production
- 8064 × 8 bits of one-time programmable ROM
- 512 × 4 bits of RAM
- 1024 × 4 bits of EEPROM (Data memory area)
- Ports 0 to 3 and 6 to 8 with software-selectable pull-up resistors
- Port 9 with software-selectable pull-down resistors
- 12 N-channel open drain input/output ports (ports 4, 5, and 10)
- Low-voltage operation possible (V_{DD} = 2.7 to 6.0 V)

ORDERING INFORMATION

Part number	Package	Quality grade
μPD75P048CW	64-pin plastic shrink DIP (750 mil)	Standard
μPD75P048GC-AB8	64-pin plastic QFP (□14 mm)	Standard

Caution Pull-up/pull-down resistor mask options are not available.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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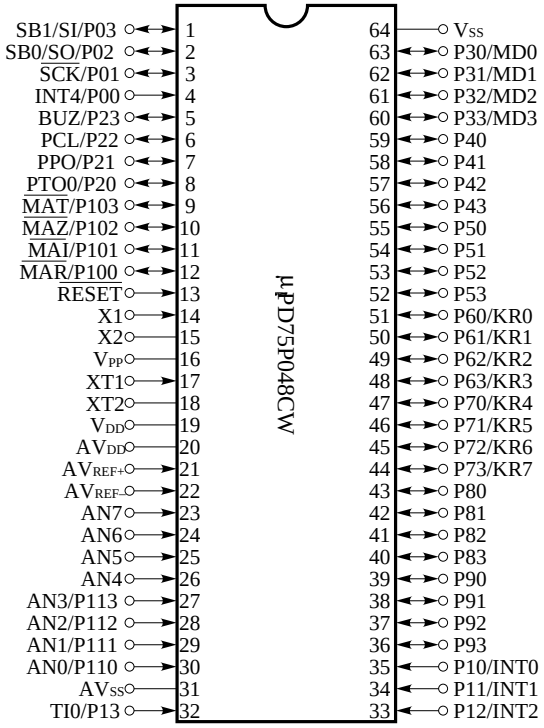
Date Published August 1994 P
Printed in Japan

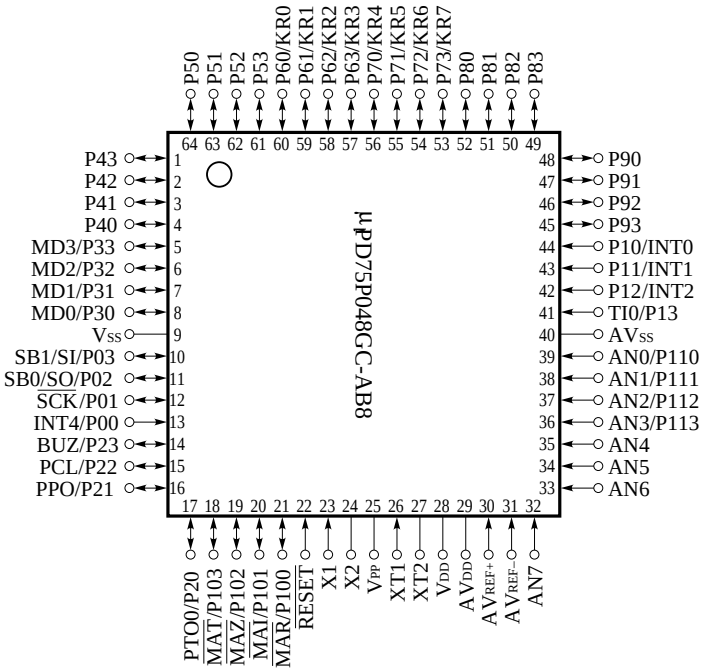
The mark ★ shows major revised points.

PIN CONFIGURATION (Top View)

- **64-pin plastic shrink DIP**



- **64-pin plastic QFP**

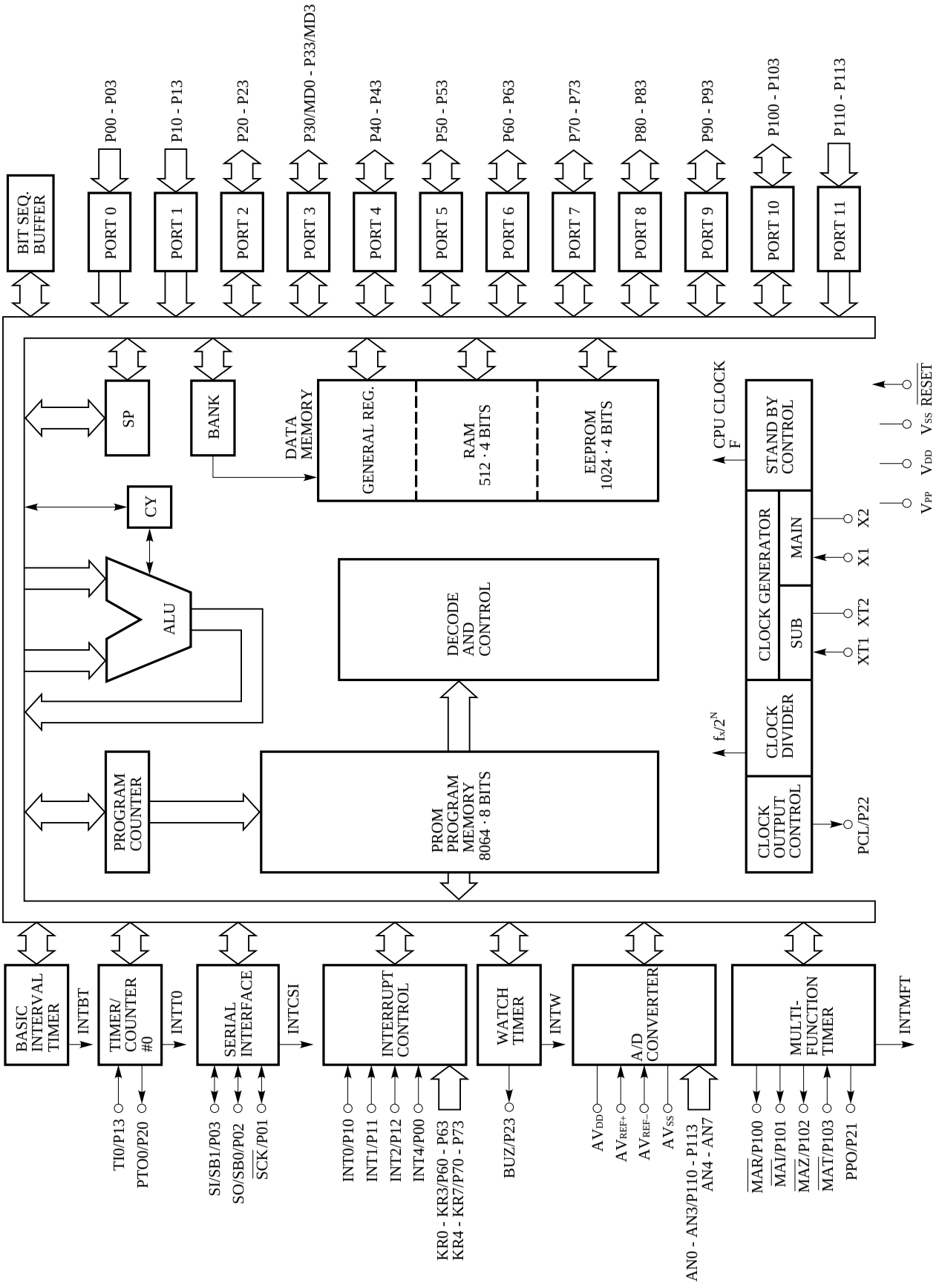


PIN IDENTIFICATION ★

P00-03 : Port0
P10-13 : Port1
P20-23 : Port2
P30-33 : Port3
P40-43 : Port4
P50-53 : Port5
P60-63 : Port6
P70-73 : Port7
P80-83 : Port8
P90-93 : Port9
P100-103 : Port10
P110-113 : Port11
KR0-7 : Key Return
$\overline{SCK}$: Serial Clock
SI : Serial Input
SO : Serial Output
SB0, 1 : Serial Bus 0, 1
$\overline{RESET}$: Reset Input
TI0 : Timer Input 0
PTO0 : Programmable Timer Output 0
BUZ : Buzzer Clock
PCL : Programmable Clock
INT0,1,4 : External Vectored Interrupt 0, 1, 4
INT2 : External Test Input 2
X1, 2 : Main System Clock Oscillation 1, 2
XT1, 2 : Subsystem Clock Oscillation 1, 2
$\overline{MAR}$: Reference Integration Control
$\overline{MAI}$: Integration Control
$\overline{MAZ}$: Autozero Control
$\overline{MAT}$: External Comparate Timing Input
} MFT A/D mode
PPO : Programmable Pulse Output ... MFT timer mode
AN0-7 : Analog Input 0-7
AV_{REF+} : Analog Reference (+)
AV_{REF-} : Analog Reference (-)
AV_{DD} : Analog V_{DD}
AV_{SS} : Analog V_{SS}
V_{DD} : Positive Power Supply
V_{SS} : Ground
V_{PP} : Programming Power Supply
MD0-MD3 : Mode Selection

Remarks MFT: Multi-function timer

BLOCK DIAGRAM



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1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin Name	Input/ Output	Shared Pin	Function	8-Bit I/O	When Reset	I/O Circuit Type Note 1
P00	Input	INT4	4-bit input port (PORT0). For P01 to P03, pull-up resistors can be provided by software in units of 3 bits.	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ-A
P02	I/O	SO/SB0				Ⓕ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ-C
P11		INT1	4-bit input port (PORT1). Pull-up resistors can be provided by software in units of 4 bits.			
P12		INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P21		PPO				
P22		PCL				
P23		BUZ				
P30 Note 2	I/O	MD0	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P31 Note 2		MD1				
P32 Note 2		MD2				
P33 Note 2		MD3				
P40 - P43 Note 2	I/O	–	N-ch open-drain 4-bit I/O port (PORT4). Can withstand 10 V. Data input/output pins for the PROM write and verity (Four low-order bits).	○	High impedance	M-A
P50 - P53 Note 2	I/O	–	N-ch open-drain 4-bit I/O port (PORT5). Can withstand 10 V. Data input/output pins for the PROM write and verify (Four high-order bits).		High impedance	M-A

Note 1. The circle (○) indicates the Schmitt trigger input.

2. Can directly drive LEDs.

1.1 PORT PINS (2/2)

Pin Name	Input/ Output	Shared Pin	Function	8-Bit I/O	When Reset	I/O Circuit Type Note
P60	I/O	KR0	Programmable 4-bit I/O port (PORT 6). Pull-up resistors can be provided by software in units of 4 bits.	○	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	4-bit I/O port (PORT 7). A pull-up resistor can be provided by software in units of 4 bits		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80 - P83	I/O	–	4-bit I/O port (PORT 8). A pull-up resistor can be provided by software in units of 4 bits.	×	Input	E-B
P90 - P93	I/O	–	4-bit I/O port (PORT 9). A pull-up resistor can be provided by software in units of 4 bits.		Input	E-D
P100	I/O	$\overline{MAR}$	N-ch open drain 4-bit I/O port (PORT 10). Can withstand 10 V in open-drain mode.	×	High impedance	M-A ★
P101		$\overline{MAI}$				
P102		$\overline{MAZ}$				
P103		$\overline{MAT}$				
P110	Input	AN0	4-bit input port (PORT 11).		Input	Y
P111		AN1				
P112		AN2				
P113		AN3				

Note The circle (○) indicates the Schmitt trigger input.

1.2 NON-PORT PINS (1/2)

Pin Name	Input/ Output	Shared Pin	Function		When Reset	I/O Circuit Type Note
TI0	Input	P13	Input for receiving external event pulse signal for timer/event counter		Input	Ⓑ-C
PTO0	I/O	P20	Timer/event counter output		Input	E-B
PCL	I/O	P22	Clock output		Input	E-B
BUZ	I/O	P23	Output for arbitrary frequency output (for buzzer output or system clock trimming)		Input	E-B
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	Ⓕ-A
SO/SB0	I/O	P02	Serial data output Serial bus I/O		Input	Ⓕ-B
SI/SB1	I/O	P03	Serial data input Serial bus I/O		Input	Ⓜ-C
INT4	Input	P00	Edge detection vectored interrupt input (either rising edge or falling edge detection)		Input	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input (detection edge selectable)		Input	Ⓑ-C
INT1		P11				
INT2	Input	P12	Edge detection testable input (rising edge detection)		Input	Ⓑ-C
KR0 - KR3	I/O	P60 - P63	Parallel falling edge detection testable input		Input	Ⓕ-A
KR4 - KR7	I/O	P70 - P73	Parallel falling edge detection testable input		Input	Ⓕ-A
$\overline{MAR}$	I/O	P100	In MFT integrating A/D converter mode	Reverse integration signal output	High impedance	M-A
$\overline{MAI}$	I/O	P101		Integration signal output	High impedance	M-A
$\overline{MAZ}$	I/O	P102		Auto-zero signal output	High impedance	M-A
$\overline{MAT}$	I/O	P103		Comparator input	High impedance	M-A
PPO	I/O	P21	In MFT timer mode	Timer pulse output	Input	E-B
AN0 - AN3	Input	P110 - P113	For A/D converter only	8-bit analog input	–	Y-A
AN4 - AN7		–				Y-A
AV_{REF+}	Input	–		Reference voltage input (AV_{DD} side)	–	Z-A
AV_{REF-}	Input	–		Reference voltage input (AV_{SS} side)	–	Z-A
AV_{DD}	–	–		Positive power supply	–	–
AV_{SS}	–	–		GND potential	–	–

Note The circle (◯) indicates the Schmitt trigger input.

Remark MFT: Multi-Function Timer

1.2 NON-PORT PINS (2/2)

Pin Name	Input/ Output	Shared Pin	Function	When Reset	I/O Circuit Type Note 1
X1, X2	Input	–	Crystal/ceramic resonator connection for main system clock generation. When external clock signal is used, it is applied to X1, and its reverse phase signal is applied to X2.	–	–
XT1, XT2	Input	–	Crystal connection for subsystem clock generation. When external clock signal is used, it is applied to XT1, and its reverse phase signal is applied to XT2. XT1 can be used as a 1-bit input (test).	–	–
$\overline{\text{RESET}}$	Input	–	System reset input	–	Ⓑ
MD0 - MD3	I/O	P30 - P33	Operation mode selection pins during the PROM write/verify cycles.	Input	E-B
V_{PP} Note 2	–	–	Normally connected to V_{DD} directly; +12.5 V is applied as the programming voltage during the PROM write/verify cycles.	–	–
V_{DD}	–	–	Positive power supply	–	–
V_{SS}	–	–	GND potential	–	–

Note 1. The circle (◯) indicates the Schmitt trigger input.

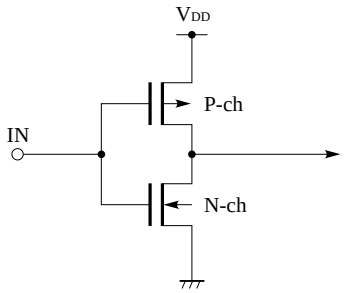
2. The V_{PP} should be connected to V_{DD} directly in normal operation mode. If V_{PP} and V_{DD} pins are not connected, the μPD75P048 does not operate correctly.

1.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuit of each μPD75P048 pin is shown below in a simplified manner.

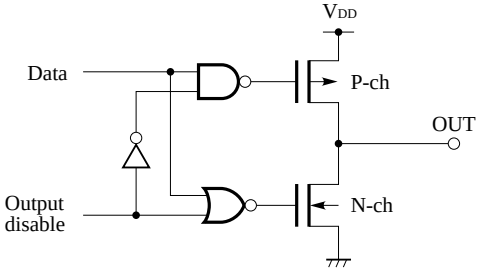
(1/3)

Type A (For Type E-B)



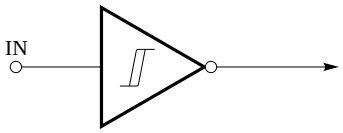
CMOS input buffer

Type D (For Type E-B, F-A)



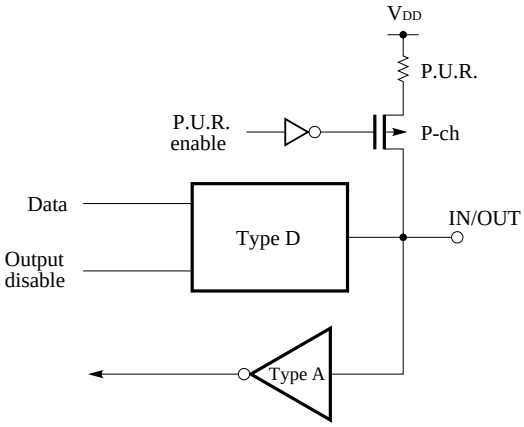
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type B



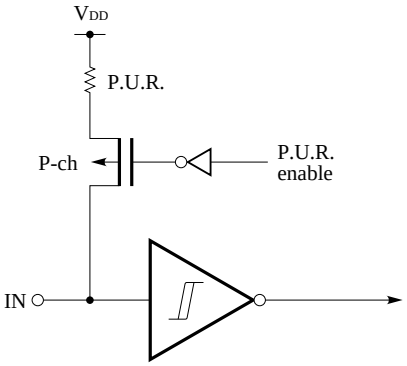
Schmitt trigger input with hysteresis

Type E-B



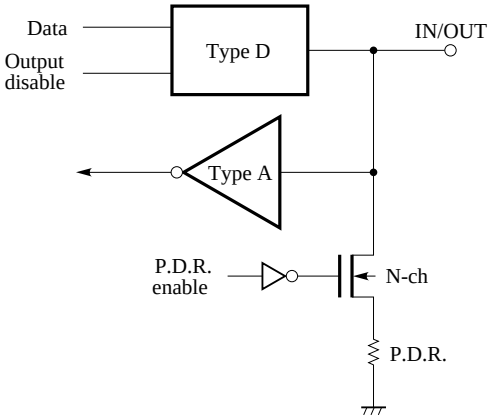
P.U.R.: Pull-Up Resistor

Type B-C



P.U.R.: Pull-Up Resistor

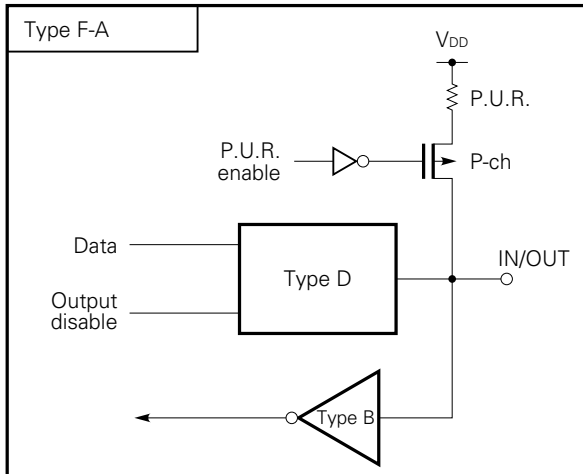
Type E-D



P.D.R.: Pull-Down Resistor

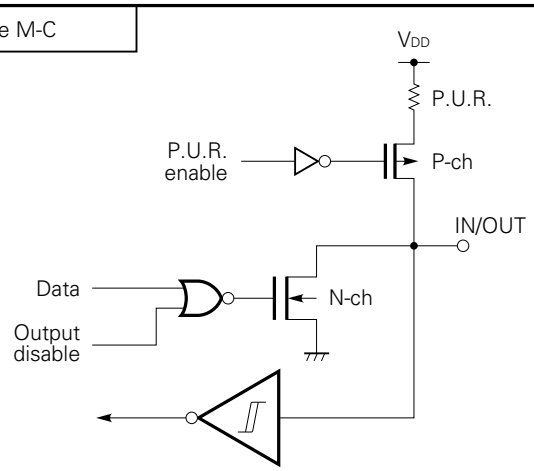
(2/3)

Type F-A



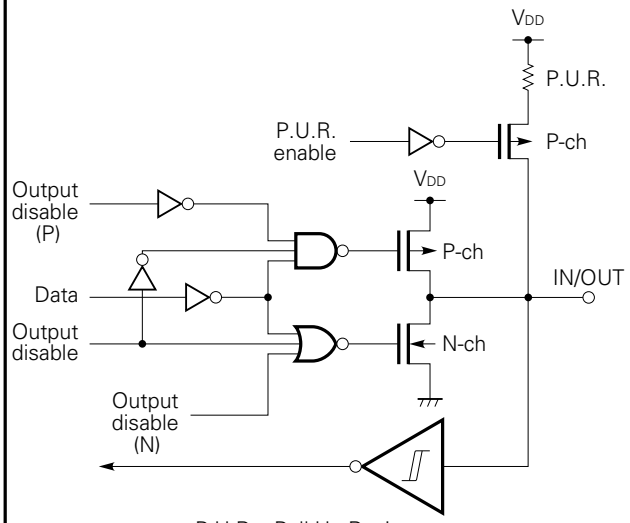
P.U.R.: Pull-Up Resistor

Type M-C



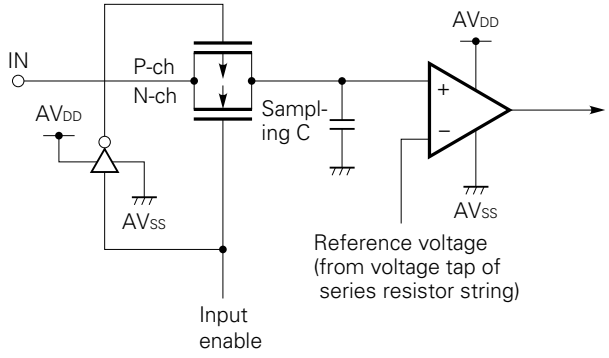
P.U.R.: Pull-Up Resistor

Type F-B

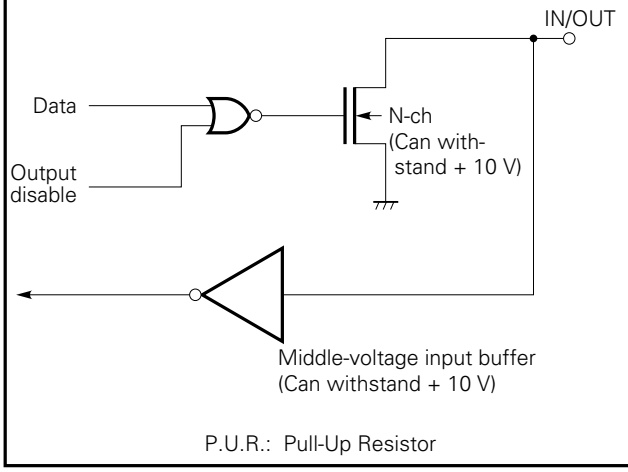


P.U.R.: Pull-Up Resistor

Type Y

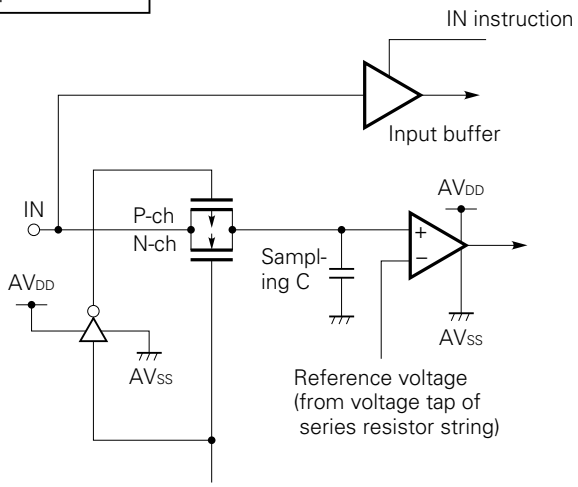


Type M-A



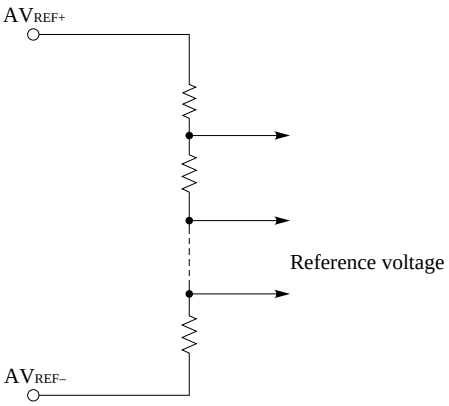
P.U.R.: Pull-Up Resistor

Type Y-A



(3/3)

Type Z-A



2. DIFFERENCES BETWEEN THE μPD75P048 AND THE μPD75048

The μPD75P048 is a One-Time PROM version of the μPD75048. The μPD75P048 has the same CPU and internal hardwares. Table 2-1 shows the differences between the μPD75P048 and the μPD75048. Bear in mind the differences between these two products when debugging or developing on an experimental basis your application system by using the one-time PROM model, and then mass-producing the application system by using the mask ROM model.

Details for the CPU functions and internal hardwares are available in **μPD75048 User's Manual (IEU-1278)**.

Table 2-1 Differences between the μPD75P048 and the μPD75048

Items		μPD75P048	μPD75048
Program Memory		One-time PROM	Mask ROM
		• 0000H to 1F7FH • 8064 × 8 bits	
Pull-up Resistors	Ports 0 to 3 and 6 to 8	Software-selectable	
	Ports 4, 5 and 10	N/A	Mask-option
Pull-Down Resistors	Port 9	Software-selectable	
XT1 Feedback Resistor		On-chip	Mask-option
Pin Connection	60 - 63 (SDIP) 5 - 8 (QFP)	P33/MD3 - P30/MD0	P33 - P30
	16 (SDIP) 25 (QFP)	V_{PP}	IC
Electrical Specification		Current dissipation differs. For details, refer to Data Sheet of each model.	
Other		Circuit scale and mask layout differ. Consequently, noise immunity and noise radiation differ.	

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Note The noise immunity and noise radiation of the PROM and mask ROM models differ. To replace the PROM mode, which has been used for experimental production of your application system with the mask ROM model for mass production of the application system, be sure to perform thorough evaluation by using the CS model (not ES model) of the mask ROM model. ★

3. PROM (PROGRAM MEMORY) WRITE AND VERIFY

The μPD75P048 contains 8064 bytes of PROM. The following table shows the pin functions during the write and verify cycles. Note that it is not necessary to enter an address, because the address is updated by pulsing the X1 clock pins.

Pin Name	Function
V_{PP}	Normally 2.7 to 6 V; 12.5 V is applied during write/verify
X1, X2	After a write/verify write, the X1 and X2 clock pins are pulsed. The inverted signal of the X1 should be input to the X2. Note that these pins are also pulsed during a read.
MD0 - MD3 (P30 - P33)	Operation mode selection pins.
P40 - P43 (lower 4 bits) P50 - P53 (higher 4 bits)	8-bit data input/output pins for write and verify
V_{DD}	Supply voltage. Normally 2.7 to 6 V; 6 V is applied during write/verify

Caution The μPD75P048CW/GC do not have a UV erase window, thus the PROM contents cannot be erased with ultra-violet ray.

3.1 PROM WRITE AND VERIFY OPERATION MODE

When 6 V and 12.5 V are applied to the V_{DD} and V_{PP} pins, respectively, the PROM is placed in the write/verify mode. The operation is selected by the MD0 to MD3 pins, as shown in the table.

The other pins should be returned to V_{SS} potential via pull-down resistors.

Operation Mode Specification						Operation Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Clear program memory address to 0
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit

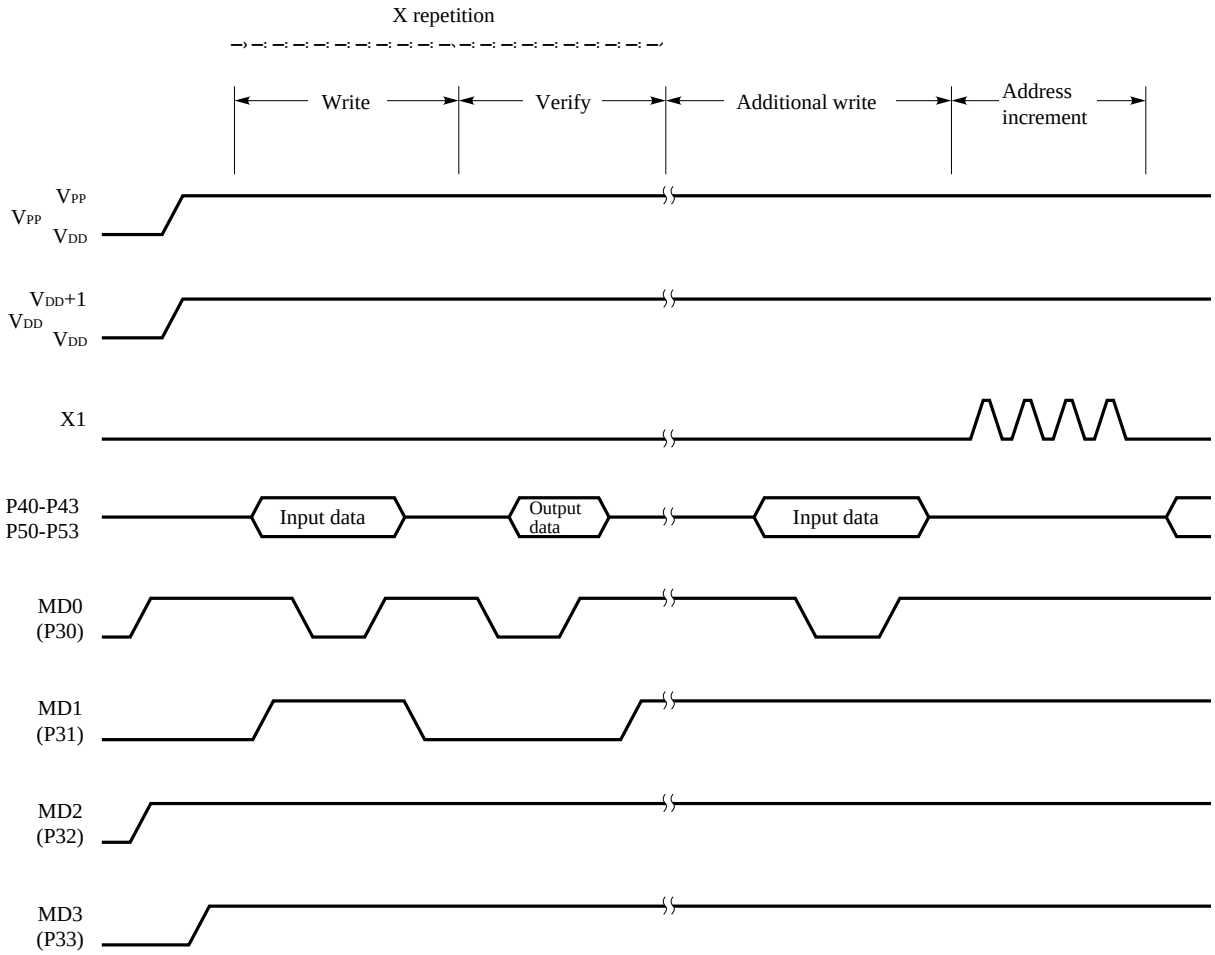
×: Don't care.

3.2 PROM WRITE PROCEDURE

PROMs can be written at high speed using the following procedure: (see the following figure)

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 volts to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Select the zero clear program memory address mode.
(5) Supply 6 volts to the V_{DD} and 12.5 volts to the V_{PP} pins.
(6) Select the program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Select the program inhibit mode.
(9) Select the verify mode. If the data is correct, proceed to step (10). If not, repeat steps (7), (8) and (9).
(10) Perform one additional write (duration of 1 ms × number of writes at (7) to (9)).
(11) Select the program inhibit mode.
(12) Apply four pulses to the X1 pin to increment the program memory address by one.
(13) Repeat steps (7) to (12) until the end address is reached.
(14) Select the zero clear program memory address mode.
(15) Return the V_{DD} and V_{PP} pins back to + 5 volts.
(16) Turn off the power.

The following figure shows steps (2) to (12).

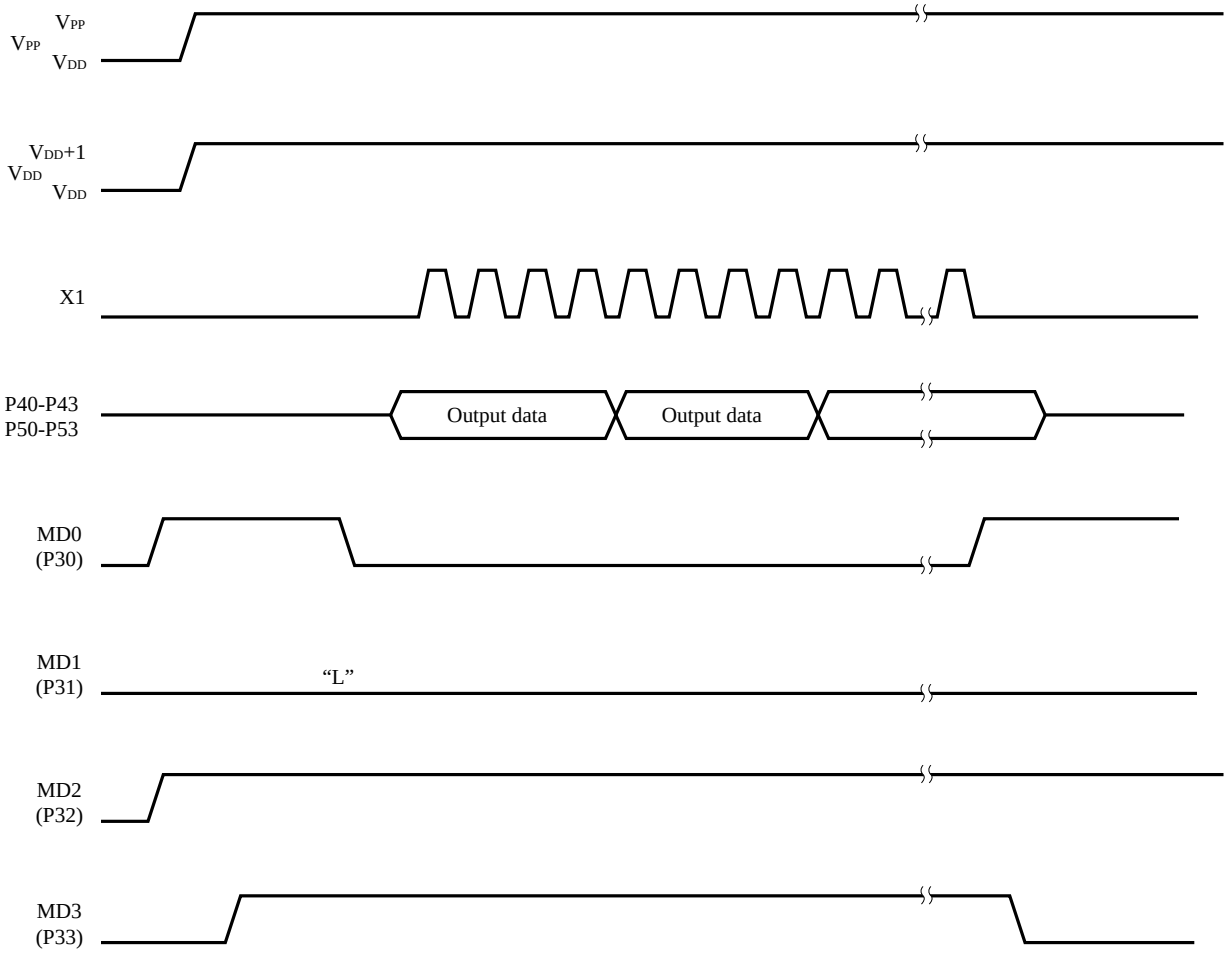


3.3 PROM READ PROCEDURE

The PROM contents can be read in the verify mode by using the following procedure: (see the following figure)

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 volts to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Select the clear program memory address mode.
(5) Supply 6 volts to the V_{DD} and 12.5 volts to the V_{PP} pins.
(6) Select the program inhibit mode.
(7) Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
(8) Select the program inhibit mode.
(9) Select the clear program memory address mode.
(10) Return the V_{DD} and V_{PP} pins back to + 5 volts.
(11) Turn off the power.

The following figure shows steps (2) to (9).



4. SCREENING OF ONE-TIME PROM MODEL ★

Because of their structure, the one-time PROM models (μPD75P48CW and μPD75P48GC-AB8) cannot be fully tested by NEC before shipment. It is therefore recommended that you implement screening to verify the PROM after necessary data have been written to it, and after the PROM has been stored at high temperature under the following conditions:

Storage Temperature	Storage Time
125 °C	24 hours

★ 5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 4, 5, 10		-0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4, 5, 10	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +11	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 pin		-10	mA
		All pins		-30	mA
Low-Level Output Current	I_{OL} **Note**	Ports 0, 3, 4, 5 1 pin	Peak	30	mA
			rms	15	mA
		Other than ports 0, 3, 4, 5 1 pin	Peak	20	mA
			rms	5	mA
		Total of ports 0, 3 - 9, 11	Peak	170	mA
			rms	120	mA
		Total of ports 0, 2, 10	Peak	30	mA
			rms	20	mA
Operating Temperature	T_{opt}			-10 to +70	°C
Storage Temperature	T_{stg}			-65 to +150	°C

Note rms = Peak value x $\sqrt{\text{Duty}}$

Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.

EEPROM RATINGS (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

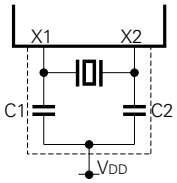
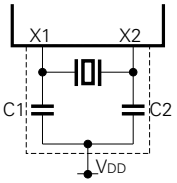
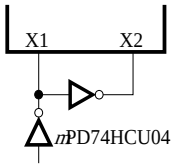
Parameter	Symbol	Conditions	Ratings	Unit
Write Times	—		100,000	times
Data Retention Time	—		10	years

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_I	f = 1 MHz		15	pF	
Output Capacitance	C_O	Pins other than those measured are at 0 V			15	pF
Input/Output	C_{IO}			15	pF	

MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic		Oscillation frequency(f_X) Note 1	V_{DD} = oscillation voltage range	2.0		5.0 Note 3	MHz
		Oscillation stabilization time Note 2	After V_{DD} come to MIN. value of oscillation voltage range			4	ms
Crystal		Oscillation frequency (f_X) Note 1		2.0	4.19	5.0 Note 3	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_X) Note 1		2.0		5.0 Note 3	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		250	ns

Note 1. Only to express the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2. Time required for oscillation to stabilize after V_{DD} has reached the minimum volue of the oscillation voltage range or the STOP mode has been released.

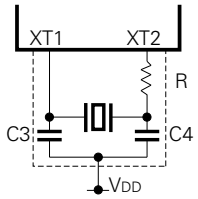
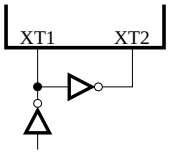
3. When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs.

Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the ground pattern through which a high curent flows.**
- **Do not extract signals from the oscillation circuit.**

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External Clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

Note 1. Indicates only the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2. Time required for oscillation to stabilize after V_{DD} has reached the minimum value of the oscillation voltage range.

Caution When using the oscillation circuit of the subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

DC CHARACTERISTICS (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Ports 2,3,8,9,11		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0,1,6,7, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4,5,10	w/pull-up resistor	0.7V_{DD}		V_{DD}	V
			Open-drain	0.7V_{DD}		10	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD}-0.5		V_{DD}	V
Low-level Input Voltage	V_{IL1}	Ports 2-5, 8-11		0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1, XT2		0		0.4	V
High-Level Output Voltage	V_{OH}	V_{DD} = 4.5 to 6.0V, I_{OH} = -1 mA		V_{DD}-1.0			V
		I_{OH} = -100 μA		V_{DD}-0.5			V
Low-Level Output Voltage	V_{OL}	Ports 3,4,5	V_{DD} = 4.5 to 6.0V, I_{OL} = 15mA		0.4	2.0	V
		V_{DD} = 4.5 to 6.0V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0, 1	Open-drain pull-up resistor ≥ 1 kΩ			0.2V_{DD}	V
High-Level Input Leakage Current	I_{LIH1}	V_I = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1,X2,XT1			20	μA
	I_{LIH3}	V_I = 9V	Ports 4,5,10 (open-drain)			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_I = 0V	Other than below			-3	μA
	I_{LIL2}		X1,X2,XT1			-20	μA
High-Level Output Leakage Current	I_{LOH1}	V_O = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_O = 9V	Ports 4,5,10 (open-drain)			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_O = 0V				-3	μA
Internal Pull-Up Resistor	R_{U1}	Ports 0,1,2,3,6,7,8 (except P00) V_I = 0V	V_{DD} = 5.0V±10%	15	40	80	kΩ
			V_{DD} = 3.0V±10%	30		300	kΩ
	R_{U2}	Ports 4,5,10 V_O = V_{DD}-2.0 V	V_{DD} = 5.0V±10%	15	40	70	kΩ
			V_{DD} = 3.0V±10%	10		60	kΩ
Internal Pull-Down Resistor	R_D	Port 9 V_{IN} = V_{DD}	V_{DD} = 5.0V±10%	15	40	70	kΩ
			V_{DD} = 3.0V±10%	10		60	kΩ

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply Current [Note 1]	I_{DD1}	4.19MHz crystal oscillator C1 = C2 = 22pF	V_{DD} = 5V±10% [Note 2]			5.5	17	mA
			V_{DD} = 3V±10% [Note 3]			1.7	5.1	mA
	I_{DD2}		HALT mode	V_{DD} = 5V±10%		900	2700	μA
				V_{DD} = 3V±10%		450	1400	μA
	I_{DD3}	32.768kHz [Note 4] crystal oscillator	Operation mode	V_{DD} = 3V±10%		100	300	μA
	I_{DD4}		HALT mode	V_{DD} = 3V±10%		35	110	μA
	I_{DD5}	XT1 = 0V STOP mode	V_{DD} = 5V±10%			0.5	20	μA
			V_{DD} = 3V±10%			0.3	10	μA
				T_a = 25°C			5	μA
	I_{DD6}	32.768kHz oscillator STOP mode	V_{DD} = 3V±10% [Note 5]			6	20	μA

Note 1. Current flowing through internal pull-up resistor. Current flowing when EEPROM is accessed is not included.

2. When μPD75048 operates in high-speed mode with processor clock control register (PCC) set to 0011.

3. When μPD75048 operates in low-speed mode with PCC set to 0000.

4. When the system clock control register (SCC) is set to 1001, the oscillation of the main system clock is stopped, and the subsystem clock is used.

5. When STOP instruction is executed with SCC set to 0000.

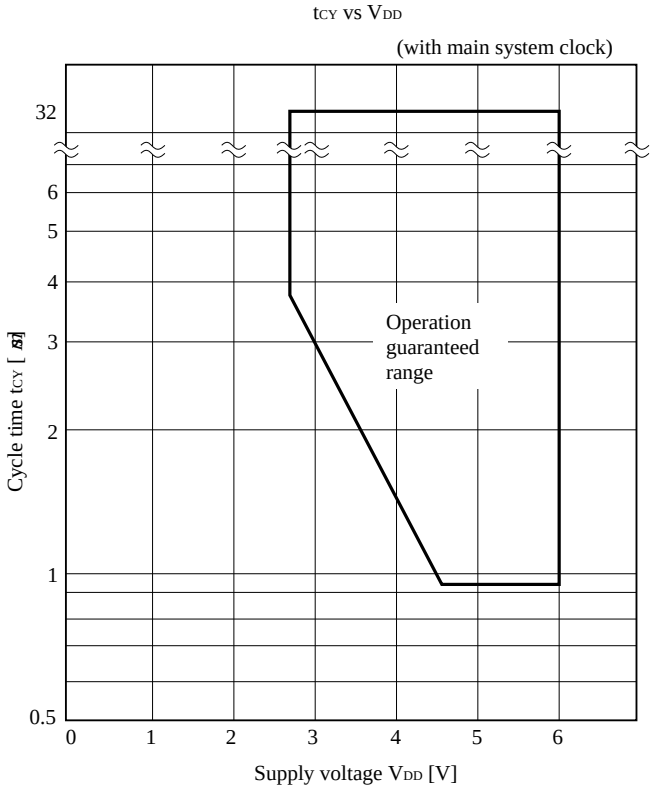
Note Supply current when EEPROM is accessed is shown in EEPROM Characteristics.

AC CHARACTERISTICS (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time (Minimum Instruction Execution Time = 1 Machine Cycle) Note 1	t_{CY}	w/main system clock	V_{DD} = 4.5 to 6.0V	0.95		32	μs
				3.8		32	μs
		w/subsystem clock		114	122	125	μs
TI0 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 Input High-, Low-Level Widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt Input High-, Low-Level Widths	t_{INTH}, t_{INTL}	INT0		Note 2			μs
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{RESET}$ Low-Level Width	t_{RSL}			10			μs

Note 1. The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC).
The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

2. $2t_{CY}$ or 128/fx depending on the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

Two-Line and Three-Line Serial I/O Modes ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
	t_{KH1}			t_{KCY1}/2-150			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK1}			150			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO1}	R_L = 1kΩ, C_L = 100pF Note	V_{DD} = 4.5 to 6.0V			250	ns
						1000	ns

TWO-LINE AND THREE-LINE SERIAL I/O MODES ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY2}	V_{DD} = 4.5 to 6.0V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL2}	V_{DD} = 4.5 to 6.0V		400			ns
	t_{KH2}			1600			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK2}			100			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO2}	R_L = 1kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0V			300	ns
						1000	ns

Note R_L and C_L are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{SCK}$: internal clock output (master))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO3}	R_L = 1kΩ, C_L = 100pF	Note V_{DD} = 4.5 to 6.0V	0		250	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0,1 ↓→ $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY3}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY3}			ns

SBI MODE ($\overline{SCK}$: external clock input (slave))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ Ligh-, Low-Level Widths	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO4}	R_L = 1kΩ, C_L = 100pF	Note V_{DD} = 4.5 to 6.0V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0,1 ↓→ $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY4}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L are load resistance and load capacitance of the SB0 and SB1 output lines.

A/D CONVERTER (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0V, AV_{SS} = V_{SS} = 0V)

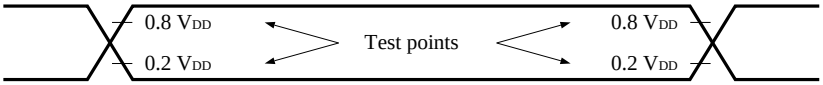
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Absolute Accuracy Note 1		2.5V ≤ AV_{REF} ≤ V_{DD}			±1.5	LSB
Conversion Time Note 2	t_{CONV}				168/f_X	μs
Sampling Time Note 3	t_{SAMP}				44/f_X	μs
Analog Input Voltage	V_{IAN}		AV_{REF-}		AV_{REF+}	V
Analog Supply Voltage	AV_{DD}		2.5		V_{DD}	V
Reference Input Voltage	AV_{REF+}	2.5V ≤ (AV_{ref+}) – (AV_{ref-})	2.5		AV_{DD}	V
Reference Input Voltage	AV_{REF-}	2.5V ≤ (AV_{ref+}) – (AV_{ref-})	0		1.0	V
Analog Input Impedance	R_{AN}			1000		MΩ
AV_{REF} Current	AI_{REF}			0.25	2.0	mA

Note 1. Absolute accuracy excluding quantization error ($\pm\frac{1}{2}$LSB)

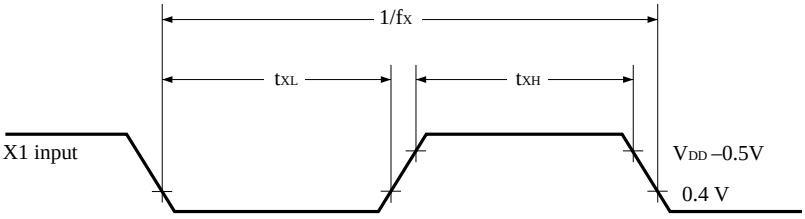
2. Time since execution of conversion start instruction until end of conversion (EOC = 1) (40.1 μs: f_X = 4.19 MHz)

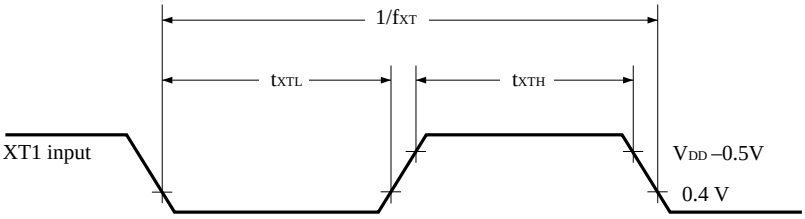
3. Time since execution of conversion start instruction until end of sampling (10.5 μs: f_X = 4.19 MHz)

AC TIMING TEST POINT (excluding X1 and XT1 inputs)

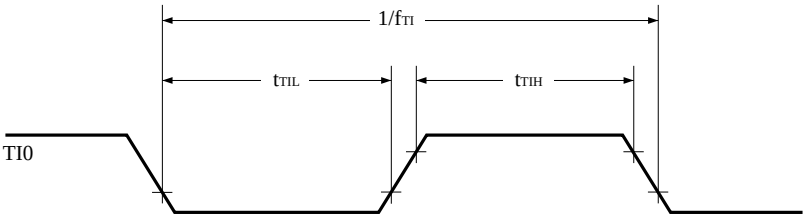


CLOCK TIMING



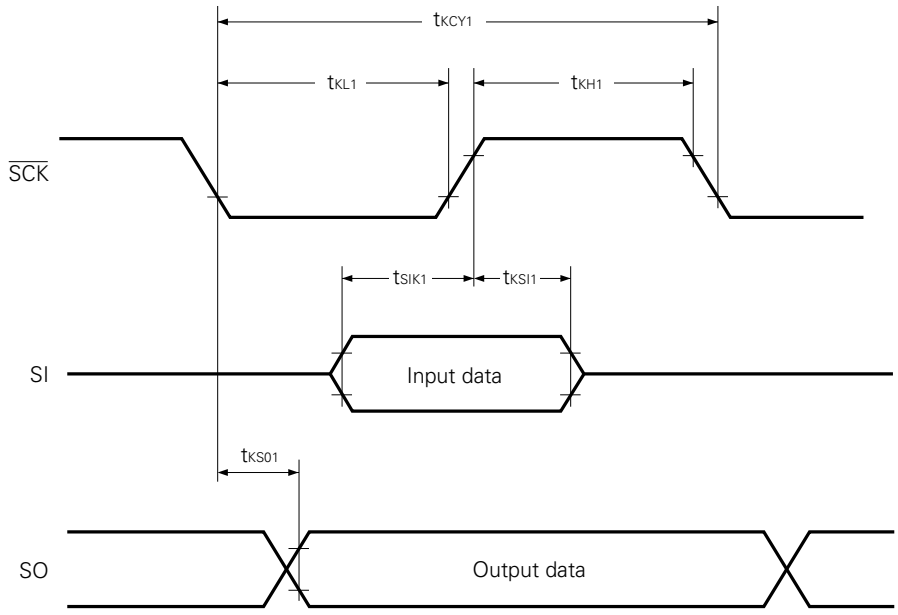


TI0 TIMING

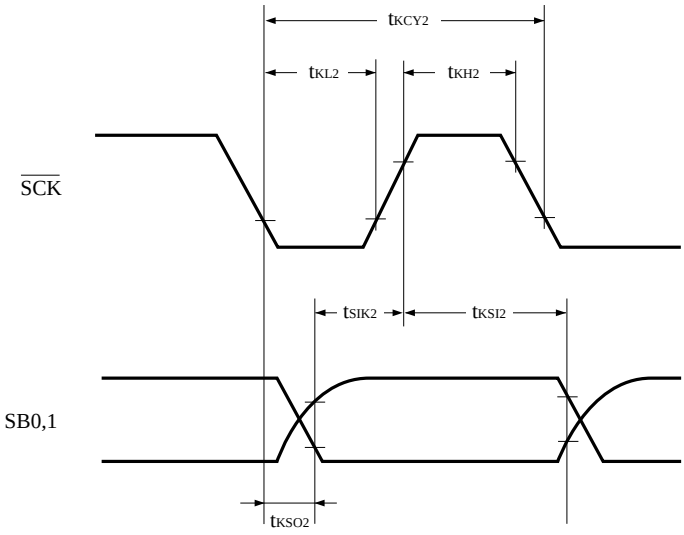


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

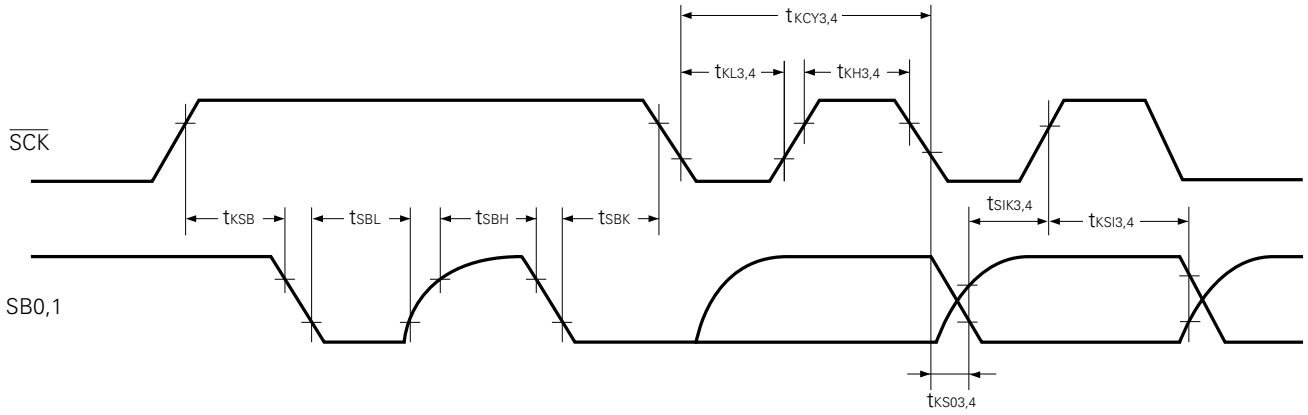


TWO-LINE SERIAL I/O MODE:

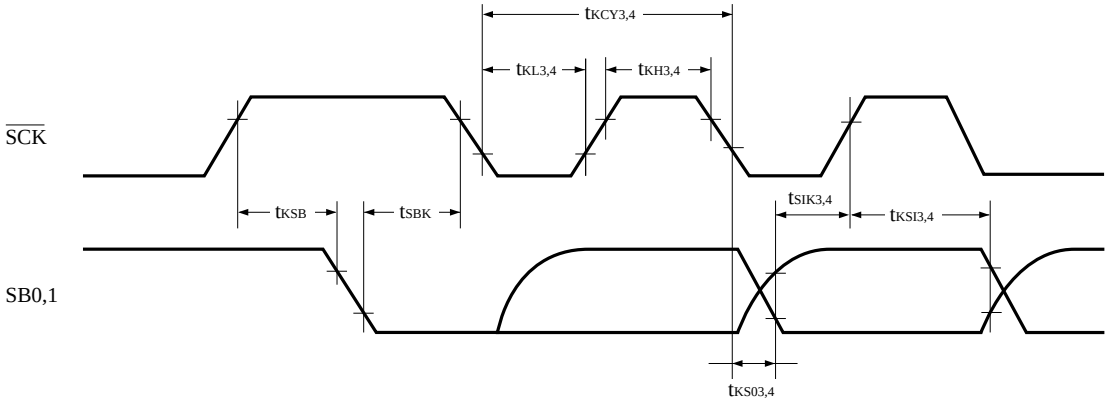


SERIAL TRANSFER TIMING

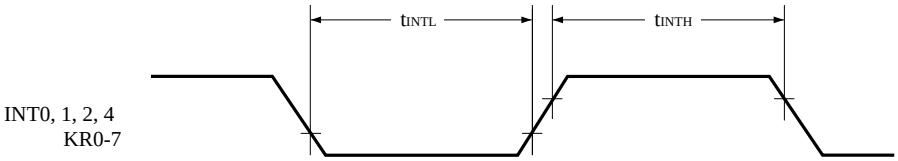
BUS RELEASE SIGNAL TRANSFER:



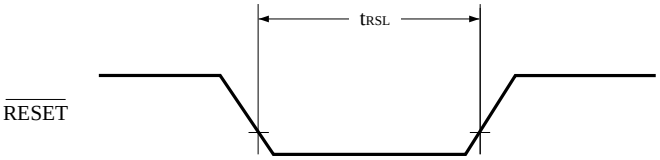
COMMAND SIGNAL TRANSFER:



INTERRUPT INPUT TIMING



RESET INPUT TIMING



EEPROM CHARACTERISTICS

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current for EEPROM access Note 1	I_{DD7}	4.19MHz crystal oscillator C1 = C = 22pF	V_{DD} = 5V+10% Note 2		6.5	20	mA
			V_{DD} = 3V+10% Note 3		2	6	mA

Note 1. Current flowing through the internal pull-up resistor is not included.

2. When the processor clock control register (PCC) is set to 0011 and the high-speed mode is used.

3. When PCC is set to 0000 and the low-speed mode is used.

EEPROM WRITE TIME

Select the write time of the EEPROM in accordance with the oscillation frequency of the main system clock as follows:

Oscillation Frequency of Main System Clock (f_X)	Setting of EEPROM Control Register		Write time
	EWTC1	EWTC0	
f_X = 2.0 to 5.0 MHz	0	0	2^{12} x 18/f_X (17.6 ms)
f_X = 2.0 to 4.2 MHz	0	1	2^{11} x 18/f_X (8.8 ms)
f_X = 2.0 MHz	1	0	2^{10} x 18/f_X

Remarks ( ): f_X = 4.19 MHz

LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = –10 to +70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current Note 1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time Note 2	t_{WAIT}	Released by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Released by interrupt request		Note 3		ms

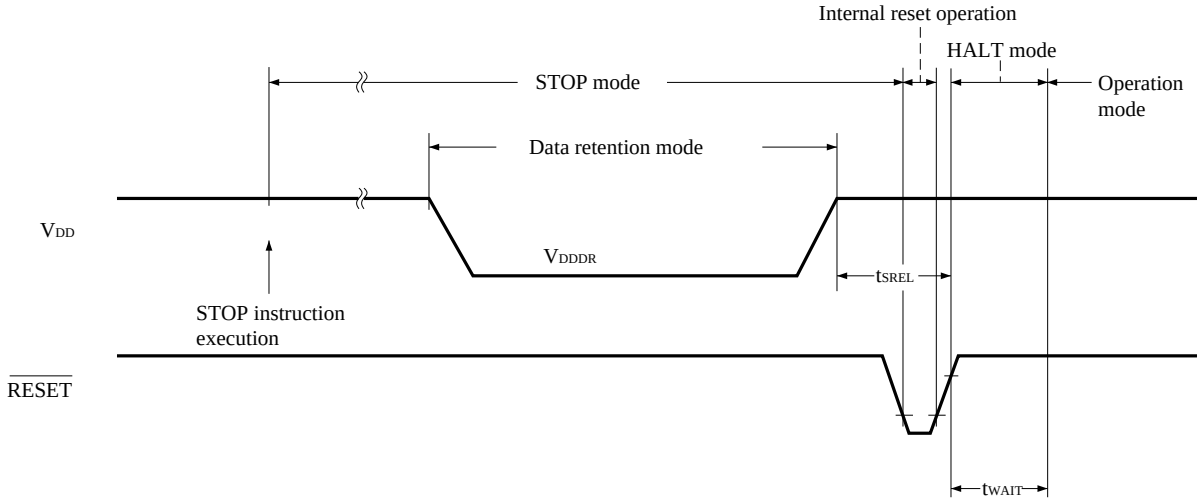
Note 1. Does not include current flowing through internal pull-up resistor

2. The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

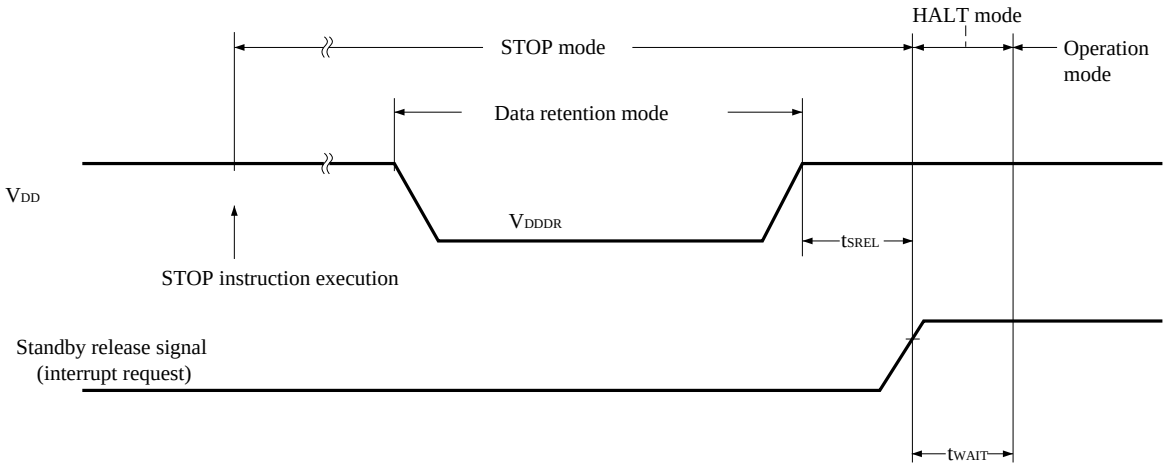
3. Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): f_X = 4.19 MHz
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

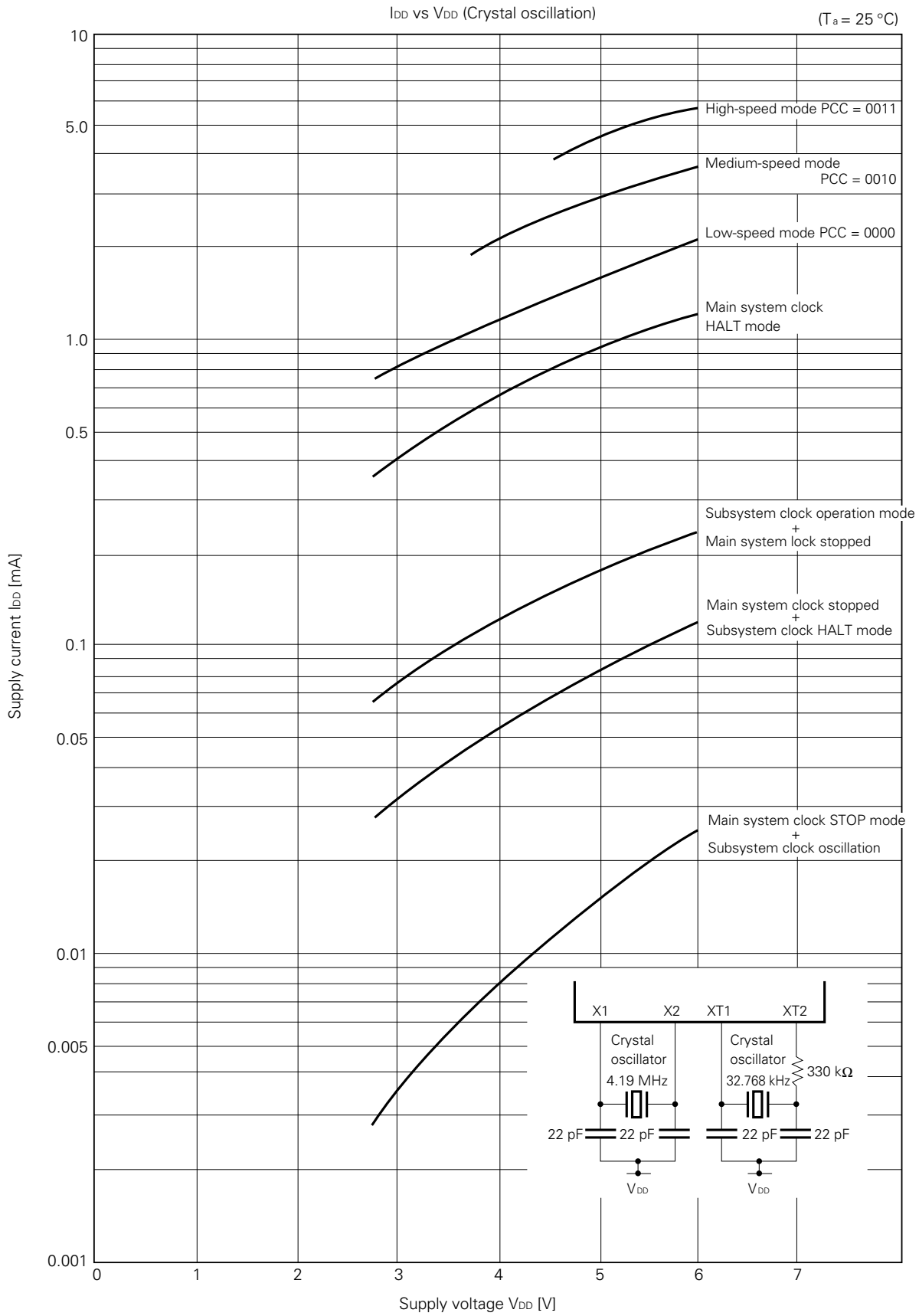
DATA RETENTION TIMING (releasing STOP mode by $\overline{\text{RESET}}$)



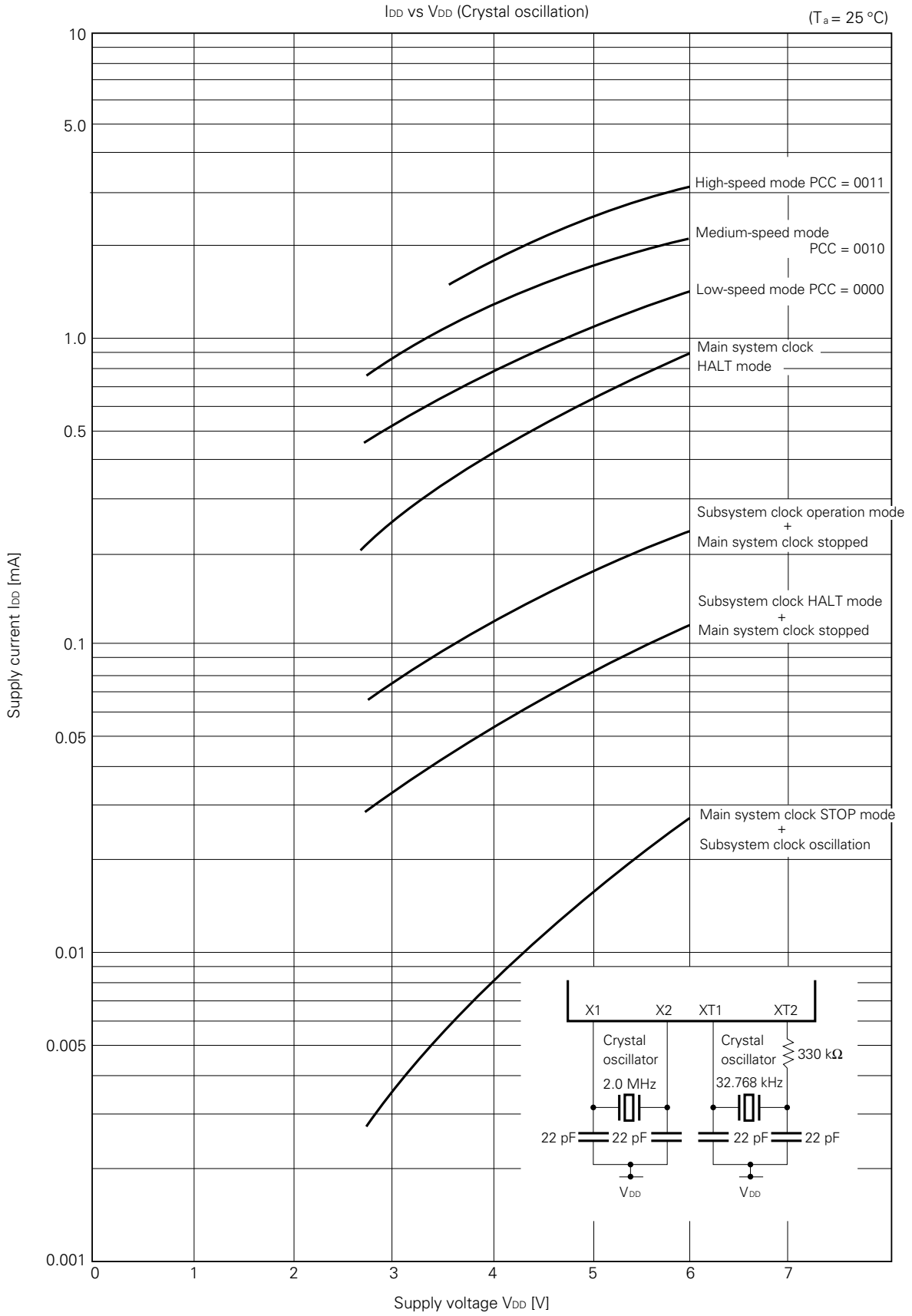
DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



★ 6. PERFORMANCE CURVE (REFERENCE VALUE)



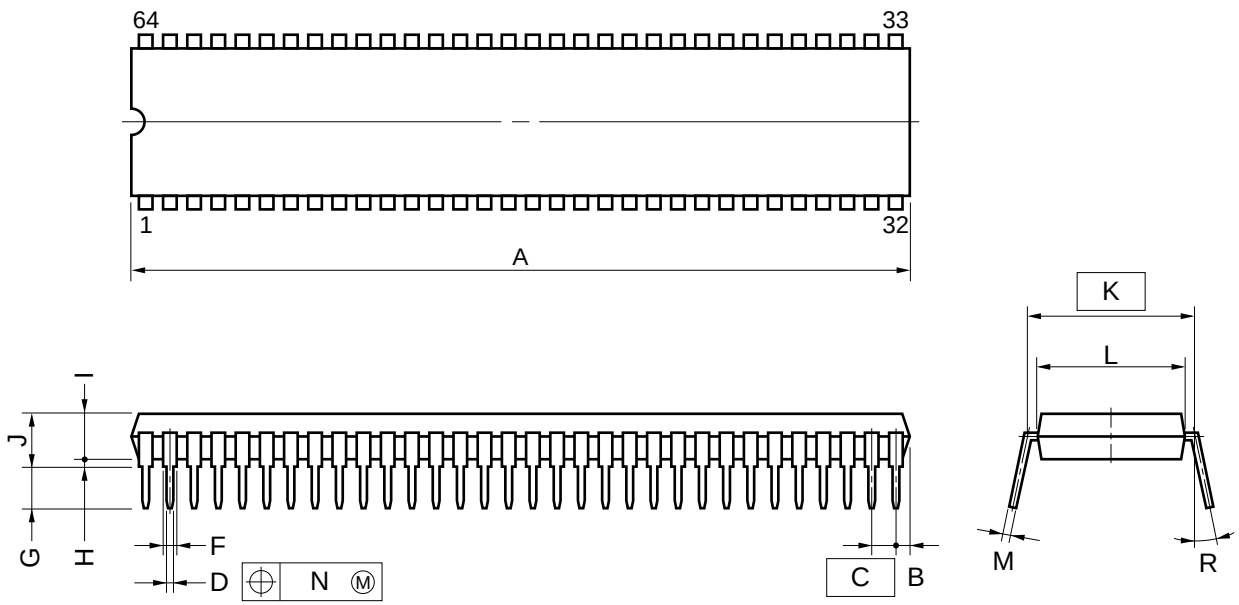
Note Does not include current flowing through EEPROM.



Note Does not include current flowing through EEPROM.

7. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



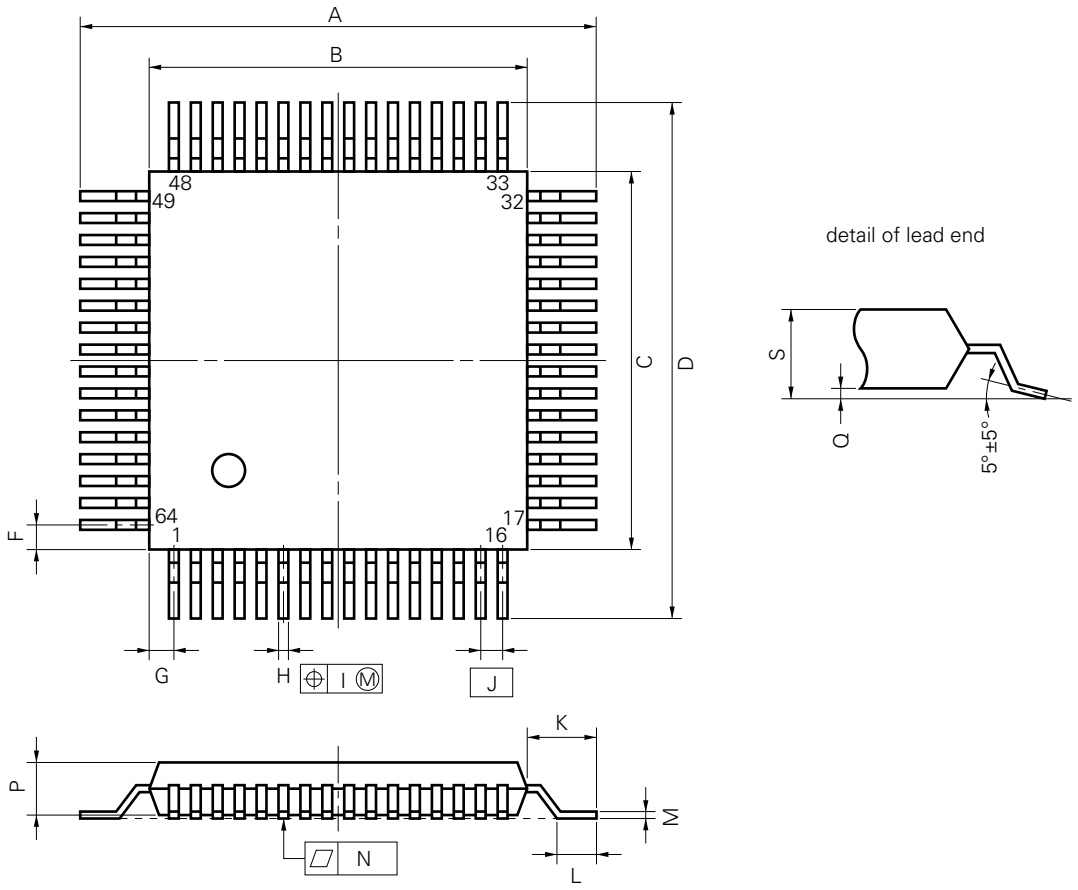
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)



P64GC-80-AB8-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

★ 8. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75P048 be soldered under the following conditions. For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-1207). For other soldering methods and conditions, consult NEC.

Table 8-1 Soldering Conditions of Surface-Mount Type

μPD75P048GC-AB8: 64-pin plastic QFP (□ 14 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 235°C, time: 30 seconds max. (210°C min.), number of times: 2 max. <Caution> (1) Start second reflow after device temperature (which has risen because of first reflow) has returned to room temperature. (2) Do not clean flux with water after first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1 max. <Caution> (1) Start second reflow after device temperature (which has risen because of first reflow) has returned to room temperature. (2) Do not clean flux with water after first reflow.	VP15-00-2
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

Caution Do not use two or more soldering methods in combination (except the pin partial heating method).

Table 8-2 Soldering Conditions of Through-Hole Type

μPD75P048CW: 64-pin plastic shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (lead parts only)	Soldering bath temperature: 260°C max., time: 10 seconds max.,
Pin Partial Heating	Pin temperature: 260°C max., time: 10 seconds max.

Caution The wave soldering must be performed at the lead part only. Note that the soldering must not be directly contacted to the board.

APPENDIX A. DEVELOPMENT TOOLS ★

The following development tools are readily available to support development of systems using μPD75P048:

Hardware	IE-75000-R Note 1 IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM Note 2	Emulation board for IE-75000-R and IE-75001-R
	EP-75028CW-R	Common emulation probe commonly used with μPD75028CW
	EP-75028GC-R EV-9200GC-64	Emulation probe commonly used with μPD75028GC, provided with EV-9200GC-64, 64-pin conversion socket
	PG-1500	PROM programmer
	PA-75P036CW	PROM programmer adapter commonly used with μPD75P036. It is connected to PG-1500.
	PA-75P036GC	PROM programmer adapter commonly used with μPD75P036GC. It is connected to PG-1500.
Software	IE Control Program	Host machine
	PG-1500 Controller	PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A Note 3)
	RA75X Relocatable Assembler	IBM PC/AT™ (Refer to **OS for IBM PC**.)

Note 1. Maintenance product

2. Not provided with IE-75001-R.

3. Ver. 5.00/5.00A has a task swap function, but this function cannot be used with this software.

Remarks For development tools from other companies, refer to **75X Series Selection Guide (IF-1027)**.

OS for IBM PC

As OS for IBM PC, the followings are supported.

OS	Version
PC DOS™	Ver. 5.02 to Ver. 6.1
MS-DOS	Ver. 3.30 to Ver. 5.00A Note 1 5.0/V Note 2
IBM DOS™	J5.02/V Note 2

Note 1. Version later than 5.0 have a task swap function, but this function cannot be used with this software.

2. This supports English mode only.

★ APPENDIX B. RELATED DOCUMENTS

Documents related to device

Document	Document No.
User's manual	IEU-1278
Instruction list	—
75X series selection guide	IF-1027

Documents related to development tools

Doument			Document No.
Hardware	IE-75000-R/IE-75001-R user's manual		EEU-1416
	IE-75000-R-EM user's manual		EEU-1294
	EP-750028CW-R user's manual		EEU-1314
	EP-75028GC-R user's manual		EEU-1306
	PG-1500 user's manual		EEU-1335
Software	RA75X assembler package user's manual	Operation	EEU-1346
		Language	EEU-1343
	PG-1500 controller user's manual		EEU1291

Other related documents

Document	Document No.
Package manual	IEI-1213
Semiconductor device - mounting maual	IEI-1207
NEC semiconductor device quality grade	IEI-1209
NEC semiconductor device reliabiliy quality control	—
Static electricity discharge (ESD) test	—
Semiconductor device quality guarantee guide	MEI-1202
Product guide related to microcomputer - other manufacturers	—

Note The documents listed above are subject to change without notice. Be sure to use the latest document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

NEC is manufacturing and selling the products under microcomputer (with on-chip EEPROM) patent license with the BULL CP8.
This product should not be used for IC cards (SMART CARD).

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