

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μ PD75P116 is a version of the μ PD75116 in which the on-chip mask ROM is replaced by one-time PROM which can be written to once only.

Since the μ PD75P116 is capable of program write by a user, it is suitable for evaluation in system development and limited production.

Detailed functional descriptions are shown in the following User's Manual. Be sure to read for design purposes.

μ PD751 $\times\times$ Series User's Manual : IEM-922

FEATURES

- μ PD75116 compatible
- Program memory (PROM) capacitance : 16256×8 bits
- Data memory (RAM) capacitance : 512×4 bits
- Single power supply $5\text{ V} \pm 10\%$

ORDERING INFORMATION

| Ordering Code | Package | Quality Grade | ★ |
|----------------------|--|---------------|---|
| μ PD75P116CW | 64-pin plastic shrink DIP (750 mil) | Standard | |
| μ PD75P116GF-3BE | 64-pin plastic QFP (14 \times 20 mm) | Standard | |

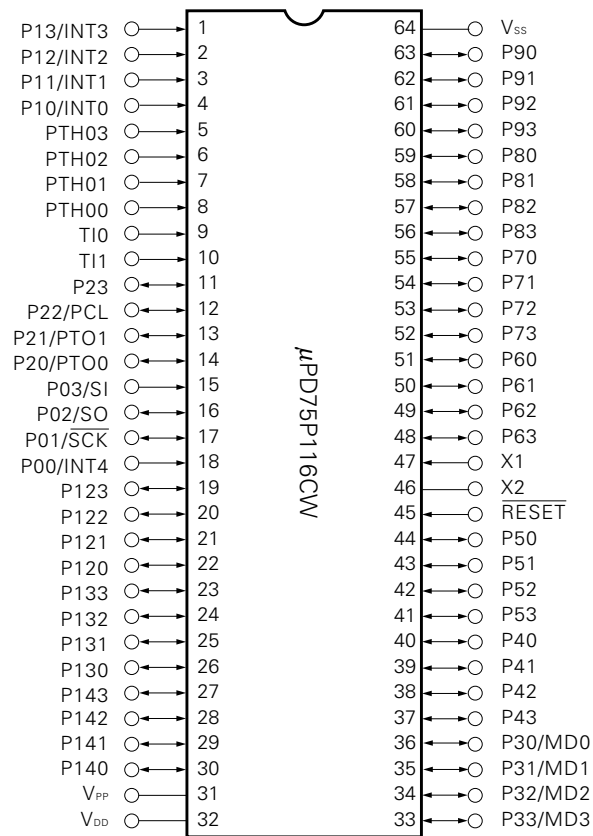
Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Note There are no on-chip pull-up resistor and power-on reset function by means of a mask option.

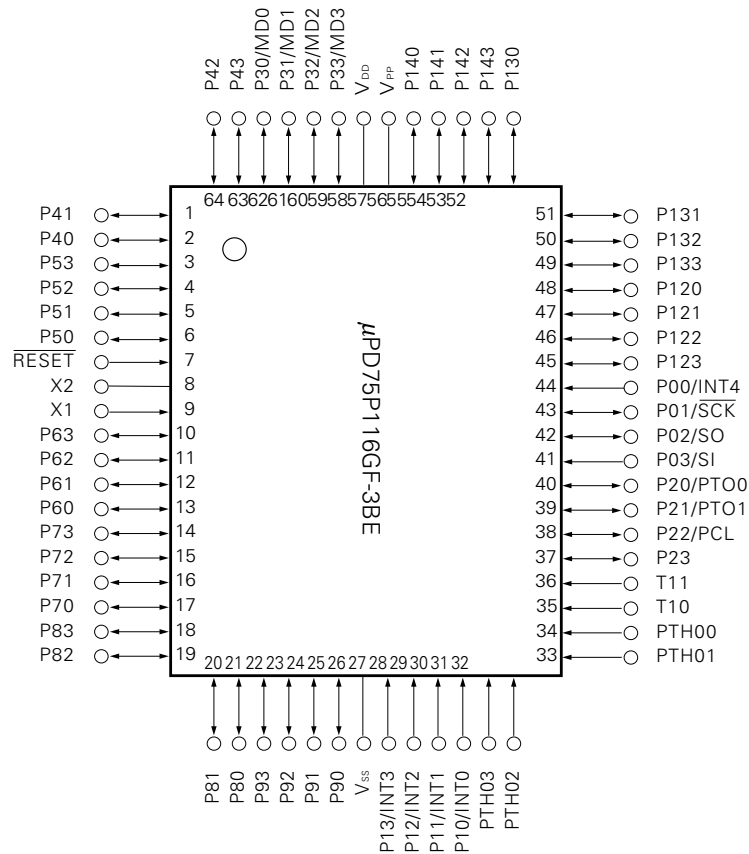
The information in this document is subject to change without notice.

PIN CONFIGURATION (TOP VIEW)

64-pin plastic shrink DIP (750 mil)



64-pin plastic QFP (14 × 20 mm)



Pin Name

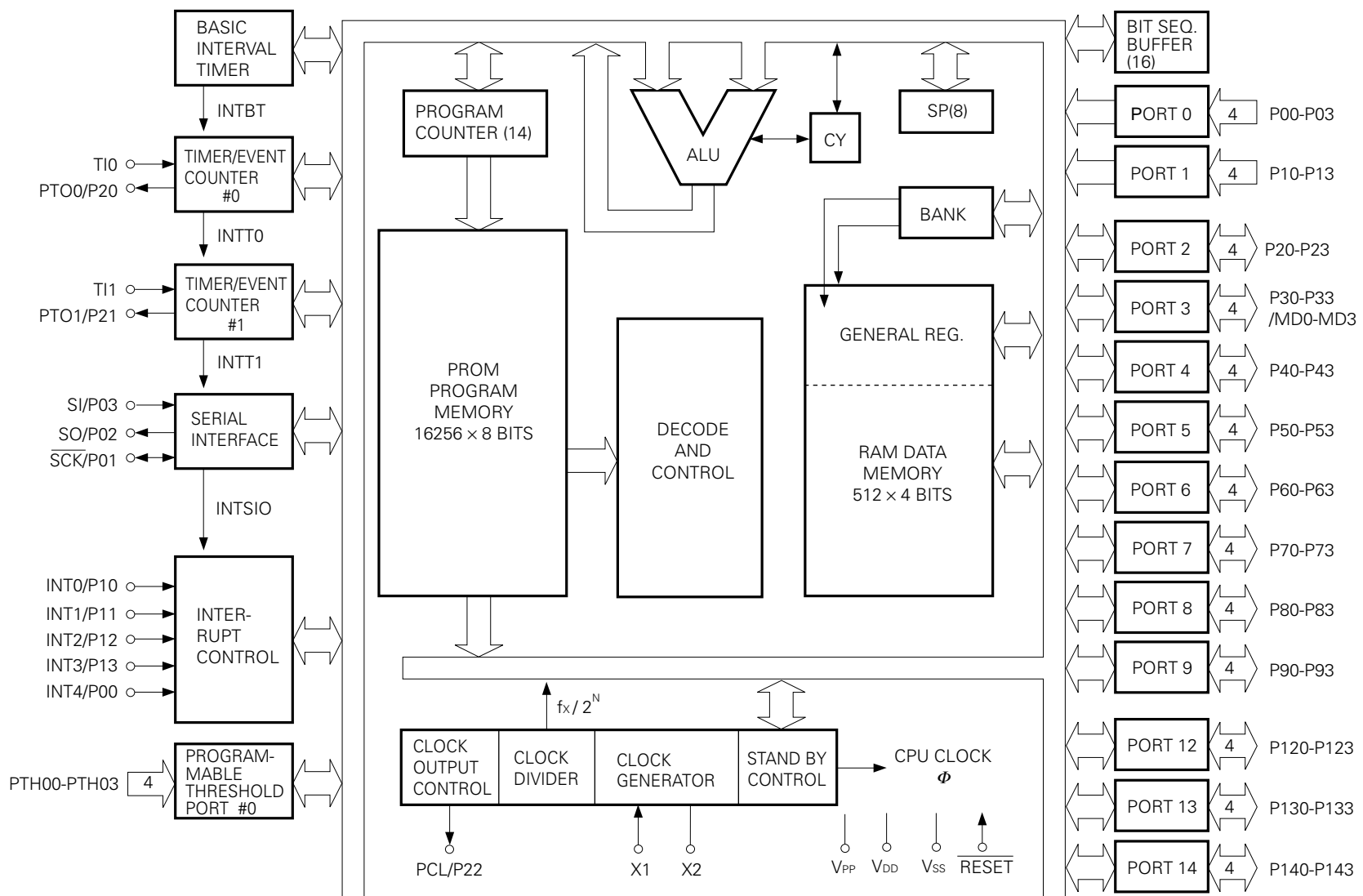
- P00 to P03 : Port 0
- P10 to P13 : Port 1
- P20 to P23 : Port 2
- P30 to P33 : Port 3
- P40 to P43 : Port 4
- P50 to P53 : Port 5
- P60 to P63 : Port 6
- P70 to P73 : Port 7
- P80 to P83 : Port 8
- P90 to P93 : Port 9
- P120 to P123 : Port 12
- P130 to P133 : Port 13
- P140 to P143 : Port 14

- SCK : Serial Clock
- SO : Serial Output
- SI : Serial Input
- PTO0, PTO1 : Programmable Timer Output
- PCL : Clock Output
- PTH00 to PTH03 : Programmable Threshold Input
- INT0, INT1, INT4 : External Vectored Interrupt Input
- INT2, INT3 : External Test Input
- T10, T11 : Timer Input
- X1, X2 : Clock Oscillation
- RESET : Reset
- NC : No Connection
- VDD : Positive Power Supply
- VSS : Ground
- VPP : Programming Power Supply
- MD0 to MD3 : Mode Selection

OVERVIEW OF FUNCTIONS

| Item | Description |
|------------------------------------|---|
| Basic instructions | 43 |
| Minimum instruction execution time | 0.95 μ s, 1.91 μ s, 15.3 μ s (4.19 MHz operation) 3-stage switching capability |
| Internal memory | ROM 16256 \times 8 |
| | RAM 512 \times 4 |
| General register | 4 bits \times 8 \times 4 banks (memory mapping) |
| Accumulator | 3 types of accumulators corresponding to bit length of manipulated data • 1-bit accumulator (CY), 4-bit accumulator (A), 8-bit accumulator (XA) |
| Input/output port | Total 58 • CMOS input pins : 10 • CMOS input/output pins (LED direct drive capability) : 32 • Middle-high voltage N-ch open-drain input/output pins (LED direct drive capability) : 12 • Comparator input pins (4-bit precision) : 4 |
| Timer/counter | • 8-bit timer/event counter \times 2 • 8-bit basic interval timer (watchdog timer applicable) |
| Serial interface | • 8 bits • LSB-first/MSB-first switchable • Two transfer modes (transmit-receive/receive-only mode) |
| Vectored interrupt | External : 3, internal : 4 |
| Test input | External : 2 |
| Standby | • STOP/HALT mode |
| Instruction set | • Various bit manipulation instructions (set, reset, test, boolean operation) • 8-bit data transfer, comparison, operation, increment/decrement instructions • 1-byte relative branch instruction • GETI instruction that can implement arbitrary 2-byte/3-byte instructions with 1 byte |
| Operating temperature range | -40 to +85 $^{\circ}$ C |
| Operating voltage | 5 V \pm 10 % |
| Others | • Bit manipulation memory (bit sequential buffer : 16 bits) on-chip |
| Package | • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 \times 20mm) |

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS 7

1.1 PORT PINS 7

1.2 OTHER PINS 8

1.3 PIN INPUT/OUTPUT CIRCUITS 9

1.4 RECOMMENDED CONNECTION OF μPD75P116 UNUSED PINS 10

1.5 NOTES ON USING P00/INT4 PIN AND RESET PIN 10

2. DIFFERENCES BETWEEN μPD75P116 AND μPD75116 11

3. PROM (PROGRAM MEMORY) WRITE AND VERIFY 12

3.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES 12

3.2 PROGRAM MEMORY WRITE PROCEDURE 13

3.3 PROGRAM MEMORY READ PROCEDURE 14

4. ELECTRICAL SPECIFICATIONS 15

5. PACKAGE INFORMATION 26

6. RECOMMENDED SOLDERING CONDITIONS 28

APPENDIX A. DEVELOPMENT TOOLS 29

APPENDIX B. RELATED DOCUMENTATION 30

1. PIN FUNCTIONS

1.1 PORT PINS

| Pin Name | Input/Output | Dual-Function Pin | Function | 8-bit I/O | After Reset | I/O Circuit Type *1 |
|------------|--------------|-------------------------|--|-----------|-------------|---------------------|
| P00 | Input | INT4 | 4-bit input port (PORT 0). | × | Input | ⓑ |
| P01 | Input/output | $\overline{\text{SCK}}$ | | | | ⓕ |
| P02 | Input/output | SO | | | | E |
| P03 | Input | SI | | | | ⓑ |
| P10 | Input | INT0 | 4-bit input port (PORT 1). | × | Input | ⓑ |
| P11 | | INT1 | | | | |
| P12 | | INT2 | | | | |
| P13 | | INT3 | | | | |
| P20 | Input/output | PTO0 | 4-bit input/output port (PORT 2). *2 | × | Input | E |
| P21 | | PTO1 | | | | |
| P22 | | PCL | | | | |
| P23 | | — | | | | |
| P30 to P33 | Input/output | MD0 to MD3 | Programmable 4-bit input/output port (PORT 3). Input/output can be specified bit-wise. *2 | × | Input | E |
| P40 to P43 | Input/output | — | 4-bit input/output port (PORT 4). Data input/output pin for program memory (PROM) write/verify (low-order 4 bits). *2 | ○ | Input | E |
| P50 to P53 | Input/output | — | 4-bit input/output port (PORT 5). Data input/output pin for program memory (PROM) write/verify (high-order 4 bits). *2 | | Input | E |
| P60 to P63 | Input/output | — | Programmable 4-bit input/output port (PORT 6). Input/output can be specified bit-wise. *2 | ○ | Input | E |
| P70 to P73 | Input/output | — | 4-bit input/output port (PORT 7). *2 | | Input | E |
| P80 to P83 | Input/output | — | 4-bit input/output port (PORT 8). *2 | ○ | Input | E |
| P90 to P93 | Input/output | — | 4-bit input/output port (PORT 9). *2 | | Input | E |
| P120-P123 | Input/output | — | N-ch open-drain 4-bit input/output port (PORT 12). +12 V withstand voltage. *2 | ○ | Input | M-A |
| P130-P133 | Input/output | — | N-ch open-drain 4-bit input/output port (PORT 13). +12 V withstand voltage. *2 | | Input | M-A |
| P140-P143 | Input/output | — | N-ch open-drain 4-bit input/output port (PORT 14). +12 V withstand voltage. *2 | — | Input | M-A |

* 1. ○ indicates Schmitt-triggered input.
 2. LED direct drive capability

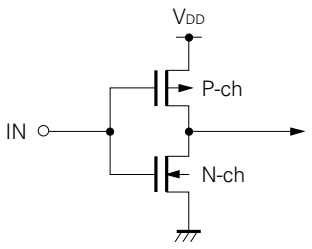
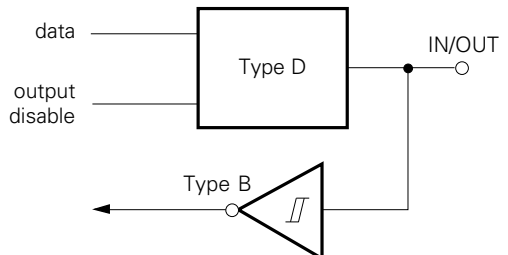
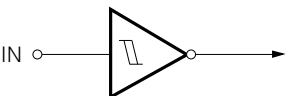
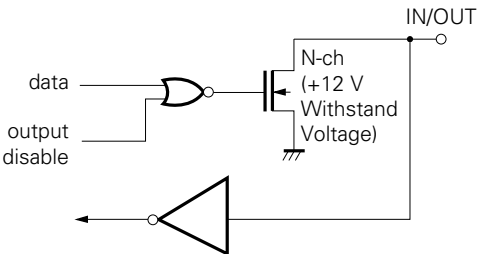
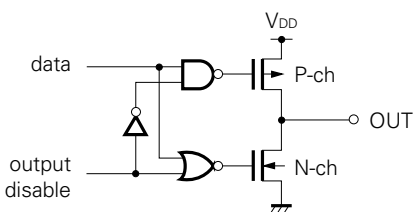
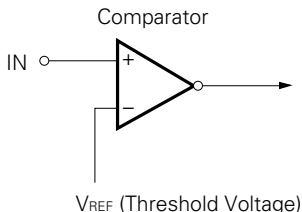
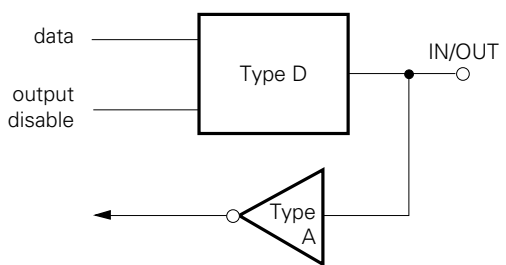
1.2 OTHER PINS

| Pin Name | Input/Output | Dual-Function Pin | Function | After Reset | I/O Circuit Type *1 |
|---------------------------|--------------|-------------------|--|-------------|---------------------|
| PTH00 to PTH03 | Input | — | Variable threshold voltage 4-bit analog input port. | | N |
| TI0 | Input | — | External event pulse input to timer/event counter. Or edge detection vectored interrupt input pin, or 1-bit input is also possible. | | ⓑ |
| TI1 | | | | | |
| PTO0 | Input/output | P20 | Timer/event counter output pin. | Input | E |
| PTO1 | | P21 | | | |
| $\overline{\text{SCK}}$ | Input/output | P01 | Serial clock input/output pin. | Input | Ⓕ |
| SO | Input/output | P02 | Serial data output pin. | Input | E |
| SI | Input | P03 | Serial data input pin. | Input | ⓑ |
| INT4 | Input | P00 | Edge detection vector interrupt input pin (detection of both rising and falling edges). | | ⓑ |
| INT0 | Input | P10 | Edge detection vector interrupt input pin (detection edge selectable). | | ⓑ |
| INT1 | | P11 | | | |
| INT2 | Input | P12 | Edge detection testable input pin (rising edge detection) | | ⓑ |
| INT3 | | P13 | | | |
| PCL | Input/output | P22 | Clock output pin | Input | E |
| X1, X2 | | — | System clock oscillation crystal/ceramic connection pin. When an external clock is used, the clock is input to X1 and the inverted clock is input to X2. | | |
| $\overline{\text{RESET}}$ | Input | — | System reset input pin (low-level active). | | ⓑ |
| MD0 to MD3 | Input/output | P30 to P33 | Mode selection pin for program memory (PROM) write/verify. | Input | E |
| V _{DD} | | — | Positive power supply pin. Applies +6 V for write/verify. | | |
| V _{SS} | | — | GND potential pin. | | |
| V _{PP} *2 | | — | Program voltage impression pin for program memory (PROM) write/verify. Connected to V _{DD} directly in normal operation. Applies +12.5 V for PROM write/verify. | | |

* 1. ○ indicates Schmitt-triggered input.
 2. The device will not operate correctly unless V_{PP} is connected to V_{DD} directly in normal use.

1.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuits of each pin of the μPD75P116 are shown by in abbreviated form.

| | |
|--|---|
| <p>Type A</p>  <p>CMOS specification input buffer</p> | <p>Type F</p>  <p>Input/output circuit made up to a Type D push-pull output and Type B Schmitt-triggered input.</p> |
| <p>Type B</p>  <p>Schmitt-triggered input with hysteresis characteristic</p> | <p>Type M-A</p>  <p>Middle-High Voltage Input Buffer (+12 V Withstand Voltage)</p> |
| <p>Type D</p>  <p>Push-pull output with high impedance output capability (P-ch and N-ch both OFF)</p> | <p>Type N</p>  <p>Comparator</p> <p>V_{REF} (Threshold Voltage)</p> |
| <p>Type E</p>  <p>This is an input/output circuit made up of a Type D push-pull output and Type A input buffer.</p> | |

1.4 RECOMMENDED CONNECTION OF μPD75P116 UNUSED PINS

| Pin | Recommended Connection |
|----------------|---|
| PTH00 to PTH03 | Connect to V _{SS} or V _{DD} . |
| T10 | |
| T11 | |
| P00 | Connect to V _{SS} . |
| P01 to P03 | Connect to V _{SS} or V _{DD} . |
| P10 to P13 | Connect to V _{SS} . |
| P20 to P23 | Input status : Connect to V _{SS} or V _{DD} . Output status : Leave open. |
| P30 to P33 | |
| P40 to P43 | |
| P50 to P53 | |
| P60 to P63 | |
| P70 to P73 | |
| P80 to P83 | |
| P90 to P93 | |
| P120 to P123 | |
| P130 to P133 | |
| P140 to P143 | |

1.5 NOTES ON USING P00/INT4 PIN AND RESET PIN

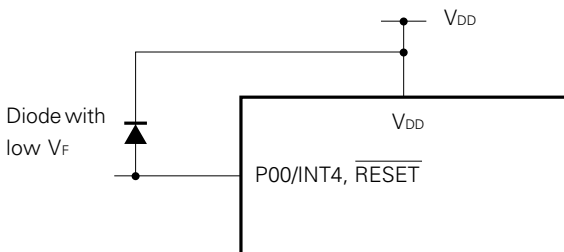
The P00/INT4 and RESET pins have a test mode setting function (for IC test) which tests internal operations of pin of the μPD75P116 in addition to those functions given in 1.1 and 1.2.

The test mode is set when voltage greater than V_{DD} is applied to either pin. Therefore, even during normal operation, the test mode is engaged when noise greater than V_{DD} is added, thus causing interference with normal operation.

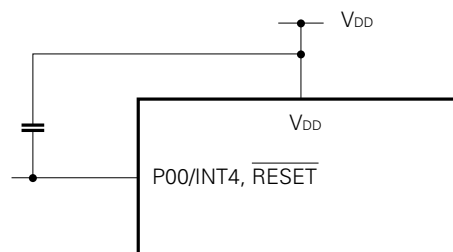
For example, this problem may occur if the P00/INT4 and RESET pins wiring is too long, causing line noise.

To avoid this, try to suppress line noise in wiring. If line noise is still high, try eliminating the noise using the exterior add-on components shown in the Figures below.

- Connect a Diode with Low V_F (0.3 V max.) Between the V_{DD} and the Pin.



- Connect a Capacitor Between the V_{DD} and the Pin.



2. DIFFERENCES BETWEEN μPD75P116 AND μPD75116

The μPD75P116 is a product in which the program memory (mask ROM) of the μPD75116 is changed to a user programmable PROM. Other functions of the μPD75P116 and μPD75116 are virtually the same only with the differences shown in Table 2-1.

For details of CPU functions and on-chip hardware, see the “μPD75116 User’s Manual” (IEM-922).

Table 2-1 Differences between μPD75P116 and μPD75116

★

| Item | | μPD75P116 | μPD75116 |
|-----------------------------------|----------------------|---|--------------|
| Program memory | | One-time PROM | Mask ROM |
| | | 0000H-3F7FH (16256 × 8 bits) | |
| Data memory | | 0000H-01FFH (512 × 4 bits) | |
| Pull-up resistor (ports 12 to 14) | | No | Mask option |
| Power-on reset function | | | |
| Operating voltage range | | 5 V ± 10 % | 2.7 to 6.0 V |
| Pin function | 31 pins (SDIP) | V _{PP} | NC |
| | 57 pins (QFP) | | |
| | 33 to 36 pins (SDIP) | P33/MD3 to P30/MD0 | P33 to P30 |
| | 59 to 62 pins (QFP) | | |
| Electrical specification | | Different consumption current, operating temperature range, etc. Refer to the electrical specifications parameters for each data sheet for details. | |
| Other | | Different noise resistance, noise radiation, etc., due to difference in the size of circuits and mask layout. | |

Note The PROM and ROM products differ in noise resistance and noise radiation. If you are considering replacement of the PROM products by the mask ROM product in the transition from preproduction to volume production, this should be thoroughly evaluated with the mask ROM CS product (not ES product).

3. PROM (PROGRAM MEMORY) WRITE AND VERIFY

The ROM built into the μPD75P116 is a 16256 × 8-bit PROM. The pins shown in the table below are used to write/verify this PROM. There is no address input; instead, a method to update the address by the clock input from the X1 pin is adopted.

| Pin Name | Function |
|---|---|
| V _{PP} | Voltage application pin for program memory write/verify (normally V _{DD} potential). |
| X1, X2 | Address update clock inputs for program memory write/verify. Inverse of X1 pin signal is input to X2 pin. |
| MD0 to MD3 | Operating mode selection pin for program memory write/verify. |
| P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits) | 8-bit data input/output pins for program memory write/verify. |
| V _{DD} | Supply voltage application pin. Applies 5 V ± 10 % in normal operation, and 6 V for program memory write/verify. |

Note Since the μPD75P116 is a one-time PROM version, UV-ray erasure is not possible.

3.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

The μPD75P116 assumes the program memory write/verify mode is +6 V and +12.5 V are applied respectively to the V_{DD} and V_{PP} pins. The table below shows the operating modes available by the MD0 to MD3 pin setting in this mode. The rest of pins are all set at the V_{SS} potential by the pull-down resistor.

| Operating Mode Setting | | | | | | Operating Mode |
|------------------------|-----------------|-----|-----|-----|-----|-----------------------------------|
| V _{PP} | V _{DD} | MD0 | MD1 | MD2 | MD3 | |
| +12.5 V | +6 V | H | L | H | L | Program memory address zero-clear |
| | | L | H | H | H | Write mode |
| | | L | L | H | H | Verify mode |
| | | H | × | H | H | Program inhibit mode |

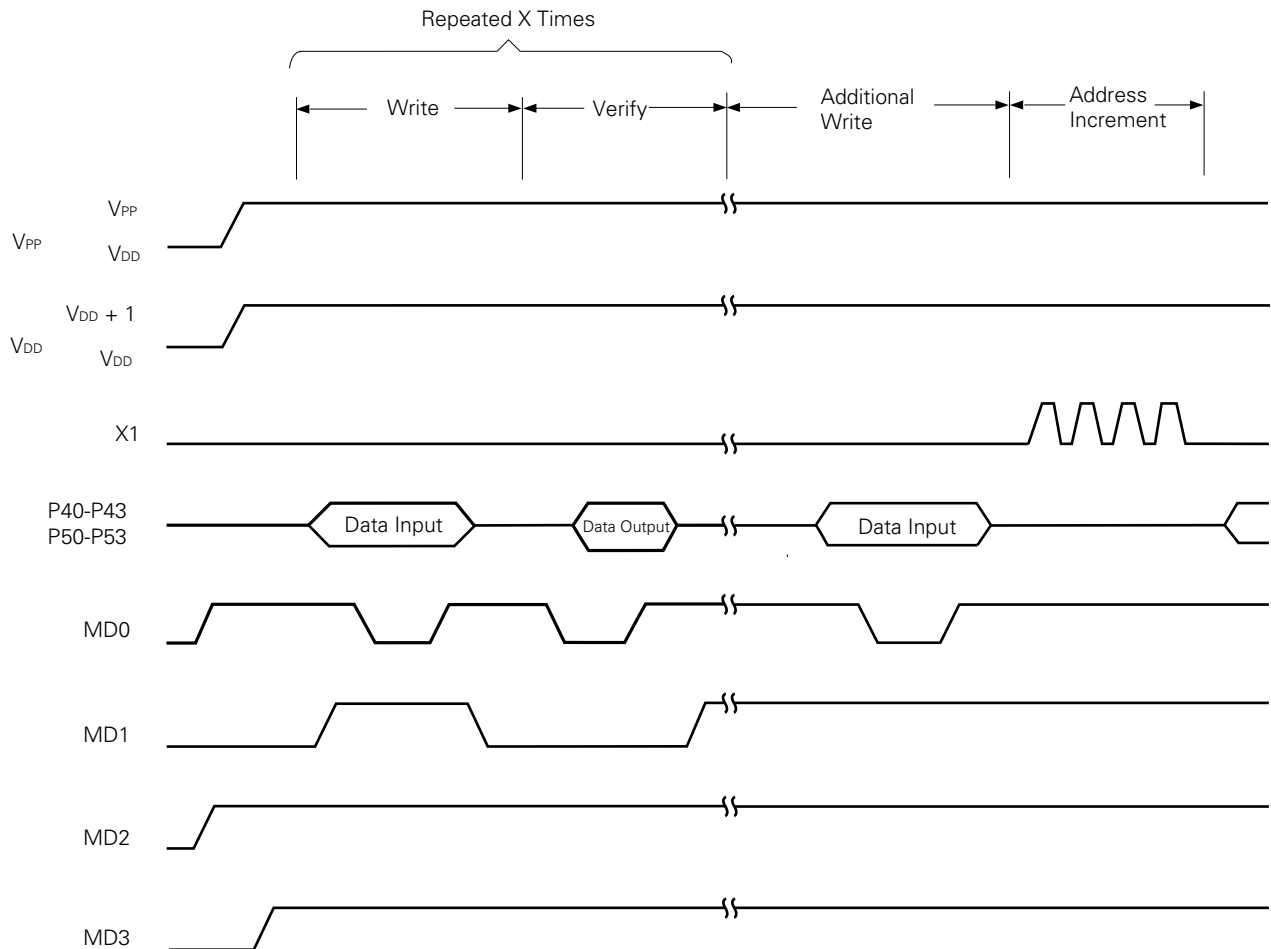
×: L or H

3.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

- (1) Pull down a pin which is not used to V_{SS} via the resistor. A low-level signal is input to the X1 pin.
- (2) Supply +5 V to the V_{DD} and V_{PP} pins.
- (3) 10 μs wait.
- (4) The program memory address 0 clear mode.
- (5) Supply +6 V and +12.5 V respectively to V_{DD} and V_{PP}.
- (6) The program inhibit mode.
- (7) Write data in the 1-ms write mode.
- (8) The program inhibit mode.
- (9) The verify mode. If written, proceed to (10); if not written, repeat (7) to (9).
- (10) (Number of times written in (7) to (9): X) × 1-ms additional write.
- (11) The program inhibit mode.
- (12) Update (+1) the program memory address by inputting 4 pulses to the X1 pin.
- (13) Repeat (7) to (12) up to the last address.
- (14) The program memory address 0 clear mode.
- (15) Change the V_{DD} and V_{PP} pins voltage to +5 V.
- (16) Power off.

The diagram below shows the procedure of the above (2) to (12).

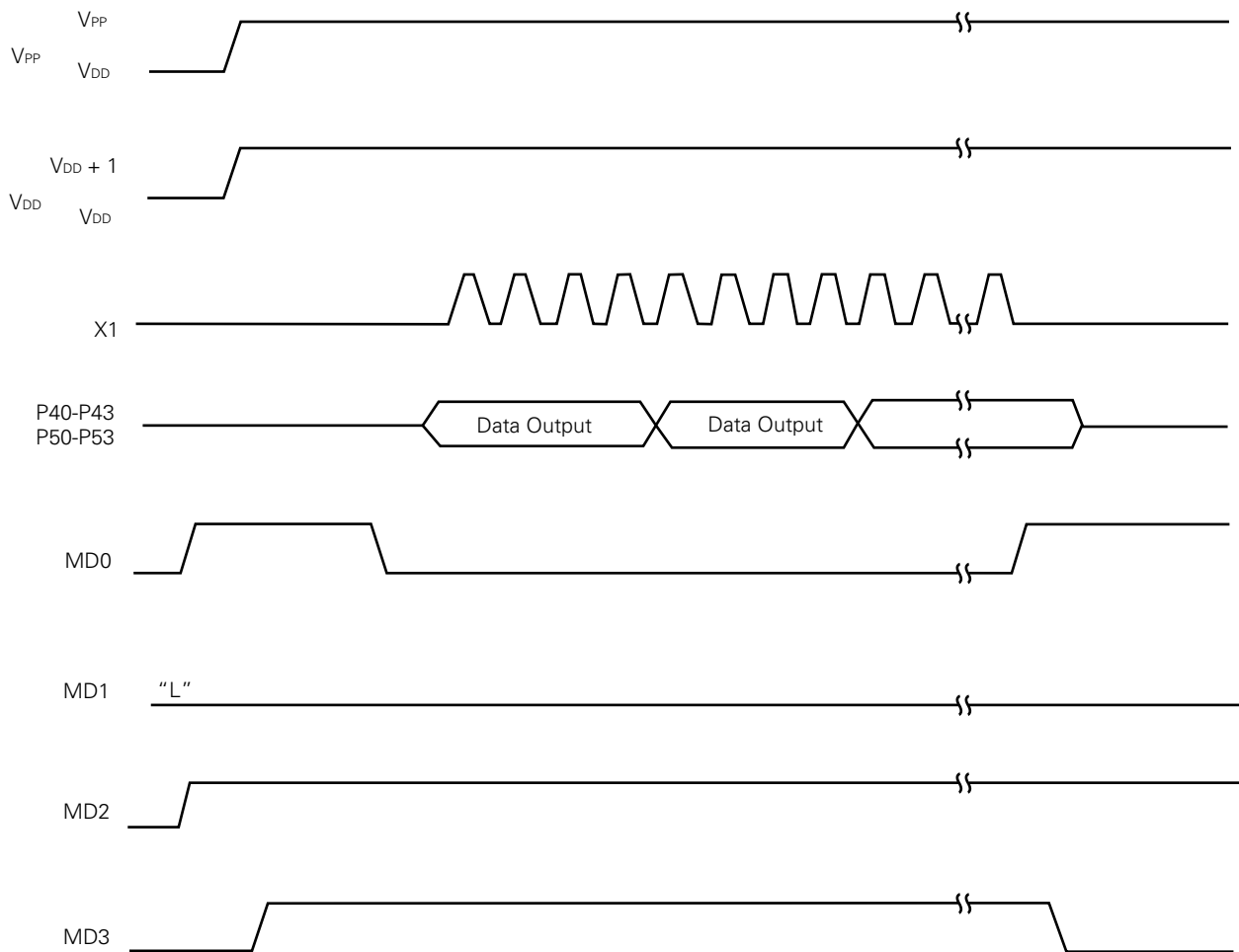


3.3 PROGRAM MEMORY READ PROCEDURE

The μPD75P116 can read the content of the program memory in the following procedure.

- (1) Pull down a pin which is not used to V_{SS} via the resistor. A low-level signal is input to the X1 pin.
- (2) Supply +5 V to the V_{DD} and V_{PP} pins.
- (3) 10 μs wait.
- (4) The program memory address 0 clear mode.
- (5) Supply +6 V and +12.5 V respectively to V_{DD} and V_{PP}.
- (6) The program inhibit mode.
- (7) The verify mode. If clock pulses are input to the X1 pin, data is output sequentially 1 address at a time at the period of inputting 4 pulses.
- (8) The program inhibit mode.
- (9) The program memory address 0 clear mode.
- (10) Change the V_{DD} and V_{PP} pins voltage to +5 V.
- (11) Power off.

The diagram below shows the procedure of the above (2) to (9).



4. ELECTRICAL SPECIFICATIONS

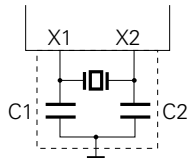
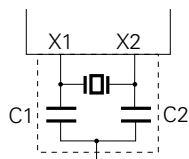
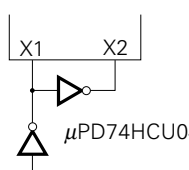
ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

| PARAMETER | SYMBOL | TEST CONDITIONS | RATING | UNIT | |
|-----------------------|--------------------|---------------------------------|-------------------------------|------|----|
| Supply voltage | V _{DD} | | -0.3 to + 7.0 | V | |
| Supply voltage | V _{PP} | | -0.3 to 13.5 | V | |
| Input voltage | V _{I1} | Except ports 12 to 14 | -0.3 to V _{DD} + 0.3 | V | |
| | V _{I2} *1 | Ports 12 to 14 | -0.3 to +13 | V | |
| Output voltage | V _O | | -0.3 to V _{DD} + 0.3 | V | |
| Output current high | I _{OH} | 1 pin | -15 | mA | |
| | | Total pins | -30 | mA | |
| Output current low | I _{OL} *2 | 1 pin | Peak value | 30 | mA |
| | | | Effective value | 15 | mA |
| | | Ports 0, 2 to 4, 12 to 14 total | Peak value | 100 | mA |
| | | | Effective value | 36 | mA |
| | | Ports 5 to 9 total | Peak value | 100 | mA |
| | | | Effective value | 36 | mA |
| Operating temperature | T _{opt} | | -40 to +85 | °C | |
| Storage temperature | T _{stg} | | -65 to +125 | °C | |

- * 1. The power supply impedance (pull-up resistor) should be 50 kΩ or more when the voltage exceeding 10 V applied to ports 12, 13 and 14.
- 2. Effective value should be calculated as follows: [Effective value] = [Peak value] × √*duty*

Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

OSCILLATION CIRCUIT CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 5 V ± 10 %)

| RESONATOR | RECOMMENDED CIRCUIT | PARAMETER | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------|---|--|--------------------------------------|------|------|-----------|------|
| Ceramic resonator |  | Oscillator frequency (f _{xx}) *1 | | 2.0 | | *3 5.0 | MHz |
| | | Oscillation stabilization time *2 | After V _{DD} reaches 4.5 V. | | | 4 | ms |
| Crystal resonator |  | Oscillator frequency (f _{xx}) *1 | | 2.0 | 4.19 | *3 5.0 | MHz |
| | | Oscillation stabilization time *2 | After V _{DD} reaches 4.5 V. | | | 10 | ms |
| External clock |  | X1 input frequency (f _x) *1 | | 2.0 | | *3 5.0 | MHz |
| | | X1 input high/low level width (t _{xH} , t _{xL}) | | 100 | | 250 | ns |

- * 1. Indicates only oscillation circuit characteristics. Refer to “AC Characteristics” for instruction execution time.
- 2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN. or STOP mode release.
- ★ 3. When the oscillator frequency is 4.19 MHz < f_{xx} ≤ 5.0MHz, PCC = 0011 should not be selected as instruction execution time. If PCC = 0011 is selected, 1 machine cycle becomes less than 0.95 μs, with the result that the specified MIN value of 0.95 μs cannot be observed.

★ Note When the system clock oscillator is used, the following points should be noted concerning wiring in the section enclosed by dots, in order to prevent the effects of wiring capacitance, etc.

- Keep the wiring as short as possible.
- Do not cross any other signal lines.
- Keep away from lines in which a high fluctuating current flows.
- Ensure that oscillator capacitor connection points are always at the same potential as V_{SS}. Do not ground in a ground pattern in which a high current flows.
- Do not take a signal from the oscillator.

DC CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 5 V ± 10 %)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|-----------------------------|-------------------|--|--------------------------------|-----------------------------|------|--------------------|------|
| Input voltage high | V _{IH1} | Other than below | | 0.7V _{DD} | | V _{DD} | V |
| | V _{IH2} | Ports 0 & 1, TIO & 1, $\overline{\text{RESET}}$ | | 0.8V _{DD} | | V _{DD} | V |
| | V _{IH3} | Ports 12 to 14 | | 0.7V _{DD} | | 12 | V |
| | V _{IH4} | X1, X2 | | V _{DD} -0.5 | | V _{DD} | V |
| Input voltage low | V _{IL1} | Other than below | | 0 | | 0.3V _{DD} | V |
| | V _{IL2} | Ports 0 & 1, TIO & 1, $\overline{\text{RESET}}$ | | 0 | | 0.2V _{DD} | V |
| | V _{IL3} | X1, X2 | | 0 | | 0.4 | V |
| Output voltage high | V _{OH} | I _{OH} = -1 mA | | V _{DD} -1.0 | | | V |
| Output voltage low | V _{OL} | I _{OL} = 15 mA | Ports 0, 2, to 9 | | 0.55 | 2.0 | V |
| | | I _{OL} = 10 mA | Ports 12 to 14 | | 0.35 | 2.0 | V |
| | | I _{OL} = 1.6 mA | | | | 0.4 | V |
| Input leakage current high | I _{LIH1} | V _{IN} = V _{DD} | Other than below | | | 3 | μA |
| | I _{LIH2} | | X1, X2 | | | 20 | μA |
| | I _{LIH3} | V _{IN} = 12 V | Ports 12 to 14 | | | 20 | μA |
| Input leakage current low | I _{LIL1} | V _{IN} = 0 V | Except X1 & X2 | | | -3 | μA |
| | I _{LIL2} | | X1, X2 | | | -20 | μA |
| Output leakage current high | I _{LOH1} | V _{OUT} = V _{DD} | Other than below | | | 3 | μA |
| | I _{LOH2} | V _{OUT} = 12 V | Ports 12 to 14 | | | 20 | μA |
| Output leakage current low | I _{LOL} | V _{OUT} = 0 V | | | | -3 | μA |
| Power supply current *1 | I _{DD1} | 4.19 MHz Crystal oscillation C1 = C2 = 22 pF | V _{DD} = 5 V ± 5 % *2 | | 5 | 10 | mA |
| | I _{DD2} | | HALT mode*3 | V _{DD} = 5 V ± 5 % | 500 | 1500 | μA |
| | I _{DD3} | STOP mode, V _{DD} = 5 V ± 5 % | | | 0.5 | 20 | μA |

- * 1. Not including current flowing in comparator.
- 2. When processor clock control register (PCC) is set to 0011 operating in high-speed mode.
- 3. When PCC is set to 0100 and CPU is halted in HALT mode.

CAPACITANCE (Ta = 25 °C, VDD = 0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------|------------------|---|------|------|------|------|
| Input capacitance | C _{IN} | f = 1 MHz Unmeasured pins returned to 0 V. | | | 15 | pF |
| Output capacitance | C _{OUT} | | | | 15 | pF |
| I/O capacitance | C _{IO} | | | | 15 | pF |

COMPARATOR CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 5 V ± 10 %)

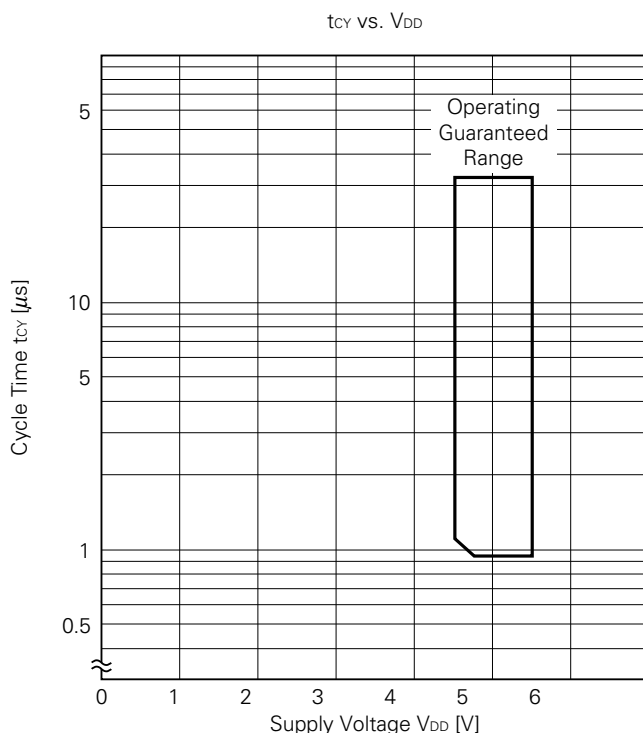
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--------------------|------------------|------|------|-----------------|------|
| Comparison accuracy | V _{ACOMP} | | | | ±100 | mV |
| Threshold voltage | V _{TH} | | 0 | | V _{DD} | V |
| PTH input voltage | V _{IPTH} | | 0 | | V _{DD} | V |
| Comparator circuit current consumption | | PTHM7 set to "1" | | 1 | | mA |

AC CHARACTERISTICS (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|---------------------------------|------------------------|------|------|------|
| CPU clock cycle time* (minimum instruction execution time = 1 machine cycle) | t _{cy} | V _{DD} = 4.75 to 5.5 V | 0.95 | | 32 | μs |
| | | | 1.1 | | 32 | μs |
| TI input frequency | f _{TI} | | 0 | | 1 | MHz |
| TI input high/low-level width | t _{TIH} , t _{TIL} | | 0.48 | | | μs |
| SCK cycle time | t _{KCY} | Input | 0.8 | | | μs |
| | | Output | 0.95 | | | μs |
| SCK high/low-level width | t _{KH} , t _{KL} | Input | 0.4 | | | μs |
| | | Output | t _{KCY} /2-50 | | | ns |
| SI setup time (to SCK↑) | t _{SIK} | | 100 | | | ns |
| SI hold time (from SCK↑) | t _{KSI} | | 400 | | | ns |
| SO output delay time from SCK↓ | t _{KSO} | | | | 300 | ns |
| INT0 to INT4 high/low-level width | t _{INTH} , t _{INTL} | | 5 | | | μs |
| RESET low level width | t _{RSL} | | 5 | | | μs |

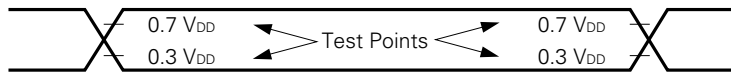
- * The cycle time of the CPU clock (Φ) is determined by the oscillator frequency of the connected resonator and the processor clock control register (PCC).
The graph on the below shows the cycle time t_{cy} characteristics against supply voltage V_{DD}.

Relation between Cycle Time and Supply Voltage

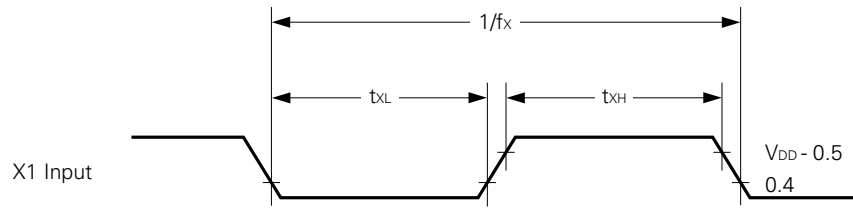


Note t_{cy} vs. V_{DD} characteristics are different from those of the μPD75P108

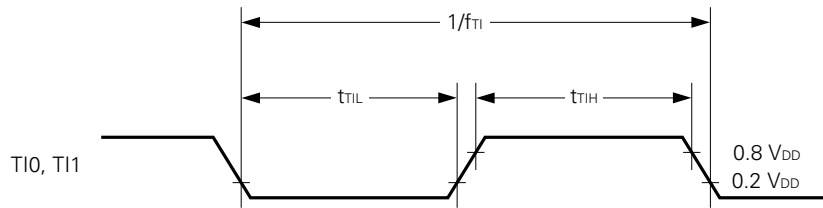
AC Timing Test Point (Excluding ports 0 & 1, T10, T11, X1, X2, RESET)



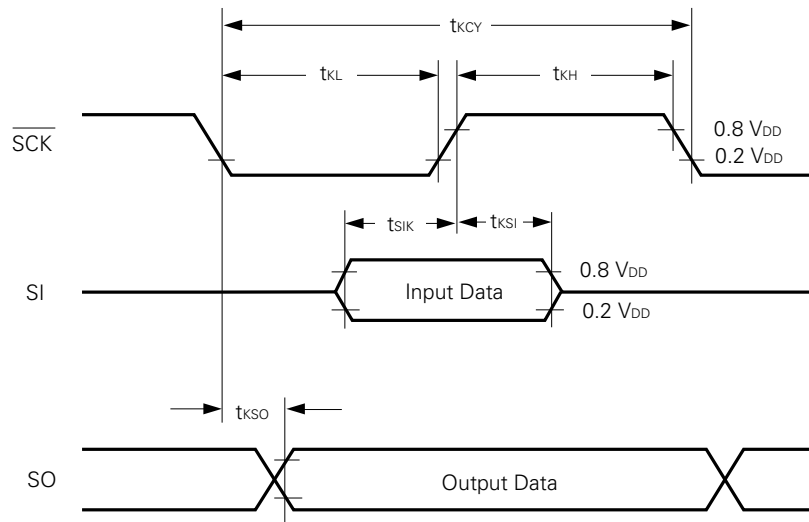
Clock Timing



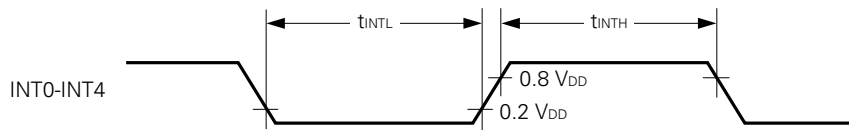
T1 Input Timing



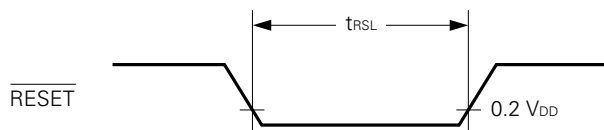
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



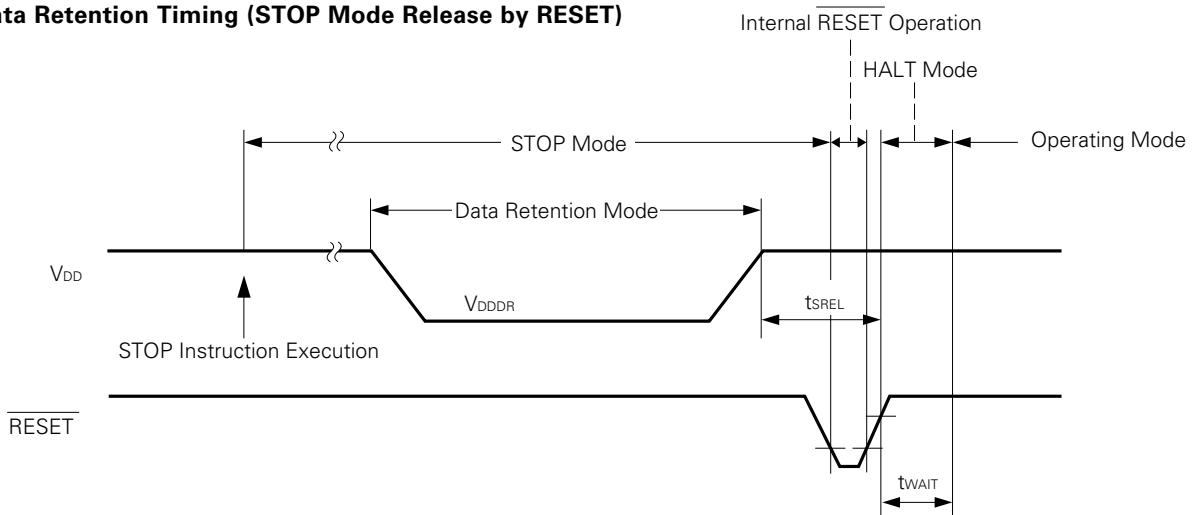
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = -40 to +85 °C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|-------------------|--------------------------------------|------|---------------------------------|------|------|
| Data retention supply voltage | V _{DDDR} | | 2.0 | | 5.5 | V |
| Data retention power supply current *1 | I _{DDDR} | V _{DDDR} = 2.0 V | | 0.1 | 10 | μA |
| Release signal set time | t _{SREL} | | 0 | | | μs |
| Oscillation stabilization wait time *2 | t _{WAIT} | Release by $\overline{\text{RESET}}$ | | 2 ¹⁷ /f _x | | ms |
| | | Release by interrupt request | | *3 | | ms |

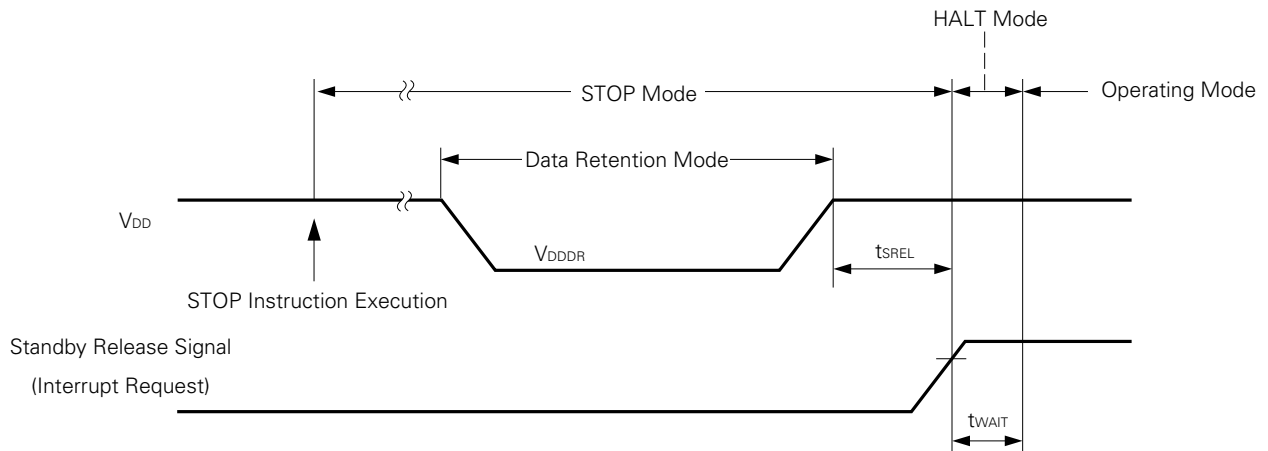
- * 1. Does not include current flowing in the comparator.
- 2. The oscillator stabilization wait time is the time during which CPU operation is halted to prevent unstable operation when oscillation begins.
- 3. Depends on the setting of the basic interval timer mode register (BTM) (table below).

| BTM3 | BTM2 | BTM1 | BTM0 | WAIT Time (Figure in Parentheses is for f _{xx} = 4.19 MHz) |
|------|------|------|------|---|
| - | 0 | 0 | 0 | 2 ²⁰ /f _{xx} (Approx. 250 ms) |
| - | 0 | 1 | 1 | 2 ¹⁷ /f _{xx} (Approx. 31.3 ms) |
| - | 1 | 0 | 1 | 2 ¹⁵ /f _{xx} (Approx. 7.82 ms) |
| - | 1 | 1 | 1 | 2 ¹³ /f _{xx} (Approx. 1.95 ms) |

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



DC PROGRAMMING CHARACTERISTICS (Ta = 25 °C, VDD = 6.0 ±0.25 V, VPP = 12.5 ±0.3 V, VSS = 0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|------------------|--|----------------------|------|---------------------|------|
| Input voltage high | V _{IH1} | Except X1 & X2 | 0.7V _{DD} | | V _{DD} | V |
| | V _{IH2} | X1, X2 | V _{DD} -0.5 | | V _{DD} | V |
| Input voltage low | V _{IL1} | Except X1 & X2 | 0 | | 0.3 V _{DD} | V |
| | V _{IL2} | X1, X2 | 0 | | 0.4 | V |
| Input leakage current | I _{LI} | V _{IN} = V _{IL} or V _{IH} | | | 10 | μA |
| Output voltage high | V _{OH} | I _{OH} = -1 mA | V _{DD} -1.0 | | | V |
| Output voltage low | V _{OL} | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{DD} supply current | I _{DD} | | | | 30 | mA |
| V _{PP} supply current | I _{PP} | MD0 = V _{IL} , MD1 = V _{IH} | | | 30 | mA |

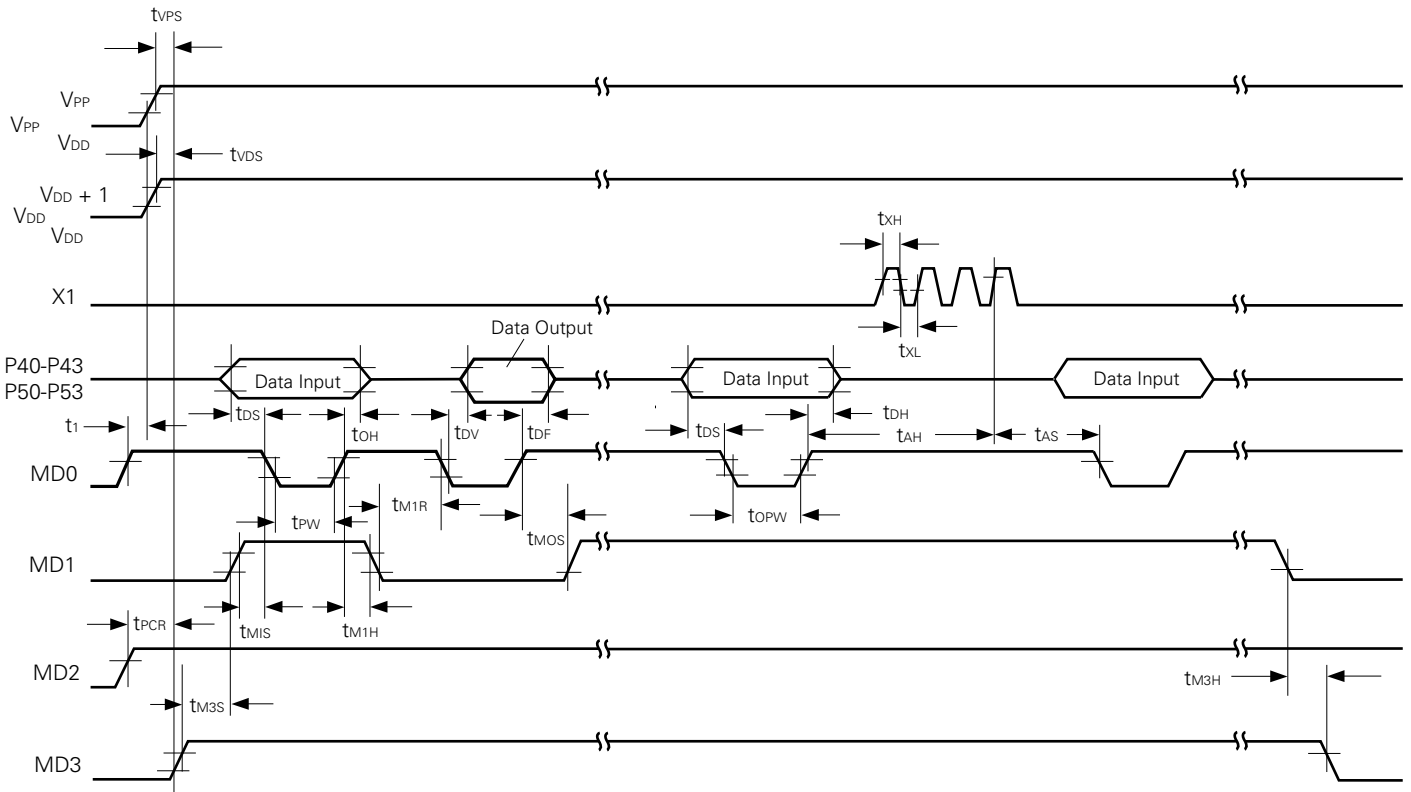
- Note 1. Ensure that V_{PP} does not reach +13.5 V or above including overshoot.**
2. Ensure that V_{DD} is applied before V_{PP} and cut off after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (Ta = 25 °C, VDD = 6.0 ±0.25 V, VPP = 12.5 ±0.3 V, VSS = 0 V)

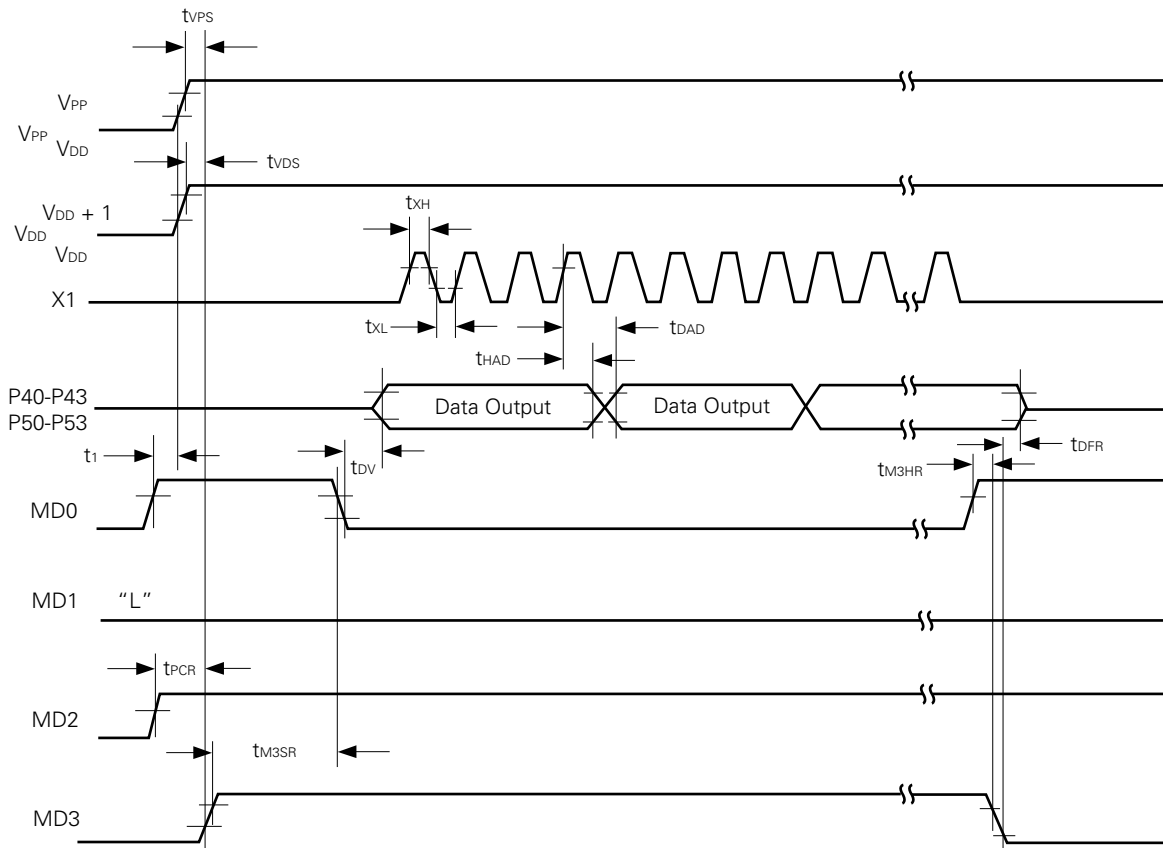
| PARAMETER | SYMBOL | *1 | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|----------|------|------------------------|-------|------|------|------|
| Address setup time *2 (to MD0↓) | tAS | tAS | | 2 | | | μs |
| MD1 setup time (to MD0↓) | tM1S | tOES | | 2 | | | μs |
| Data setup time (to MD0↓) | tDS | tDS | | 2 | | | μs |
| Address hold time *2 (from MD0↑) | tAH | tAH | | 2 | | | μs |
| Data hold time (from MD0↑) | tDH | tDH | | 2 | | | μs |
| Data output float delay time from MD0↑ | tDF | tDF | | 0 | | 130 | ns |
| VPP setup time (to MD3↑) | tVPS | tVPS | | 2 | | | μs |
| VDD setup time (to MD3↑) | tVDS | tVCS | | 2 | | | μs |
| Initial program pulse width | tPW | tPW | | 0.95 | 1.0 | 1.05 | ms |
| Additional program pulse width | tOPW | tOPW | | 0.95 | | 21.0 | ms |
| MD0 setup time (to MD1↑) | tMOS | tCES | | 2 | | | μs |
| Data output delay time from MD0↓ | tDV | tDV | MD0 = MD1 = VIL | | | 1 | μs |
| MD1 hold time (from MD0↑) | tM1H | tOEH | tM1H + tM1R ≥ 50 μs | 2 | | | μs |
| MD1 recovery time (from MD0↓) | tM1R | tOR | | 2 | | | μs |
| Program counter reset time | tPCR | — | | 10 | | | μs |
| X1 input high-/low-level width | tXH, tXL | — | | 0.125 | | | μs |
| X1 input frequency | fX | — | | | | 4.19 | MHz |
| Initial mode setting time | tI | — | | 2 | | | μs |
| MD3 setup time (to MD1↑) | tM3S | — | | 2 | | | μs |
| MD3 hold time (from MD1↓) | tM3H | — | | 2 | | | μs |
| MD3 setup time (to MD0↓) | tM3SR | — | In program memory read | 2 | | | μs |
| Data output delay time from address *2 | tDAD | tACC | In program memory read | 2 | | | μs |
| Data output hold time from address *2 | tHAD | tOH | In program memory read | 0 | | 130 | ns |
| MD3 hold time (from MD0↑) | tM3HR | — | In program memory read | 2 | | | μs |
| Data output float delay time from MD3↓ | tDFR | — | In program memory read | 2 | | | μs |

- * 1. Corresponding to μPD27C256 symbol.
- 2. Internal address signal is incremented by 1 on rise of 4th X1 input, and is not connected to a pin.

Program Memory Write Timing

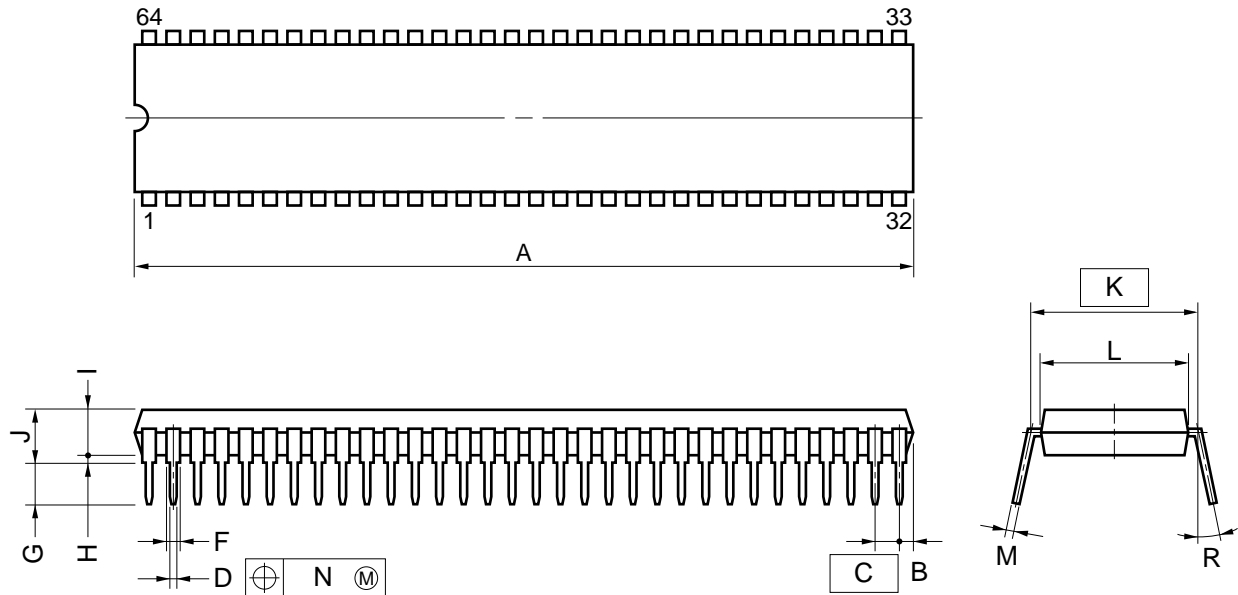


Program Memory Read Timing



5. PACKAGE INFORMATION

64 PIN PLASTIC SHRINK DIP (750 mil)



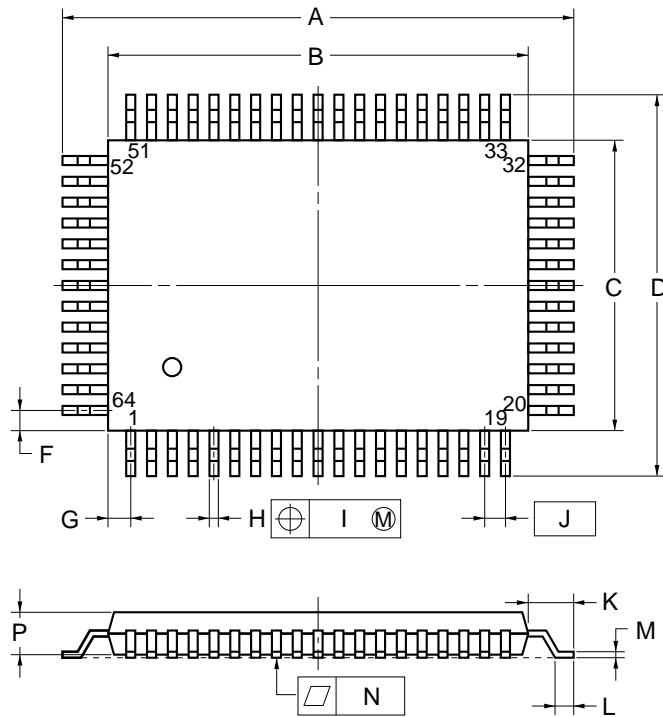
NOTE

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

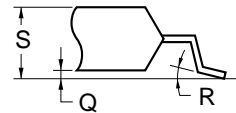
| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 58.68 MAX. | 2.311 MAX. |
| B | 1.78 MAX. | 0.070 MAX. |
| C | 1.778 (T.P.) | 0.070 (T.P.) |
| D | 0.50±0.10 | 0.020 ^{+0.004} _{-0.005} |
| F | 0.9 MIN. | 0.035 MIN. |
| G | 3.2±0.3 | 0.126±0.012 |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 19.05 (T.P.) | 0.750 (T.P.) |
| L | 17.0 | 0.669 |
| M | 0.25 ^{+0.10} _{-0.05} | 0.010 ^{+0.004} _{-0.003} |
| N | 0.17 | 0.007 |
| R | 0~15° | 0~15° |

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 23.6±0.4 | 0.929±0.016 |
| B | 20.0±0.2 | 0.795 ^{+0.008} _{-0.009} |
| C | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| D | 17.6±0.4 | 0.693±0.016 |
| F | 1.0 | 0.039 |
| G | 1.0 | 0.039 |
| H | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| I | 0.20 | 0.008 |
| J | 1.0 (T.P.) | 0.039 (T.P.) |
| K | 1.8±0.2 | 0.071 ^{+0.008} _{-0.009} |
| L | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| M | 0.15 ^{+0.10} _{-0.05} | 0.006 ^{+0.004} _{-0.003} |
| N | 0.10 | 0.004 |
| P | 2.7 | 0.106 |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 3.0 MAX. | 0.119 MAX. |

P64GF-100-3B8,3BE,3BR-2

★ 6. RECOMMENDED SOLDERING CONDITIONS

The μPD75P116 should be mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document “Surface Mount Technology Manual” (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 6-1 Surface Mount Type Soldering Conditions

μPD75P116GF-3BE : 64-pin plastic QFP (14 × 20 mm)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|------------------|---|------------------------------|
| Infrared reflow | Package peak temperature: 230°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C) | IR30-162-1 |
| VPS | Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C) | VP15-162-1 |
| Wave soldering | Solder bath temperature: 260°C max., Duration: 10 sec. max Number of times: Once Preheating temperature: 120°C max. (package surface temperature), Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C) | WS60-162-1 |
| Pin part heating | Pin part temperature: 300°C max., Duration: 3 sec. max. (per device side) | — |

* For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% 1H.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 6-2 Insertion Type Soldering Conditions

μPD75P116CW : 64-pin plastic shrink DIP (750 mil)

| Soldering Method | Soldering Conditions |
|---------------------------------|--|
| Wave Soldering (lead part only) | Solder bath temperature: 260°C max., Duration: 10sec. max. |
| Pin part heating | Pin part temperature: 260°C max., Duration: 10sec. max. |

Note Ensure that the application of (wave soldering) is limited to the lead part and no solder touches the main unit directly.

Notice

A version of this product with improved recommended soldering conditions is available. For details (improvements such as infrared reflow peak temperature extension (230 °C), number of times: twice, relaxation of time limit, etc.), contact NEC sales personnel.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75P116.

| | | |
|----------|-----------------------------|--|
| Hardware | IE-75000-R *1 IE-75001-R | In-circuit emulator for 75X series |
| | IE-75000-R-EM *2 | Emulation board for IE-75000-R and IE-75001-R |
| | EP-75108CW-R | Emulation probe for μPD75P116CW |
| | EP-75108GF-R EV-9200G-64 | Emulation probe for μPD75P116GF A 64-pin conversion socket EV-9200G-64 is provided. |
| | PG-1500 | PROM programmer |
| | PA-75P108CW | This is a PROM programmer adapter for μPD75P116CW and connects to PG-1500. |
| | PA-75P116GF | This is a PROM programmer adapter for μPD75P116GF and connects to PG-1500. |
| Software | IE control program | Host machine • PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A *3) • IBM PC/AT™ series (PC DOS™ Ver.3.1) |
| | PG-1500 controller | |
| | RA75X relocatable assembler | |

- * 1 Maintenance product
- 2 This is not incorporated in the IE-75001-R.
- 3 A task swap function is provided with Ver.5.00/5.00A; however, a task swap function cannot be used with this software.

Remarks For development tools manufactured by a third party, see the “75X Series Selection Guide” (IF-151).

★ **APPENDIX B. RELATED DOCUMENTATION**

List of Device-Related Documents

| Document Name | | Document No. |
|-------------------------------|---|--------------|
| User's Manual | | |
| Instruction Application Table | | |
| Application Note | (I) Introductory Volume | |
| | (II) Remote-Controlled Reception Volume | |
| | (III) Bar-Code Reader-Volume | |
| | (IV) IC Control for MSK Transmission/Reception Volume | |
| 75X Series Selection Guide | | |

List of Development Tool Related Documents

| Document Name | | Document No. |
|---------------|---------------------------------------|------------------|
| Hardware | IE-75000-R/IE-75001-R User's Manual | |
| | IE-75000-R-EM User's Manual | |
| | EP-75108CW-R User's Manual | |
| | EP-75108GF-R User's Manual | |
| | PG-1500 User's Manual | |
| Software | RA75X Assembler Package User's Manual | Operation Volume |
| | | Language Volume |
| | PG-1500 Controller User's Manual | |

Other Documents

| Document Name | Document No. |
|---|--------------|
| Package Manual | |
| Surface Mount Technology Manual | |
| Quality Grade on NEC Semiconductor Devices | |
| NEC Semiconductor Device Reliability Quality Control | |
| Electrostatic Discharge (ESD) Test | |
| Semiconductor Device Quality Guarantee Guide | |
| Microcomputer Related Product Guide Other Manufacturer Volume | |

Note The above related documents may be changed without notice. Be sure to use the latest documents for design purposes.

[MEMO]

[MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

The devices listed in this document are not suitable for use in aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. If customers intend to use NEC devices for above applications or they intend to use "Standard" quality grade NEC devices for applications not intended by NEC, please contact our sales people in advance.

Application examples recommended by NEC Corporation

Standard : Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special : Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

M4 92.6

MS-DOS is a trademark of Microsoft Corporation.

PC DOS and PC/AT are trademarks of IBM Corporation.