NEC

MOS INTEGRATED CIRCUIT

μPD78052,78053,78054,78055,78056,78058

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78052,78053,78054,78055,78056 and 78058 are the μPD78054 subseries products of the 78K/0 series. 8-bit resolution D/A converter, timer, serial interface, real-time output port and interrupt functions.

The μPD78P054, a one-time PROM or EPROM product which can be operated in the same supply voltage range as for the mask ROM product, and various development tools are also available.

Details of the function description, etc, are described in the following User's Manual. Be sure to read it when designing.

μPD78054 Subseries User's Manual (Preliminary): IEU-824

FEATURES

- Large on-chip ROM & RAM

Items / Products Name	Program Memory (ROM)	Data Memory		
		Internal High-Speed RAM	Buffer RAM	Internal Expanded RAM
μPD78052	16K bytes	512 bytes	32 bytes	No
μPD78053	24K bytes	1024 bytes		
μPD78054	32K bytes			
μPD78055	40K bytes			★
μPD78056	48K bytes			1024 byte
μPD78058	60K bytes			

- External memory expansion space: 64K bytes
- Instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 69 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- 8-bit resolution D/A converter : 2 channels
- Serial interface : 3 channels
- Timer: 5 channels
- Operating voltage range: 2.0 to 6.0 V ★

APPLICATION

Pocket telephone, pager, printer, AV equipment, airconditioners, cameras, PPC, fuzzy home appliances, vending machine, etc.

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The mark ★ shows major revised points.

★ ORDERING INFORMATION

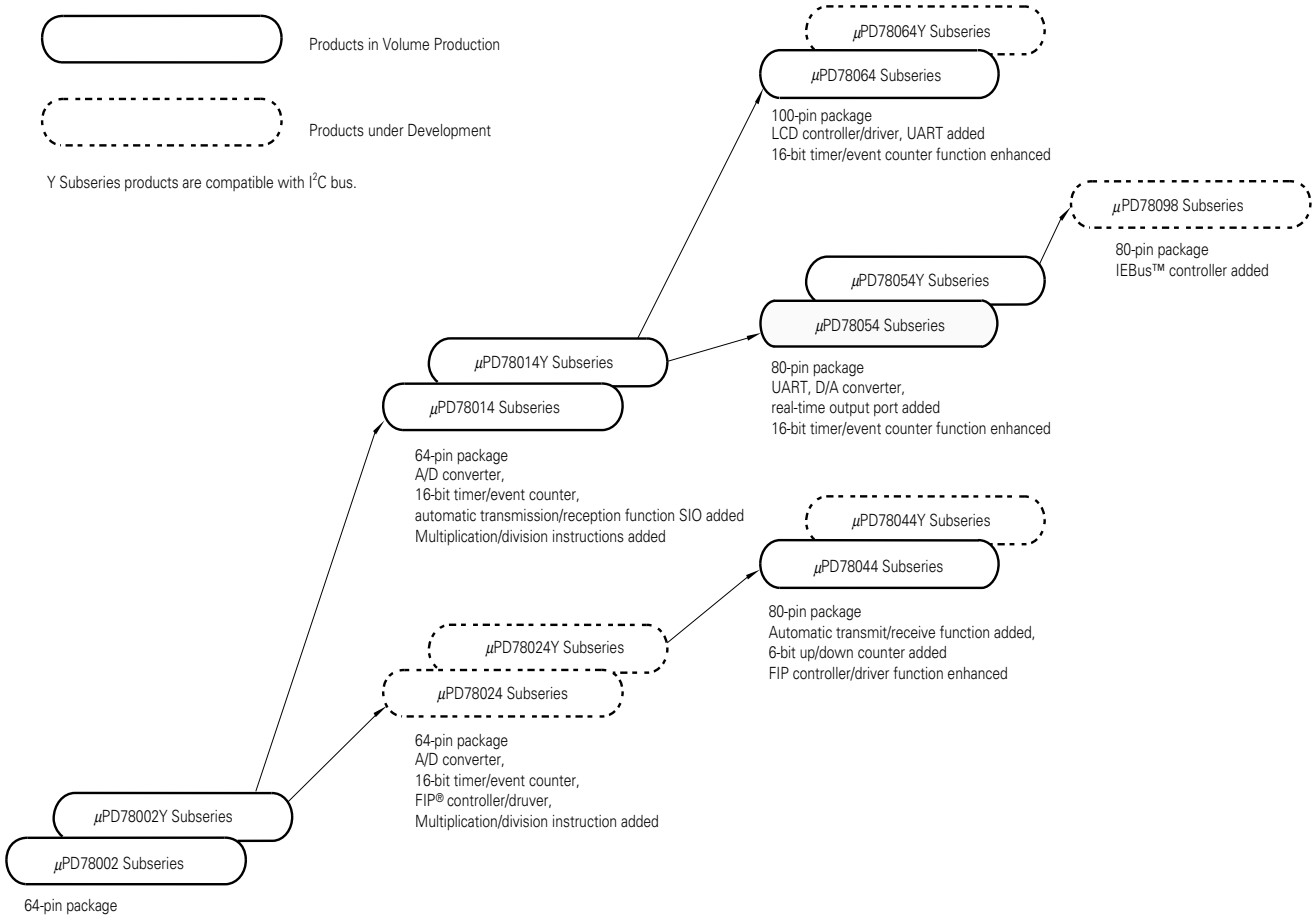
Ordering Code	Package	Quality Grade
μPD78052GC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD78052GK-×××-BE9	80-pin plastic TQFP (fine pitch) (□12 mm)	Standard
μPD78053GC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD78053GK-×××-BE9	80-pin plastic TQFP (fine pitch) (□12 mm)	Standard
μPD78054GC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD78054GK-×××-BE9	80-pin plastic TQFP (fine pitch) (□12 mm)	Standard
μPD78055GC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD78055GK-×××-BE9***1**	80-pin plastic TQFP (fine pitch) (□12 mm)	Standard
μPD78056GC-×××-3B9	80-pin plastic QFP (□14 mm)	Standard
μPD78056GK-×××-BE9***1**	80-pin plastic TQFP (fine pitch) (□12 mm)	Standard
μPD78058GC-×××-3B9***2**	80-pin plastic QFP (□14 mm)	Standard
μPD78058GK-×××-BE9***3**	80-pin plastic TQFP (fine pitch) (□12 mm)	Standard

***** **1.** In planning stage
2. Under development

Remarks ××× denotes the ROM code number.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES DEVELOPMENT



OVERVIEW OF FUNCTION

Item \ Product Name		μPD78052	μPD78053	μPD78054	μPD78055	μPD78056	μPD78058	
Internal memory	ROM	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes	60K bytes	★
	Internal high-speed RAM	512 bytes	1024 bytes					
	Buffer RAM	32 bytes						
	Internal expanded RAM	None					1024K bytes	
Memory space		64 K bytes						
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)						
Instruction cycle		On-chip instruction execution time cycle modification function						
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0 MHz operation)						
	When subsystem clock selected	122 μs (at 32.768 kHz operation)						
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.						
I/O ports		Total : 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O : 4						
A/D converter		• 8-bit resolution × 8 channels						
D/A converter		• 8-bit resolution × 2 channels						
Serial interface		• 3-wire/SBI/2-wire mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel • 3-wire/UART mode selectable: 1 channel						
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel						
Timer output		3 (14-bit PWM output × 1)						
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock 5.0 MHz operation) 32.768 kHz (at subsystem clock 32.768 kHz operation)						
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 5.0 MHz operation)						
Vectored interrupts	Maskable interrupts	Internal interrupt : 13, external interrupt : 7						
	Non-maskable interrupts	Internal interrupt : 1						
	Software interrupts	Internal interrupt : 1						
Test input		Internal : 1, external : 1						
Operating voltage range		V_{DD} = 2.0 to 6.0 V						★
Operating temperature range		– 40 to + 85°C						★
Package		• 80-pin plastic QFP (□14 mm) • 80-pin plastic TQFP (fine pitch) (□12 mm)*						

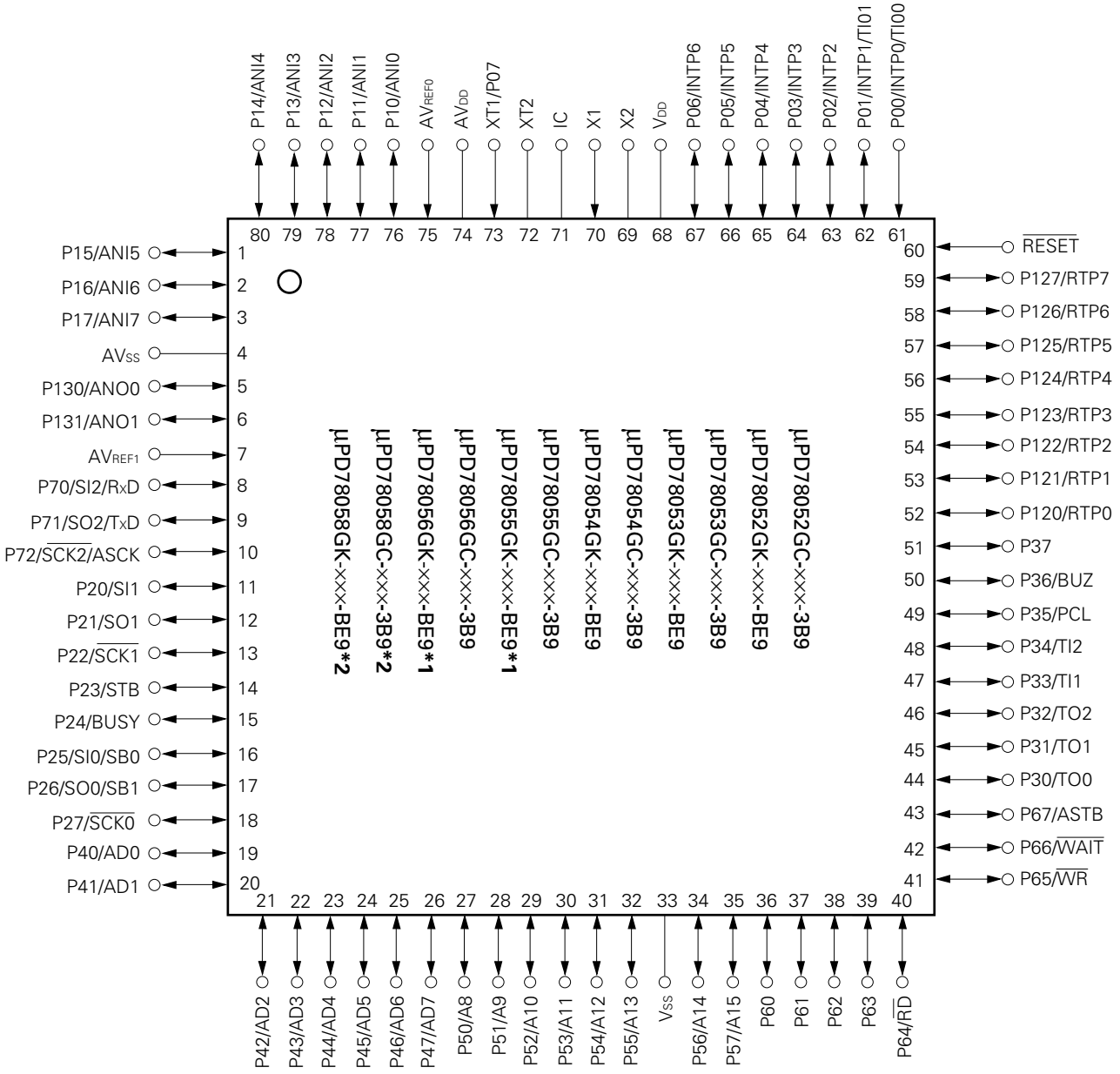
* μPD78055 and 78056 are in planning stage.

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

80-pin plastic QFP (□14 mm)

80-pin plastic TQFP (fine pitch) (□12 mm)



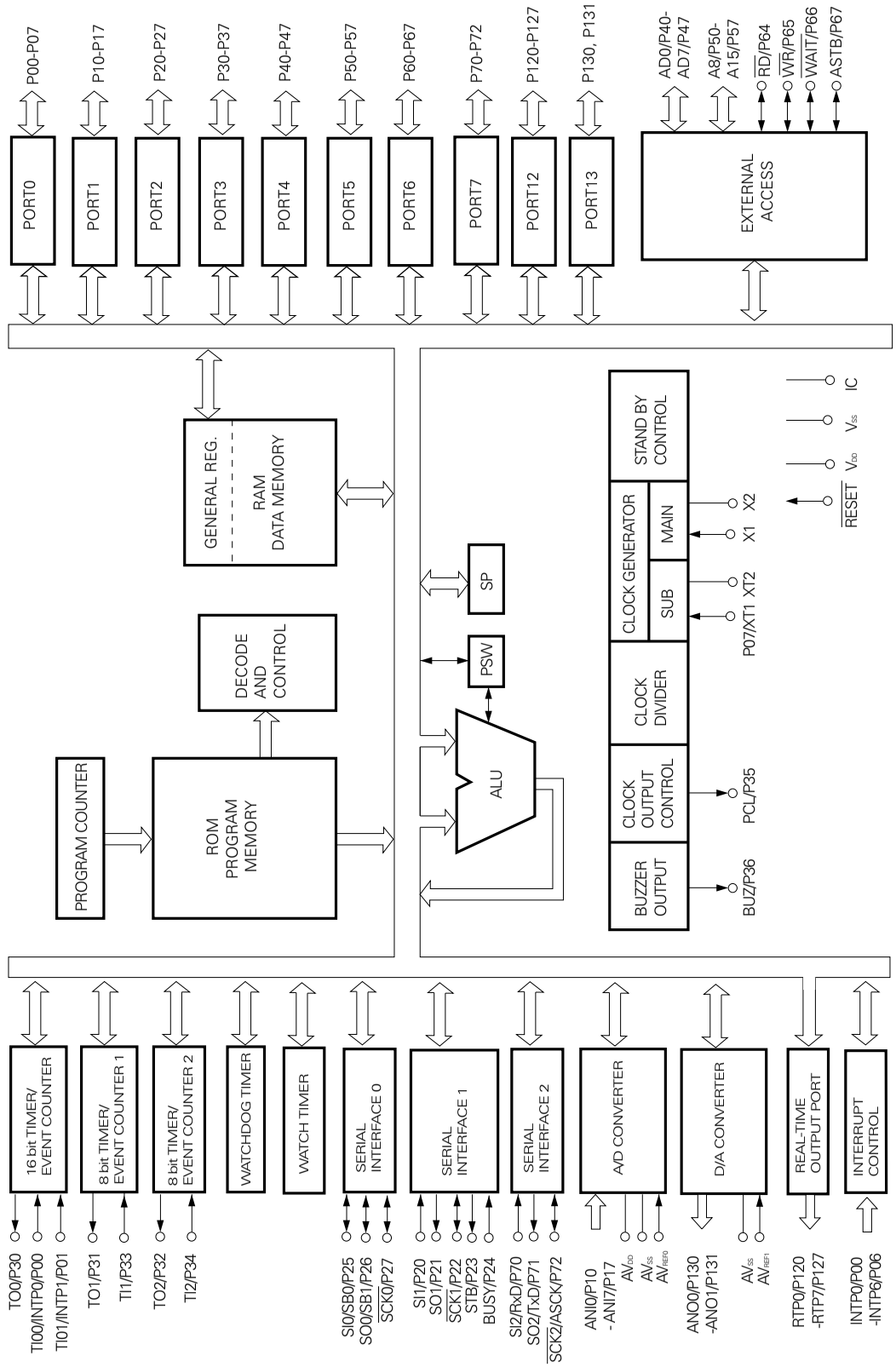
* **1.** In planning stage
2. Under development

Remarks **1.** IC (Internally Connected) should be connected directly to V_{SS}.
2. AV_{DD} pin should be connected to V_{DD} pin.
3. AV_{SS} pin should be connected to V_{SS} pin.

P00 to P07 : Port0
P10 to P17 : Port1
P20 to P27 : Port2
P30 to P37 : Port3
P40 to P47 : Port4
P50 to P57 : Port5
P60 to P67 : Port6
P70 to P72 : Port7
P120 to P127 : Port12
P130, P131 : Port13
RTP0 to RTP7 : Real-Time Output Port
INTP0 to INTP6 : Interrupt From Peripherals
TI00, TI01 : Timer Input
TI1, TI2 : Timer Input
TO0 to TO2 : Timer Output
SB0, SB1 : Serial Bus
SI0 to SI2 : Serial Input
SO0 to SO2 : Serial Output
$\overline{SCK0}$ to $\overline{SCK2}$: Serial Clock
RxD : Receive Data
TxD : Transmit Data
ASCK : Asynchronous Serial Clock

PCL : Programmable Clock
BUZ : Buzzer Clock
STB : Strobe
BUSY : Busy
AD0 to AD7 : Address/Data Bus
A8 to A15 : Address Bus
$\overline{RD}$: Read Strobe
$\overline{WR}$: Write Strobe
$\overline{WAIT}$: Wait
ASTB : Address Strobe
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)
$\overline{RESET}$: Reset
ANI0 to ANI7 : Analog Input
ANO0, ANO1 : Analog Output
AV_{DD} : Analog Power Supply
AV_{SS} : Analog Ground
$AV_{REF0,1}$: Analog Reference Voltage
V_{DD} : Power Supply
V_{SS} : Ground
IC : Internally Connected

2. BLOCK DIAGRAM



Note The internal ROM & RAM capacity depends on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 8-bit I/O port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07*1	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.*2		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be connected by software. Test flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

* **1.** When using the P07/XT1 pins as an input port, set 1 in the bit 6 (FRC) of the processor clock control register. On-chip feedback resistor of the subsystem clock oscillator should not be used.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, use of the pull-up resistor is cancelled automatically.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/outport port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	———
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be connected by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120 to P127	Input/output	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be connected by software.		Input	ANO0, ANO1

3.2 OTHER PINS (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input /output	Serial interface serial clock input/ output	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1)		P33
TI2		External count clock input to the 8-bit timer (TM2)		P34
TO0	Output	16-bit timer output (dual-function as 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120 to P127
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65

3.2 OTHER PINS (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input.	——	—
AV_{REF1}	Input	D/A converter reference voltage input.	——	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}	——	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}	——	—
$\overline{RESET}$	Input	System reset input.	——	—
X1	Input	Main system clock oscillation crystal connection.	——	—
X2	—		——	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		——	—
V_{DD}	—	Positive power supply.	——	—
V_{SS}	—	Ground potential.	——	—
IC	—	Internal connection. Connect to V_{SS} directly.	——	—

3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, see Fig. 3-1.

Table 3-1 Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P00/INTP0/TI00	2	Input	Connected to Vss.
P01/INTP1/TI01	8-A	Input/output	Input : Connected to Vss. Output : Leave open.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connected to Vss.
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P20/SI1	8-A	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P21/SO1	5-A		
P22/$\overline{\text{SCK1}}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{\text{SCK0}}$			
P30/TO0	5-A	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/output	Input : Connected to Vss. Output : Leave open.
P50/A8 to P57/A15	5-A	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P60 to P63	13-B		
P64/$\overline{\text{RD}}$	5-A		
P65/$\overline{\text{WR}}$			
P66/$\overline{\text{WAIT}}$			
P67/ASTB			

Table 3-1 Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P70/SI2/RxD	8-A	Input/ output	Input : Connected to V_{DD} or V_{SS} . Output : Leave open.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0 to P127/RTP7	5-A	Input/ output	Input : Connected to V_{DD} or V_{SS} . Output : Leave open.
P130/ANO0 , P131/ANO1	12-A	Input/ output	Input : Connected to V_{DD} or V_{SS} . Output : Leave open.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connected to V_{SS} .
AV_{REF1}			Connected to V_{DD} .
AV_{DD}			
AV_{SS}			Connected to V_{SS} .
IC			Connected to V_{SS} directly.

Fig. 3-1 Pin Input/Output Circuits (1/2)

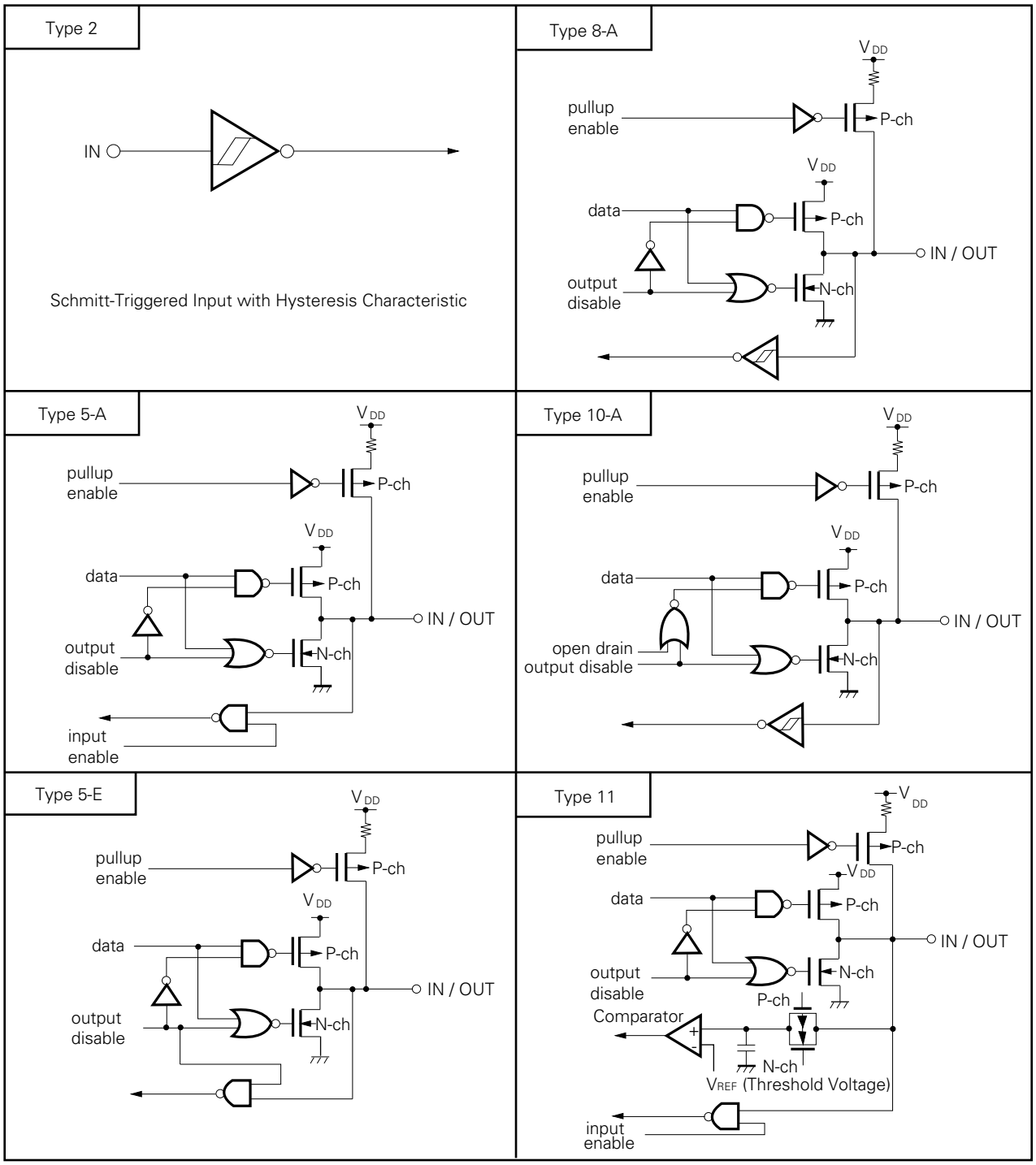
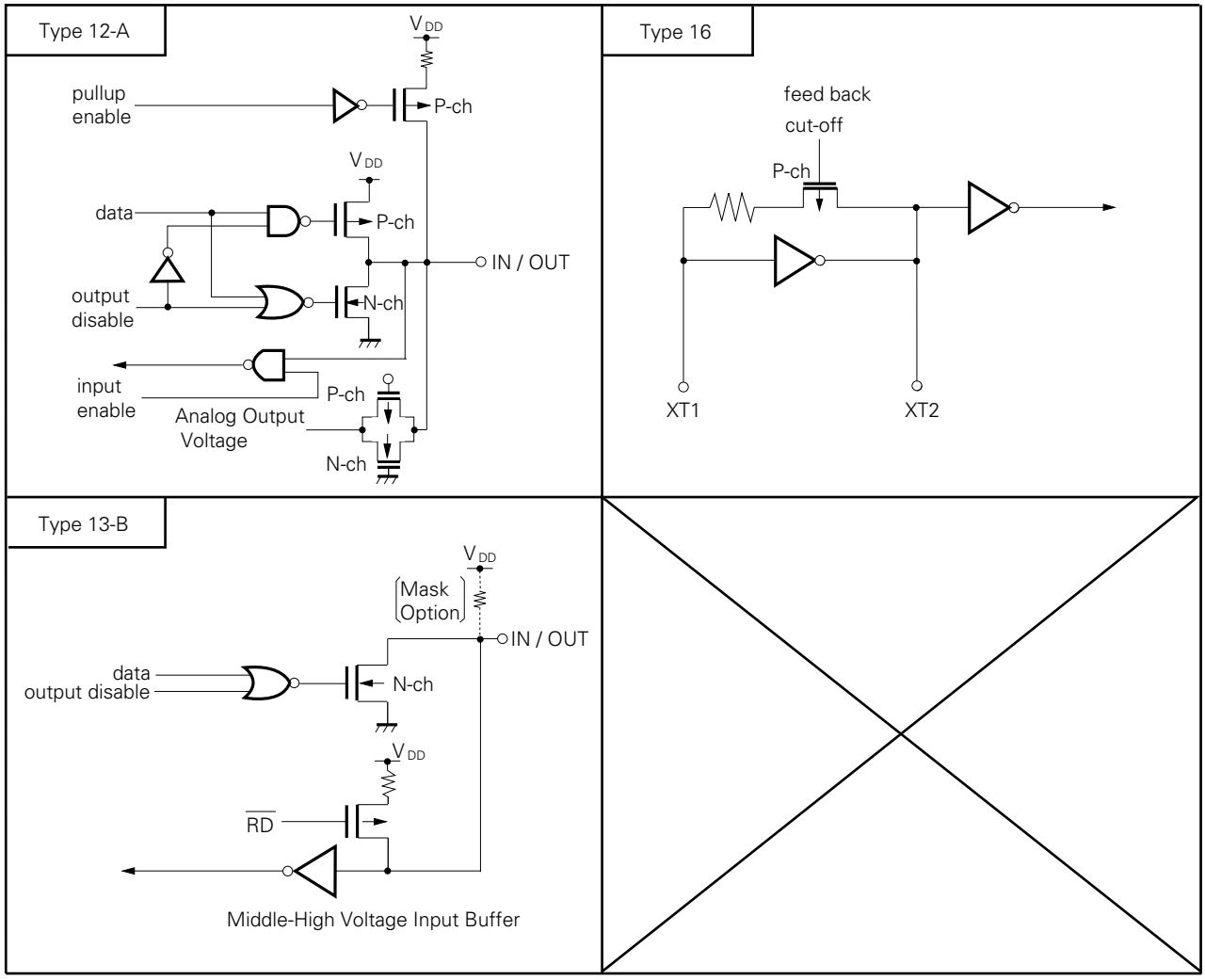


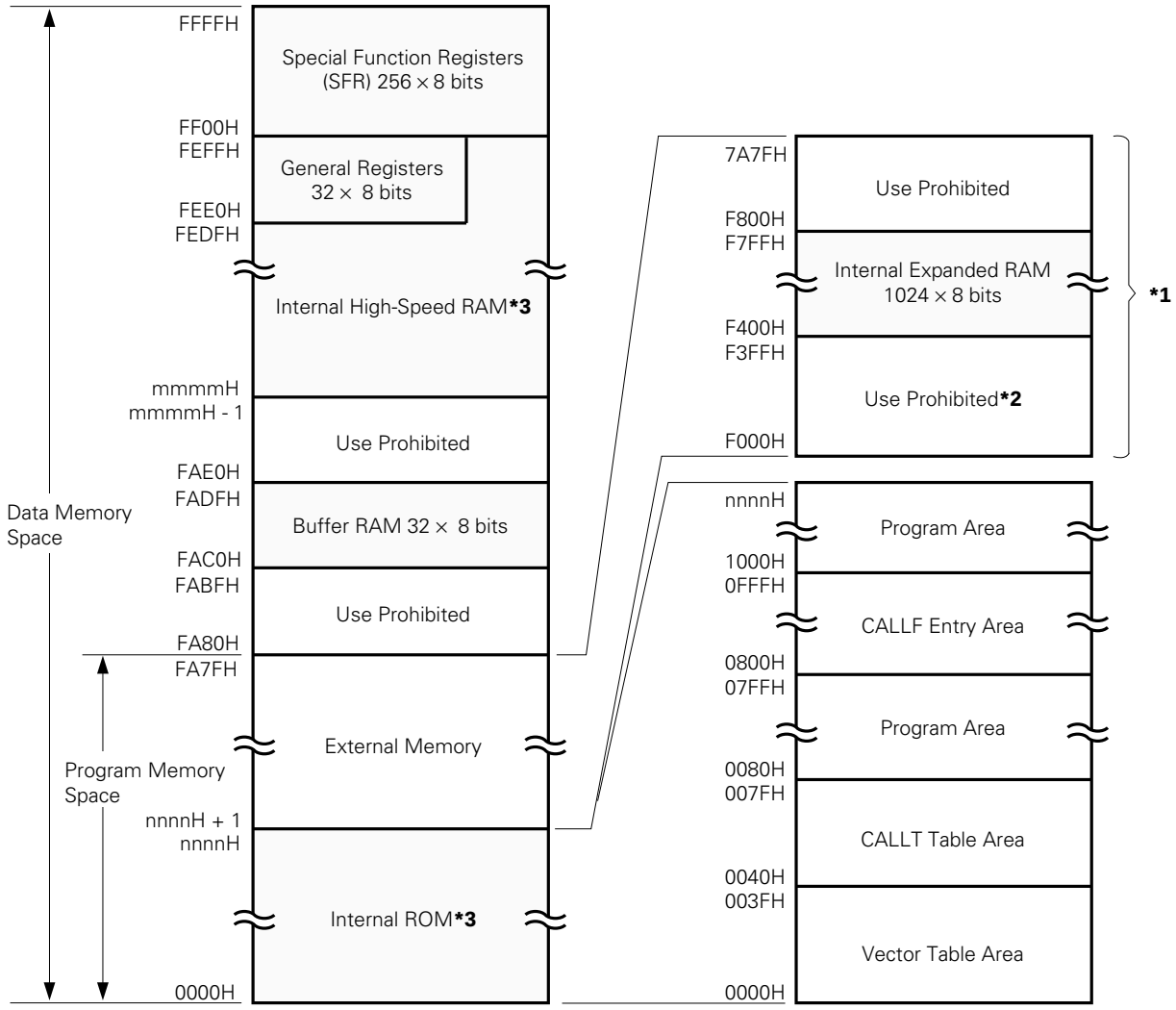
Fig. 3-1 Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the μPD78052/78053/78054/78055/78056/78058 memory map.

Fig. 4-1 Memory Map



Remarks Shaded area indicates internal memory.

*** 1.** μPD78058 only

2. When the external device expansion function is used with the μPD78058, set the internal ROM capacity to 56K bytes using the memory size switching register.

3. The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the table below).

Relevant Product Name	Internal ROM Last Address nnnnH	Internal RAM First Address mmmmH
μPD78052	3FFFH	FD00H
μPD78053	5FFFH	FB00H
μPD78054	7FFFH	
μPD78055	9FFFH	
μPD78056	BFFFH	
μPD78058	EFFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The following 3 types of I/O ports are available.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 7, port 12, port 13) : 63
- N-channel open-drain input/output (P60 to P63) : 4

Total : 69

Table 5-1 Port Functions

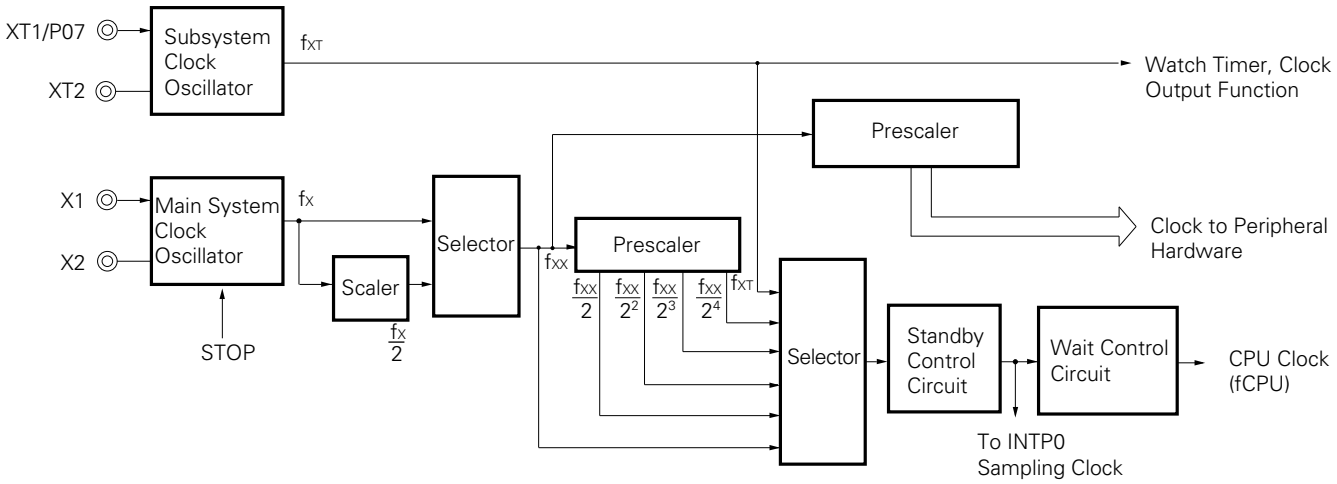
Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port pins
	P01 to P06	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable in 8-bit units. When used as input port pins, on-chip pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. LED direct drive capability.
Port 6	P60 to P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be used by mask option. LED direct drive capability.
	P64 to P67	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 7	P70 to P72	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 12	P120 to P127	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.
Port 13	P130, P131	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software.

5.2 CLOCK GENERATOR

Two types of generators, a main system clock generator and a subsystem clock generator, are avaibable.
The instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: at 5.0 MHz operation)
- 122 μs (subsystem clock: at 32.768 kHz operation)

Fig. 5-1 Clock Generator Block Diagram ★



5.3 TIMER/EVENT COUNTER

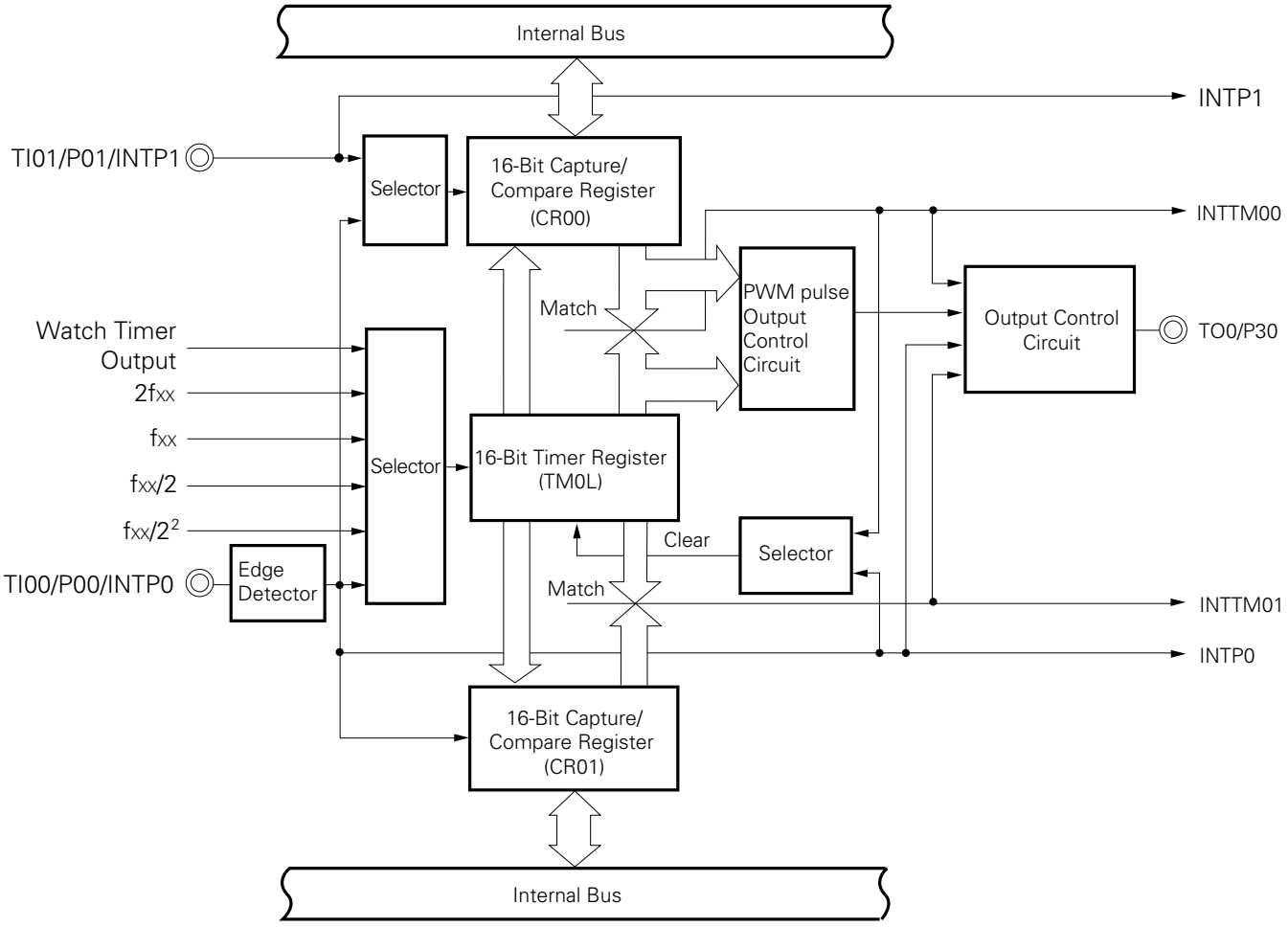
The μPD78052/78053/78054/78055/78056/78058 incorporate 5 channels of the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channel
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2 Types and Functions of Timer/Event Counter

	16-Bit Timer/Event Counter	8-Bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type				
Interval timer	1 channel	2 channels	1 channel	1 channel
External event counter	1 channel	2 channels	——	——
Function				
Timer output	1 output	2 outputs	——	——
PWM output	1 output	——	——	——
Pulse ampitude measurement	1 input	——	——	——
Square wave output	1 output	2 outputs	——	——
Ono-shot pulse output	1 output	——	——	——
Interrupt request	2	2	2	1

★ **Fig. 5-2 16-Bit Timer/Event Counter Block Diagram**



★ **Fig. 5-3 8-Bit Timer/Event Counter Block Diagram**

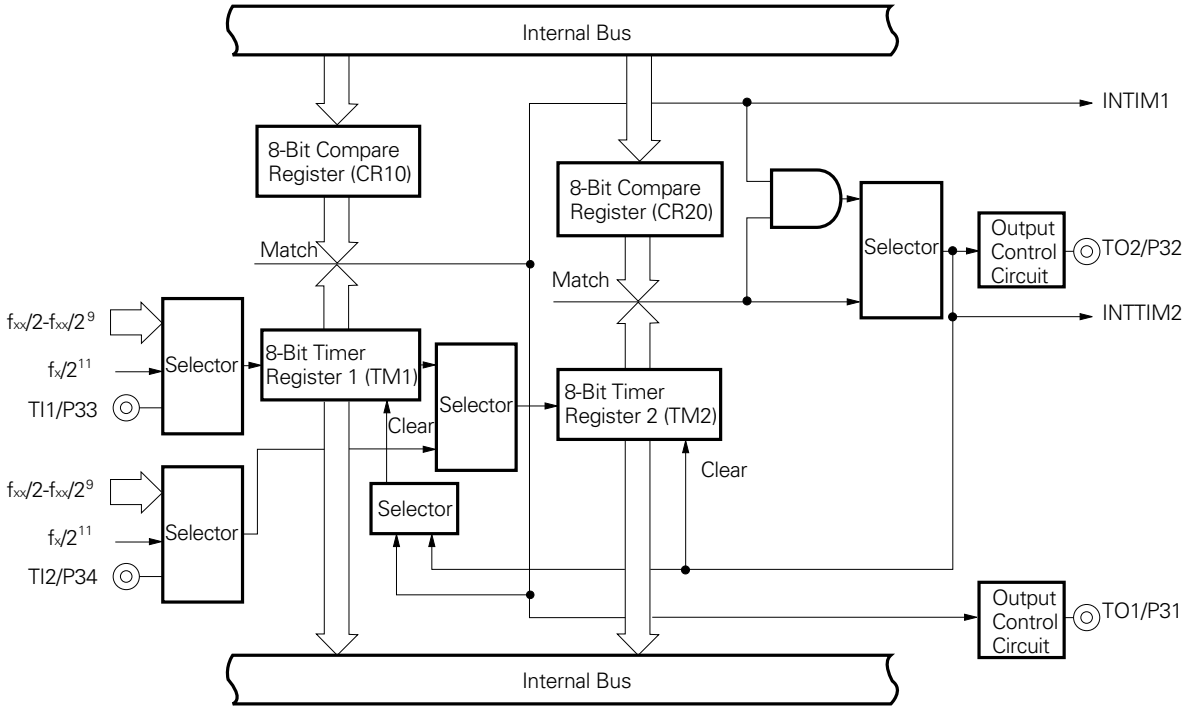


Fig. 5-4 Watch Timer Block Diagram ★

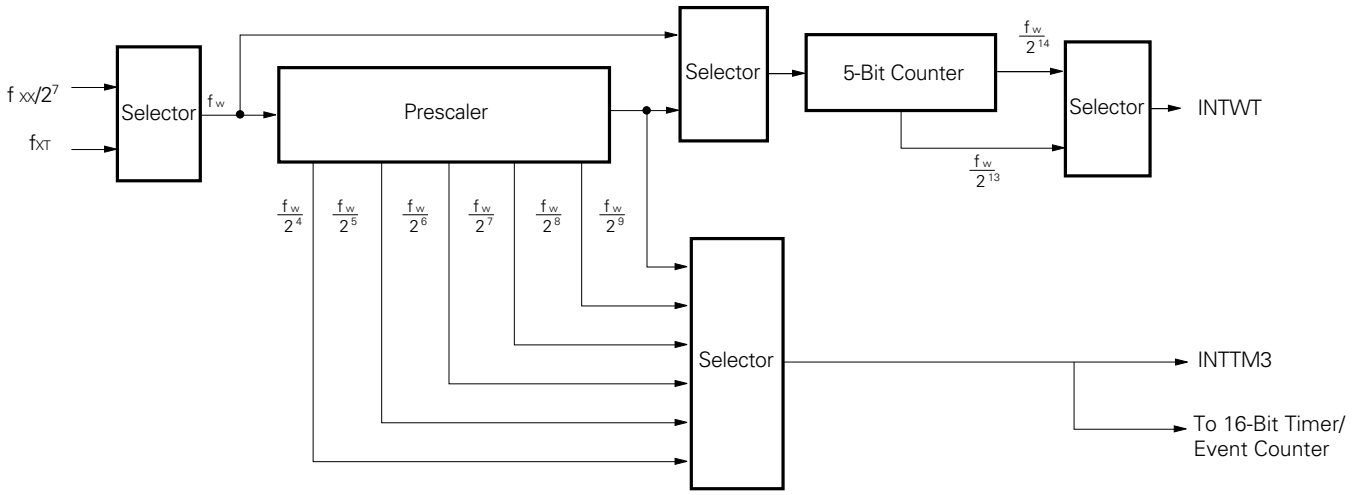
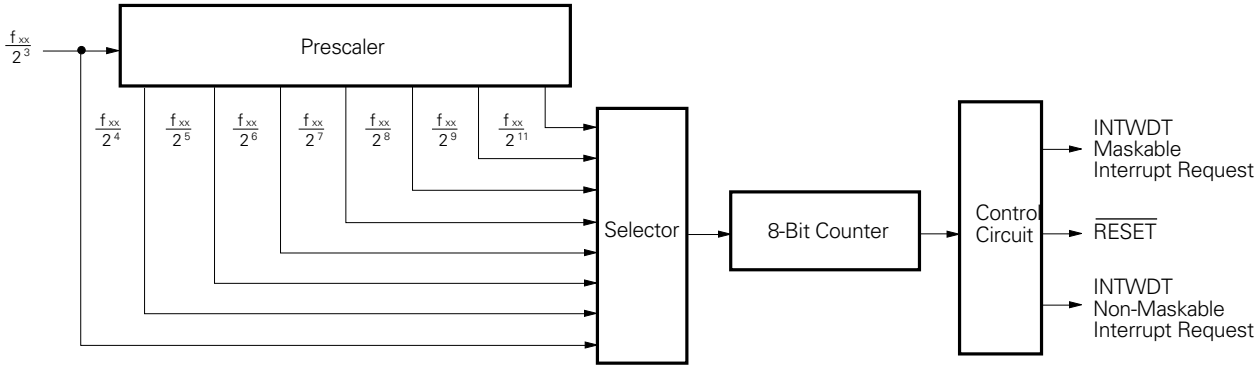


Fig. 5-5 Watchdog Timer Block Diagram ★

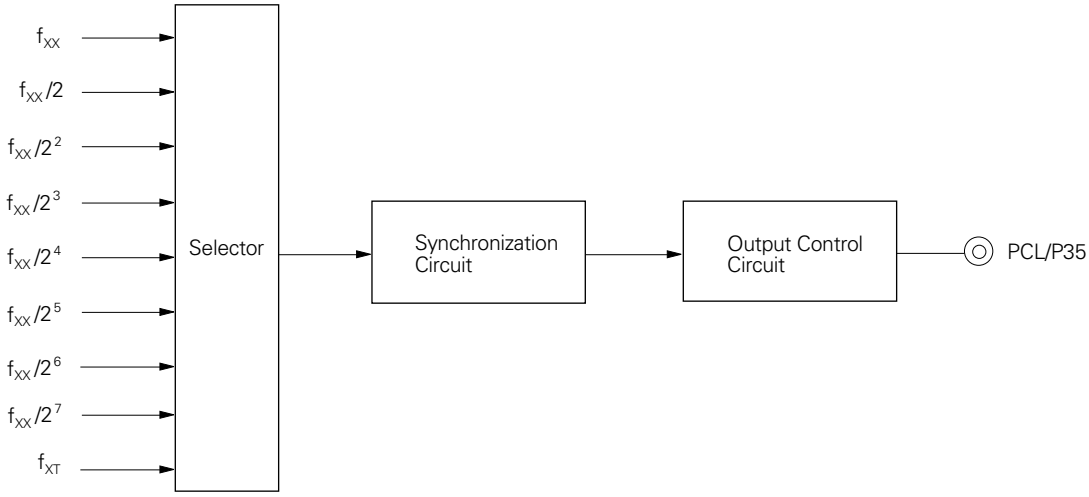


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: at 5.0 MHz operation)
- 32.768 kHz (subsystem clock: at 32.768 kHz operation)

★ **Fig. 5-6 Clock Output Control Circuit Configuration**

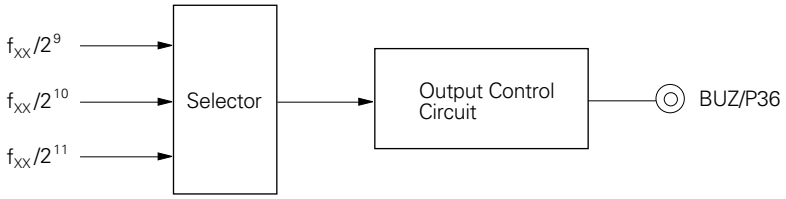


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock: at 5.0 MHz operation)

★ **Fig. 5-7 Buzzer Output Control Circuit Block Diagram**



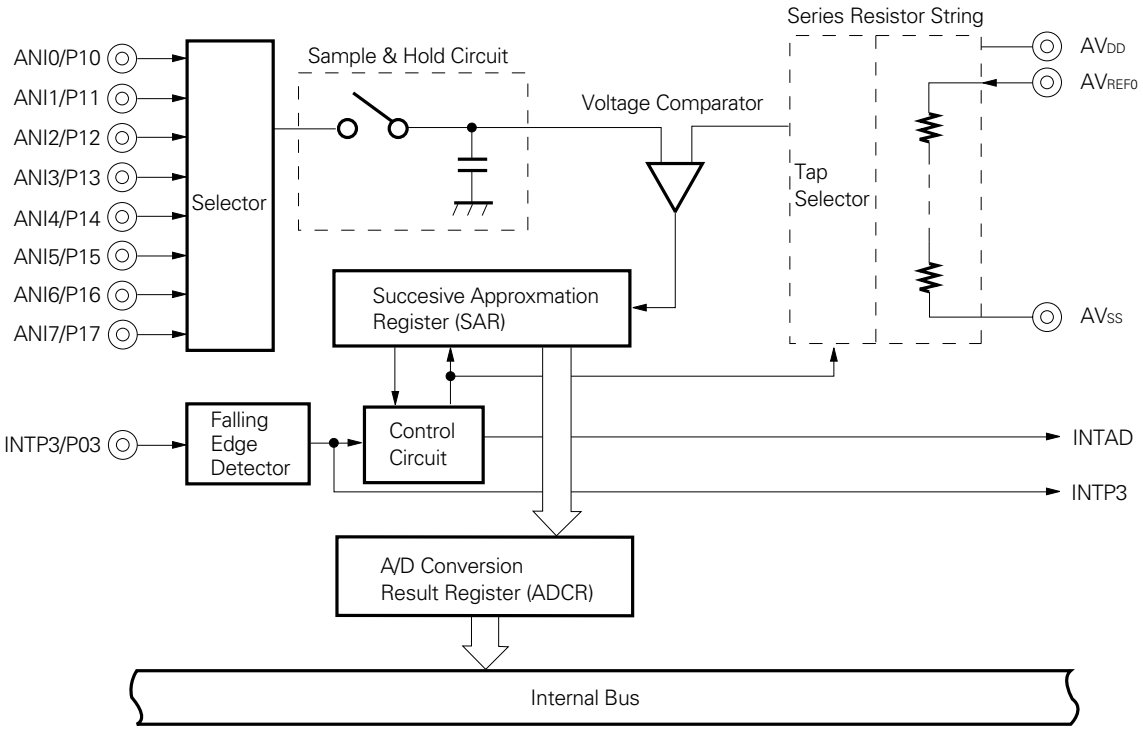
5.6 A/D CONVERTER

An A/D converter of 8-bit resolution × 8 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Fig. 5-8 A/D Converter Block Diagram ★

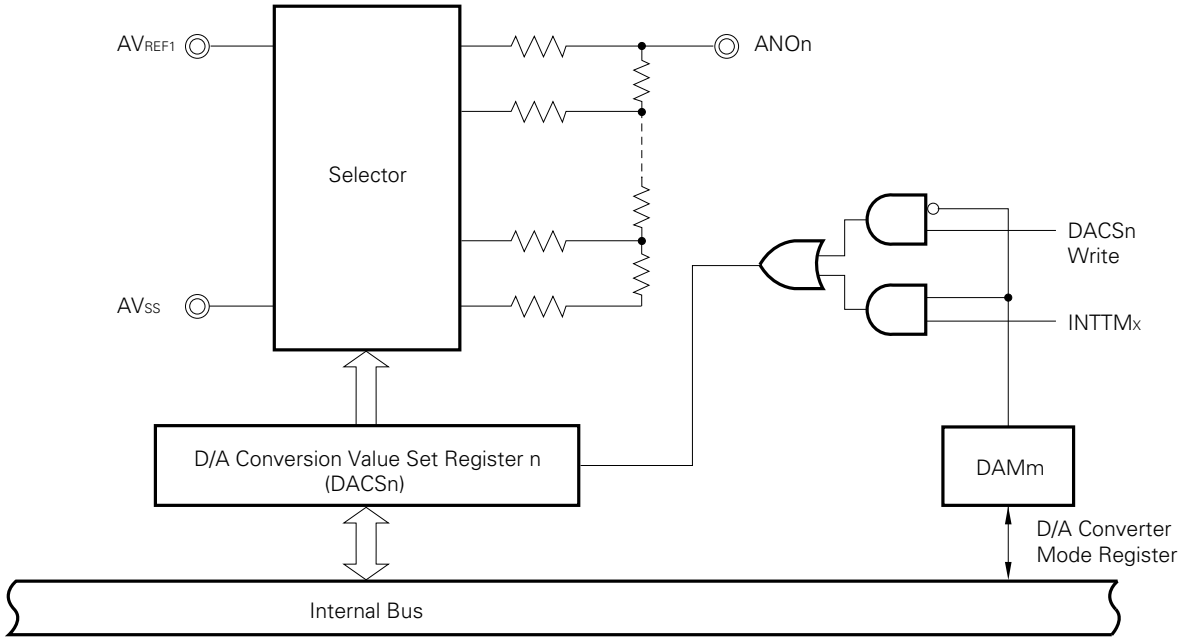


5.7 D/A CONVERTER

A D/A converter of 8-bit resolution × 2 channels is available.

Conversion method is R-2R resistor ladder method.

★ **Fig. 5-9 D/A Converter Block Diagram**



Remarks **1.** n = 0, 1
2. m = 4, 5
3. x = 1, 2

5.8 SERIAL INTERFACES

3 channels of the clocked serial interface are incorporated.

- Serifal interface channel 0
- Serifal interface channel 1
- Serifal interface channel 2

★ **Table 5-3 Types and Functions of Serial Interface**

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-Wired serial I/O mode	○(MSB/LSB first switchable)	○(MSB/LSB first switchable)	○(MSB/LSB first switchable)
3-Wired serial I/O mode with automatic transmission/reception function	———	○(MSB/LSB first switchable)	———
SBI (serial bus interface) mode	○ (MSB first)	———	———
2-wired serial I/O mode	○ (MSB first)	———	———
Asynchronous serial interface (UART) mode	———	———	○(Dedicated baud rate generator incorporated)

Fig. 5-10 Serial Interface Channel 0 Block Diagram ★

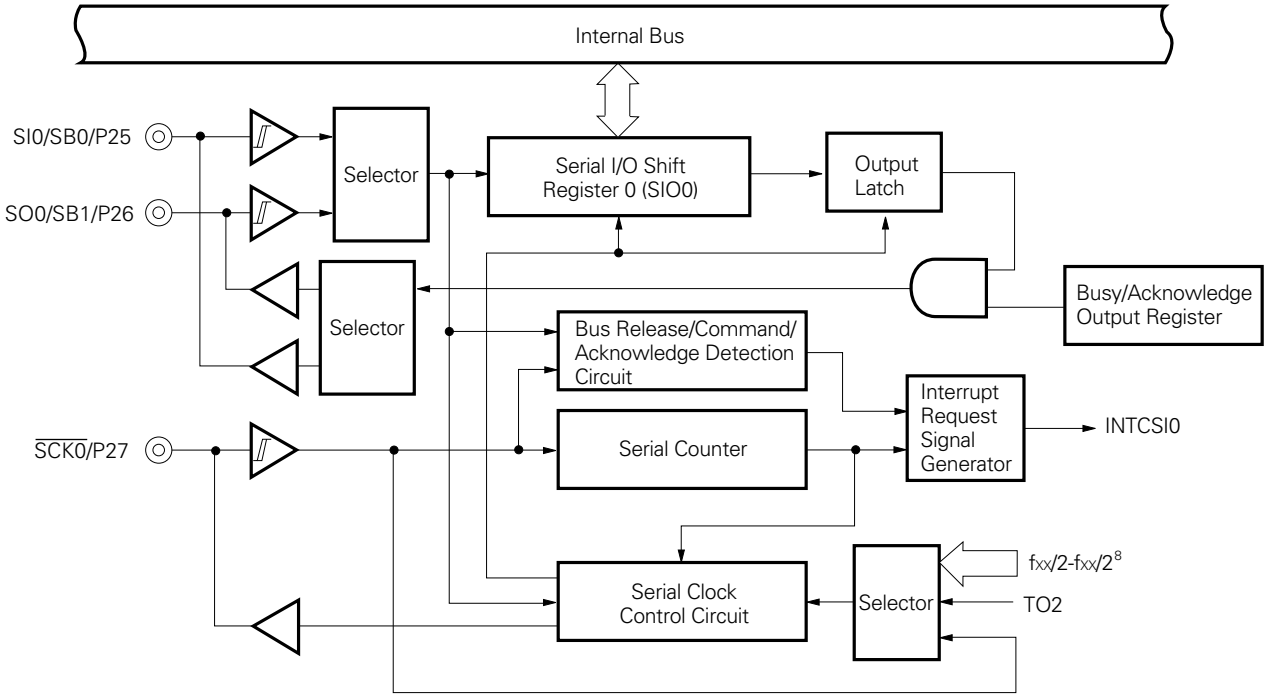
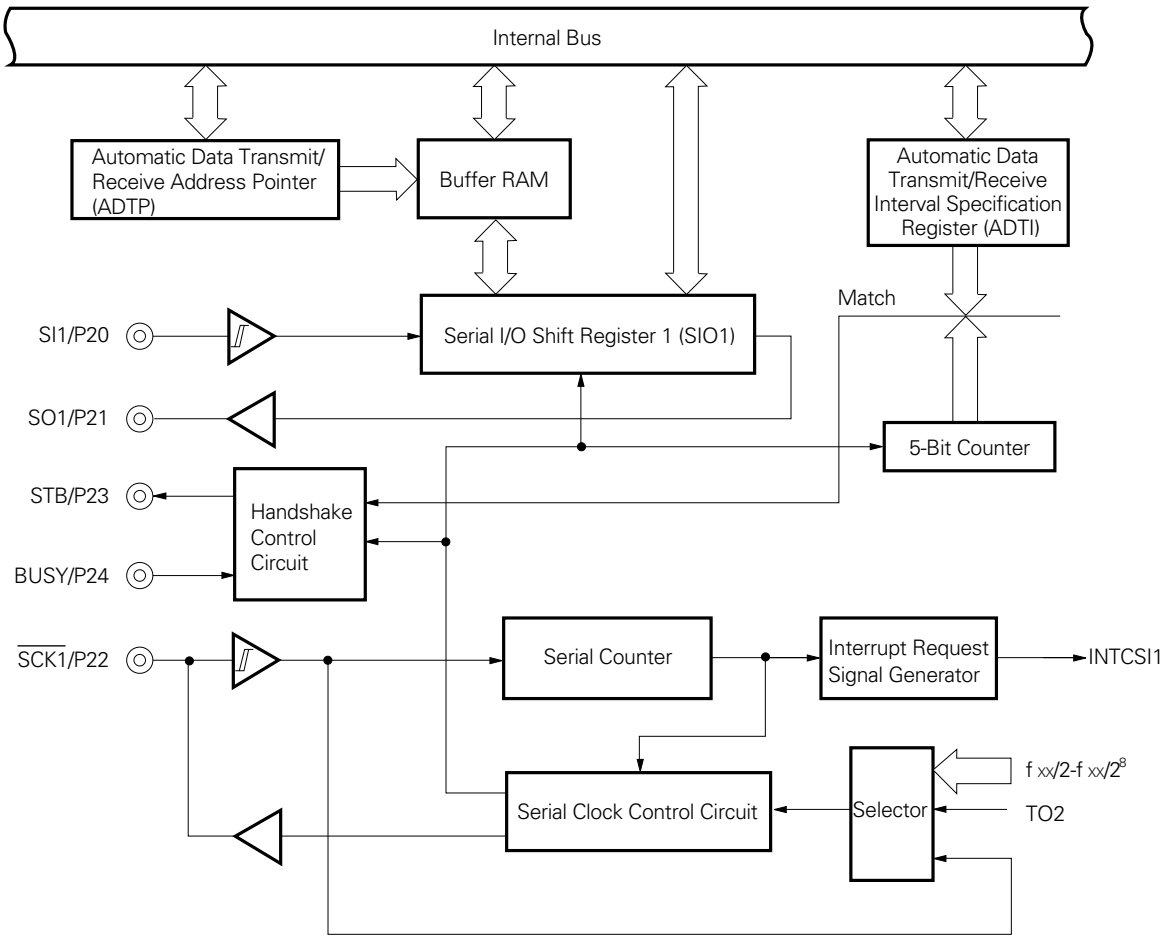
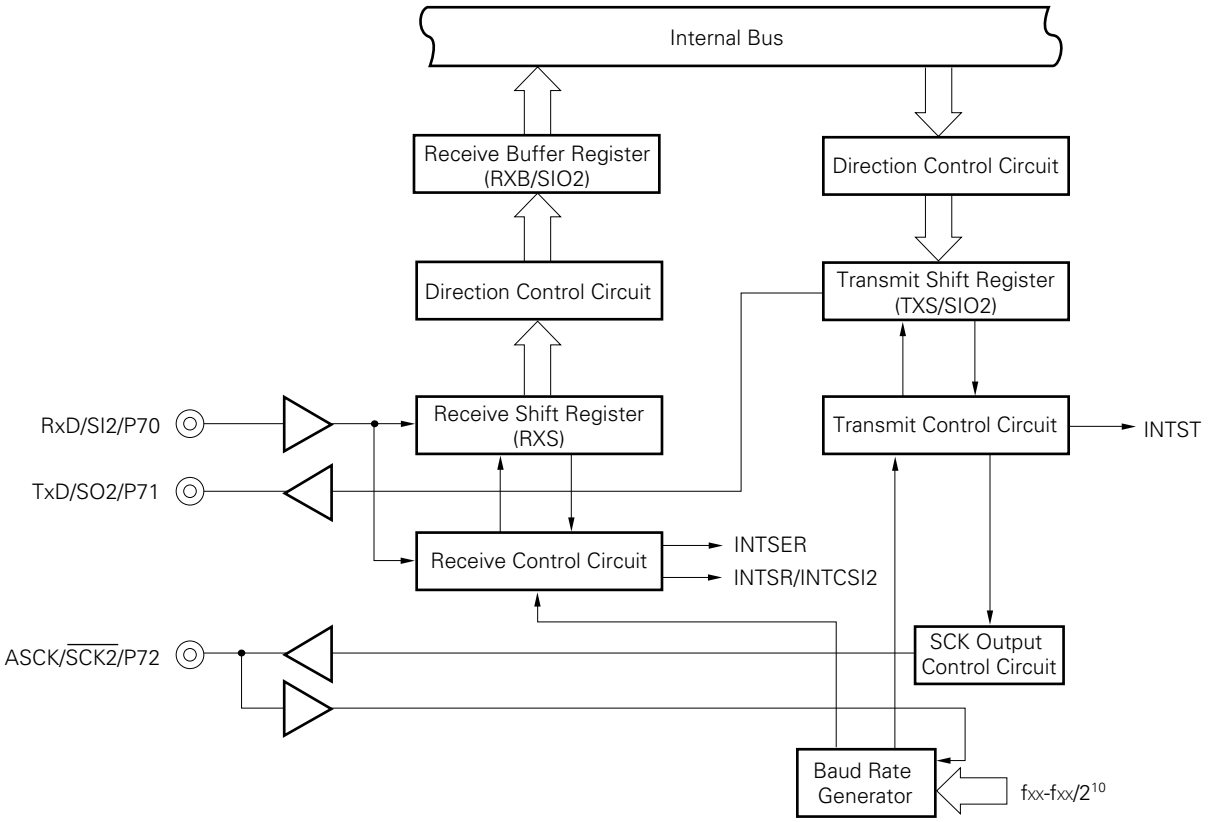


Fig. 5-11 Serial Interface Channel 1 Block Diagram ★



★ **Fig. 5-12 Serial Interface Channel 2 Block Diagram**

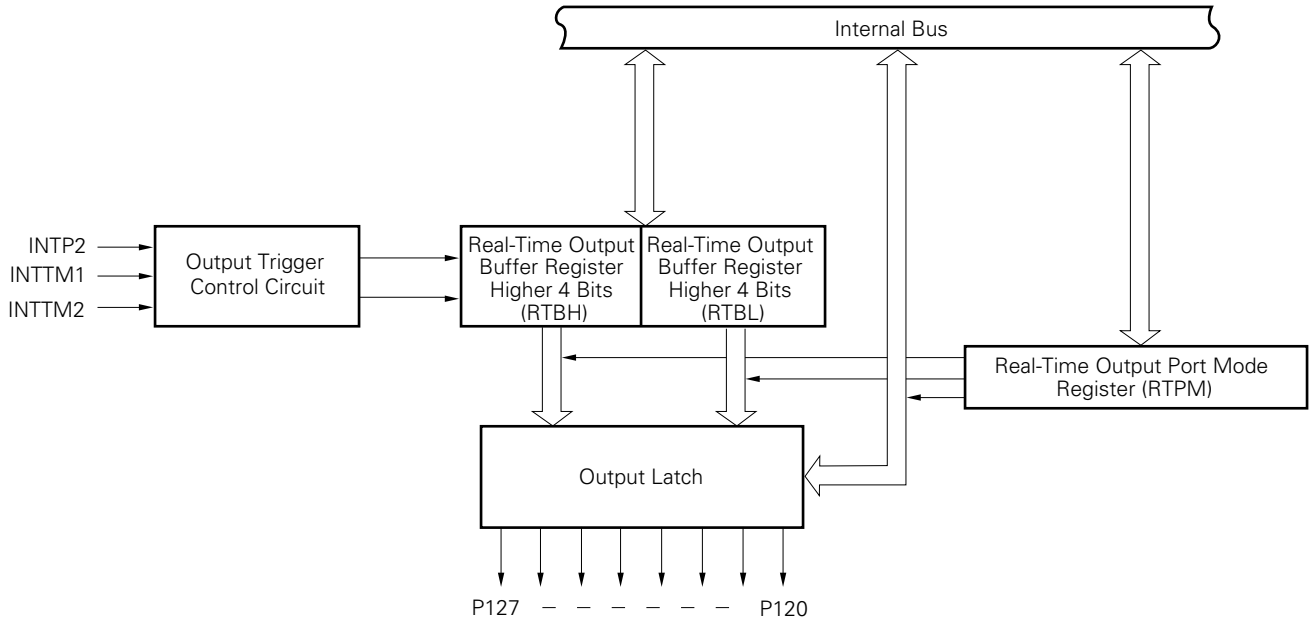


5.9 Real-Time Output Port Functions

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt and external interrupt generation in order to output to off-chip. This is real-time output function. And pins to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motor, etc.

★ **Fig. 5-13 Real-Time Output Port Block Diagram**



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are 22 interrupt functions of three different kinds, as shown below.

- Non-maskable interrupt: 1
- Maskable interrupt: 20
- Software interrupt: 1

Table 6-1 Interrupt Source List (1/2)

Interrupt Type	Default Priority*1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type*2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	A
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			B
	1	INTP0	Pin input edge detection	External	0006H	C
	2	INTP1			0008H	D
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H	B
	9	INTCSI1	End of serial interface channel 1 transfer		0016H	
	10	INTSER	Generation of serial interface channel 2 UART receive error		0018H	
	11	INTSR	End of serial interface channel 2 UART reception		001AH	
		INTCSI2	End of serial interface channel 2 3-wire transfer			
	12	INTS	End of serial interface channel 2 UART transmission		001CH	

* **1.** The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.

2. Basic configuration types A to E correspond to A to E in Fig. 6-1, respectively.

Table 6-1 Interrupt Source List (2/2)

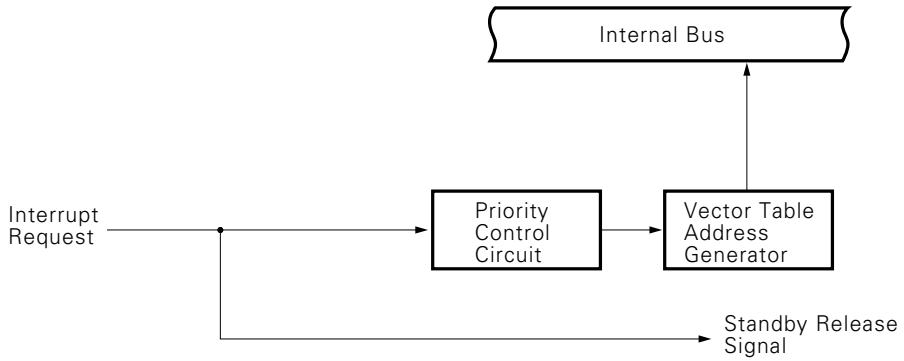
Interrupt Type	Default Priority*1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type*2
		Name	Trigger			
Maskable	13	INTTM3	Reference time interval signal from watch timer	Internal	001EH	B
	14	INTTM00	Generation of match signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of match signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of match signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of match signal of 8-bit timer/event counter 2		0026H	
	18	INTAD	End of conversion by A/D converter		0028H	
Software	—	BRK	BRK instruction execution	Internal	003EH	E

* **1.** The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.

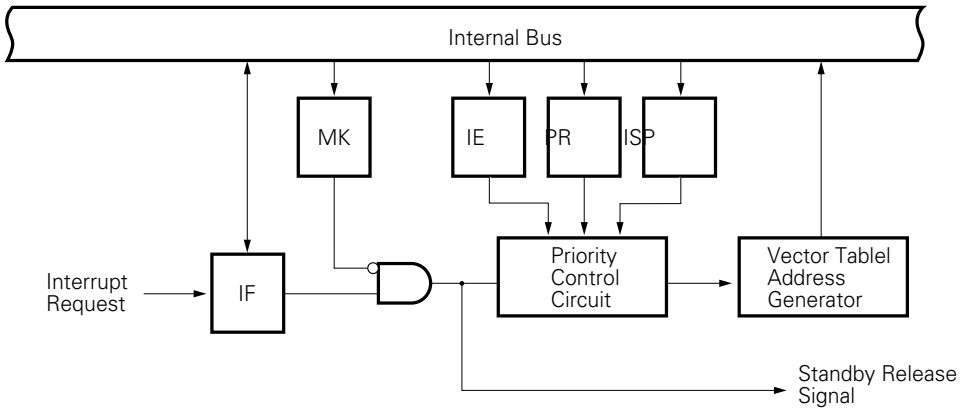
2. Basic configuration types A to E correspond to A to E in Fig. 6-1, respectively.

Fig. 6-1 Interrupt Function Basic Configuration(1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

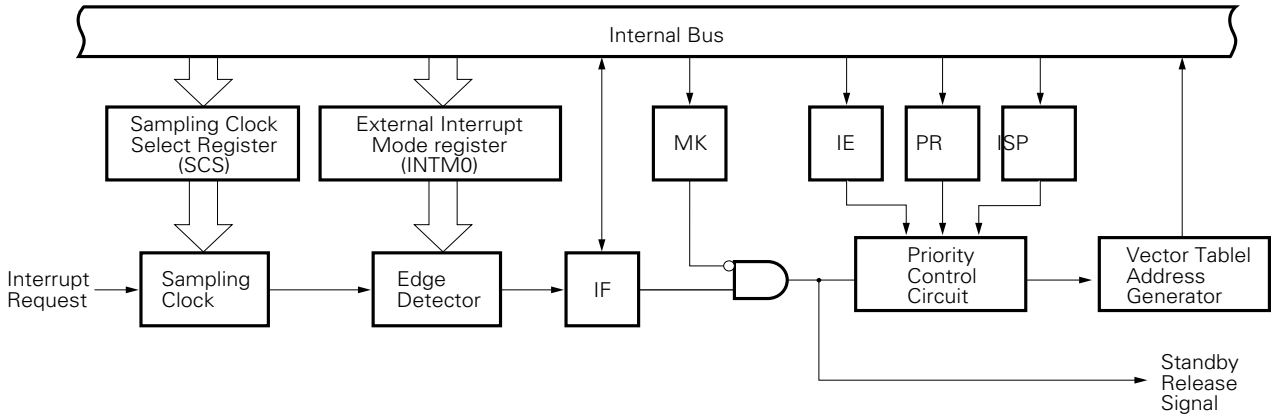
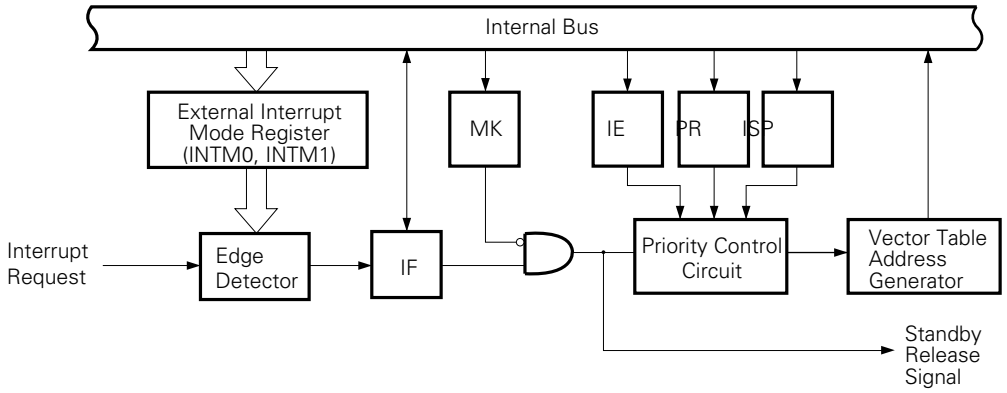
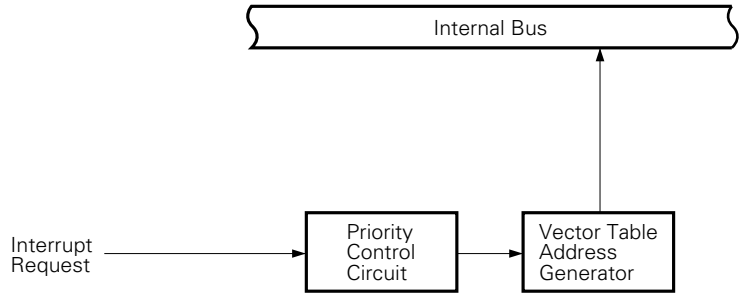


Fig. 6-1 Interrupt Function Basic Configuration(2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



Remarks
1. IF : Interrupt request flag
2. IE : Interrupt enable flag
3. ISP : In-service priority flag
4. MK : Interrupt mask flag
5. PR : Priority specification flag

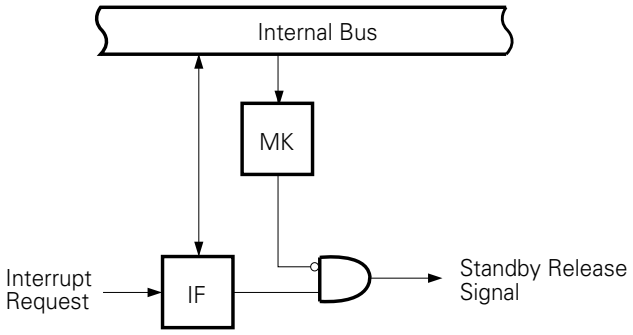
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2 Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Fig. 6-2 Test Function Basic Configuration



Remarks 1. IF : Test input flag
2. MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

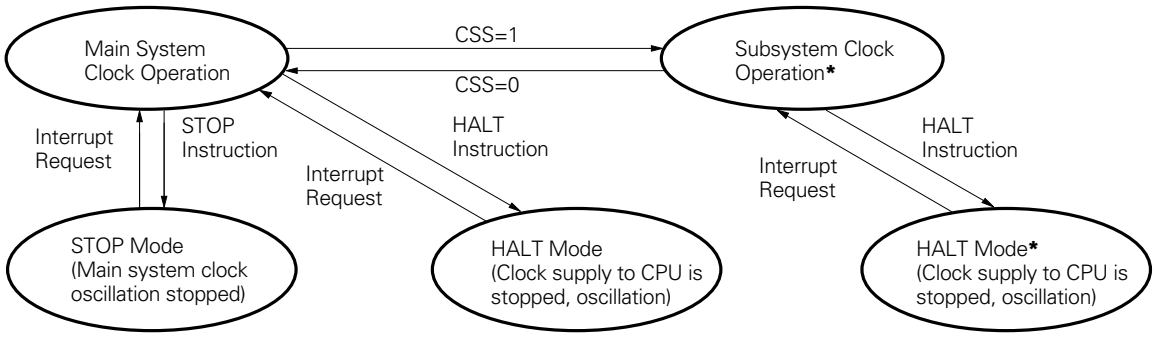
The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

★ 8. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operating clock is stopped.
  The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates withultra-low power consumption using only the subsystem clock.

Fig 8-1 Stand-by Function



* The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

Note When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by RESET pin
- Internal reset by watchdog time runaway time detection

10. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First Operand \ Second Operand	#byte	A	r *	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + Byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL	RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + Byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

* Except r = A

(2) 16-bit instruction

MOV, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second instruction / First instruction	#word	AX	rp*	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW*						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

* Only when rp = BC, DE or HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second instruction / First instruction	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second instruction / First instruction	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 11. ELECTRICAL SPECIFICATIONS *1

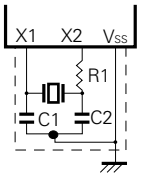
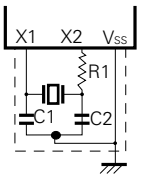
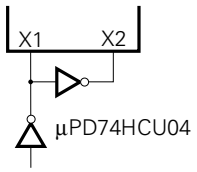
ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to + 7.0	V
	AV_{DD}			–0.3 to VDD + 0.3	V
	AV_{REF0}			–0.3 to VDD + 0.3	V
	AV_{REF1}			–0.3 to VDD + 0.3	V
	AV_{SS}			–0.3 to + 0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17,P20 to P27, P30 toP37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130 P131, X1, X2, XT2 $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch Open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to VDD + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} –0.3 to AV_{REF0} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		P01 to P06, P30-P37, P56, P57, P60 to P67, P120 to P127 total		–15	mA
		P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131 total		–15	mA
Output current low	I_{OL}**2	1 pin	Peak value	30	mA
			Effective value	15	mA
		P50 to P55 total	Peak value	100	mA
			Effective value	70	mA
		P56, P57, P60 to P63 total	Peak value	100	mA
			Effective value	70	mA
		P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131 total	Peak value	50	mA
			Effective value	20	mA
		P01 to P06, P30 to P37, P64 to P67, P120 to P127 total	Peak value	50	mA
			Effective value	20	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

* **1.** Electrical specifications for μPD78052, 78053, 78054, 78055, 78056 (target spec. for μPD78058).
2. Effective value should be calculated as follows: [Effective value] = [Peak value] × "$\overline{\text{duty}}$

Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (Ta = –40 to 85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) ***1**	V_{DD} = Oscillator voltage range	1.0		5.0	MHz
		Oscillation stabilization time ***2**	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (fx) ***1**		1.0		5.0	MHz
		Oscillation stabilization time ***2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (fx) ***1**		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		85		500	ns

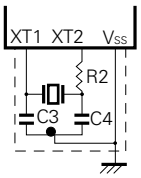
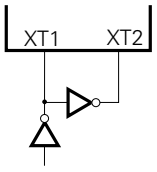
* **1.** Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.
2. Time required to stabilize oscillation after reset or STOP mode release.

Note 1. When using the main system clock oscillator, wirinin the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

SUBSYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (fXT) ***1**		32	32.768	35	kHz
		Oscillation stabilization time ***2**	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (fXT) ***1**		32		100	kHz
		XT1 input high/low level width (tXTH , tXTL)		5		15	μs

* **1.** Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.
2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Note 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level,more prone to misoperation due to noise than the main system clock.

RECOMMENDED OSCILLATION CIRCUIT CONSTANT

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (Ta = –40 to +85 °C)

Manufacture	Product Name	FREQUENCY (MHZ)	Recommended Circuit Constant			Oscillator Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSA5.00MG	5.00	30	30	0	2.0	6.0	
	CST5.00MGW	5.00	On chip	On chip	0	2.0	6.0	Capacitor on chip
Kyocera	KBR-5.0MSA	5.00	33	33	0	2.0	6.0	Lead type
	KBR-5.0MKS	5.00	On chip	On chip	0	2.0	6.0	Capacitor on chip, lead type
	KBR-5.0MWS	5.00	On chip	On chip	0	2.0	6.0	Capacitor on chip, lead type
	PBRC 5.00A	5.00	33	33	0	2.0	6.0	Chip type

MAIN SYSTEM CLOCK: CRISTAL RESONATOR (Ta = –10 to + 70 °C)

Manufacture	Product Name	FREQUENCY (MHZ)	Recommended Circuit Constant			Oscillator Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	SMD-49	3.579545	27	27	1.5	2.0	6.0

CAPACITANCE (Ta = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmedsured pins retured to 0 V.	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, RESET			14	pF
			P60 to P63			20	pF
Input/Output	C_{IO}		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remarks The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

DC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37 P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72 $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch Open-drain)	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 6.0 V	V_{DD}-0.5		V_{DD}	V
				V_{DD}-0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			2.0 V≤ V_{DD} < 2.7 V*	0.9V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67. P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0		0.3 V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P60 to P63	4.5 V≤ V_{DD} ≤ 6.0 V	0		0.3 V_{DD}	V
			2.7 V≤ V_{DD} ≤ 4.5 V	0		0.2 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P04, XT2	4.5 V≤ V_{DD} ≤ 6.0 V	0		0.2 V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			2.0 V≤ V_{DD} < 2.7 V*	0		0.1 V_{DD}	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1mA		V_{DD}-1.0			V
		I_{OH} = –100 mA		V_{DD}-0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 6.0 V, open-drain pulled-up (R = 1 KΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

* For use as P07, use an inverter to input the reverse phase of P07 to the XT2 pin.

Remarks The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, RESET			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, RESET			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			– 20	μA
	I_{LIL3}		P60 to P63			– 3***1**	μA
Output leakage current high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL1}	V_{OUT} = 0 V				– 3	μA
Mask option pull-up resister	R_1	V_{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resister*2	R_2	V_{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130	4.5 V≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V≤ V_{DD} ≤ 4.5 V	20		500	kΩ

* **1.** When an input instruction is executed, the low-level input leakage current for P60 to P63 becomes -200 μA (MAX.) only in one clock cycle (no wait). It remains at -3 μA (MAX.) for other than an input instruction.

2. A software pull-up resistor can be used only in the range of V_{DD} = 2.7 to 6.0 V.

Remarks The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current ***5**	I_{DD1}	5.0 MHz Crystal oscillation operating mode (f_{XX} = 2.5 MHz)***3**	V_{DD} = 5.0 V ± 10 % ***1**		4	12	mA
			V_{DD} = 3.0 V ± 10 % ***2**		0.6	1.8	mA
			V_{DD} = 2.2 V ± 10 % ***2**		0.35	1.05	mA
		5.0 MHz Crystal oscillation operating mode (f_{XX} = 5.0 MHz)***4**	V_{DD} = 5.0 V ± 10 % ***1**		6.5	19.5	mA
			V_{DD} = 3.0 V ± 10 % ***2**		0.8	2.4	mA
	I_{DD2}	5.0 MHz Crystal oscillation HALT mode (f_{XX} = 2.5 MHz)***3**	V_{DD} = 5.0 V ± 10 % ***1**		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10 % ***2**		0.5	1.5	mA
			V_{DD} = 2.2 V ± 10 % ***2**		280	840	μA
		5.0 MHz Crystal oscillation HALT mode (f_{XX} = 5.0 MHz)***4**	V_{DD} = 5.0 V ± 10 % ***1**		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10 % ***2**		0.65	1.95	mA
	I_{DD3}	32.768 kHz Crystal oscillation operating mode ***6**	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		32	64	μA
			V_{DD} = 2.2 V ± 10 %		24	48	μA
	I_{DD4}	32.768 kHz Crystal oscillation HALT mode ***6**	V_{DD} = 5.0 V ± 10 %		25	55	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
			V_{DD} = 2.2 V ± 10 %		2.5	12.5	μA
	I_{DD5}	XT1 = 0 V STOP mode When feedback resister is used	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
			V_{DD} = 2.2 V ± 10 %		0.3	10	μA
	I_{DD6}	XT1 = 0 V STOP mode When feedback resister is unused	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA
			V_{DD} = 2.2 V ± 10 %		0.05	10	μA

***** **1.** Operating in high-speed mode (when set the processor clock control register to 00H).
2. Operating in low-speed mode (when set the processor clock control register to 04H).
3. Operation with $f_{XX} = f_X/2$ (when oscillation mode selection register is set to 00H)
4. Operation with $f_{XX} = f_X$ (when oscillation mode selection register is set to 01H)
5. The AV_{REF0}, AV_{REF1}, AV_{DD} currents and port current (including a current flowing in the on-chip pull-up resistor) are not included.
6. When the main system clock is halted

Remarks **1.** f_{XX}: Main system clock frequency (f_X or $f_X/2$)
2. f_X: Main system clock oscillatior frequency

AC CHARACTERISTICS

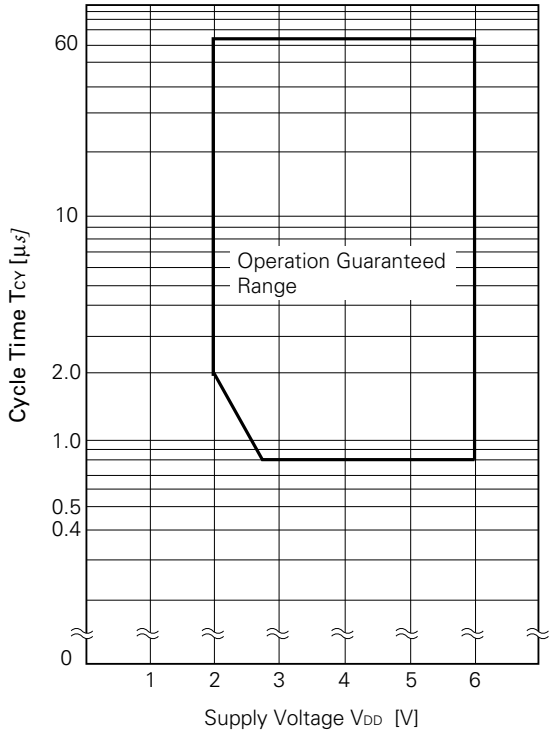
(1) BASIC OPERATION (T_a = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ ***1**	V_{DD} = 2.7 to 6.0 V	0.8		64	μs
					2.2		64	μs
			$f_{XX} = f_X$ ***2**	4.5 V≤ V_{DD} ≤ 6.0 V	0.4		32	μs
				2.7 V≤ V_{DD} ≤ 4.5 V	0.8		32	μs
		Operating on sub systema clock			40	122	125	ms
TI input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V			0		4	MHz
					0		275	kHz
TI input high/low-level width	t_{TIH},t_{TIL}	V_{DD} = 4.5 to 6.0 V			100			ns
					1.8			μs
Interrupt input high/low-level width	t_{INTH},t_{INTL}	INTP0			8/f_{sam} ***3**			μs
		INTP1 to INTP6, KR0 to KR7		V_{DD} = 2.7 to 6.0 V	10			μs
					20			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}	V_{DD} = 2.7 to 6.0 V			10			μs
					20			μs

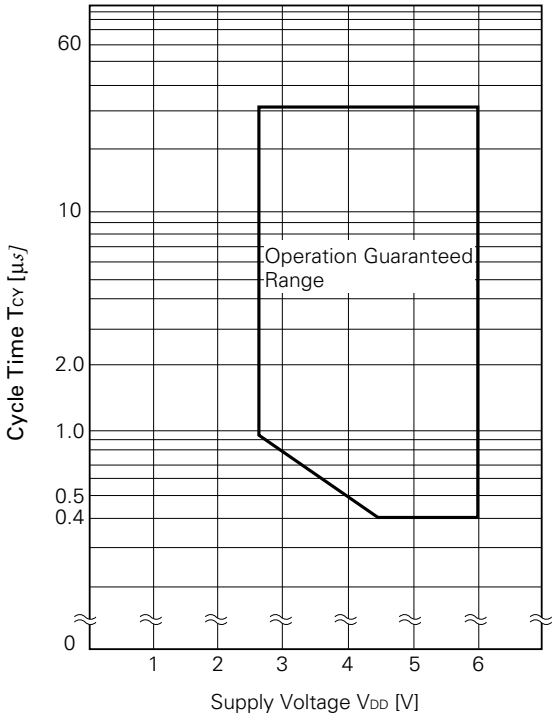
* **1.** When oscillation mode selection register is set to 00H
2. When oscillation mode selection register is set to 01H
3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of fsam is possible between $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$ and $f_{XX}/128$ (when N= 0 to 4).

Remarks 1. f_{XX}: Main system clock frequency (f_X or $f_X/2$)
2. f_X: Main system clock oscillation frequency

T_{CY} vs V_{DD} (AT $f_{XX} = f_X/2^N$ MAIN SYSTEM CLOCK OPERATION)



T_{CY} vs V_{DD} (AT $f_{XX} = f_X$ MAIN SYSTEM CLOCK OPERATION)



(2) READ/WRITE OPERATION

(a) When MCS = 1, PCC2 to PCC0 = 000B (Ta = –40 to + 85 °C, V_{DD} = 4.5 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY} - 50$		ns
Address setup time	t_{ADS}		$0.85t_{CY} - 50$		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85+2n)t_{CY}-80$	ns
	t_{ADD2}			$(4+2n)t_{CY}-100$	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2+2n)t_{CY}-100$	ns
	t_{RDD2}			$(2.85+2n)t_{CY}-100$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2+2n)t_{CY}-60$		ns
	t_{RDL2}		$(2.85+2n)t_{CY}-60$		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.85t_{CY}-50$	ns
	t_{RDWT2}			$2t_{CY}-60$	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{CY}-60$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15+2n)t_{CY}$	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85+2n)t_{CY}-100$		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.85+2n)t_{CY}-60$		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY} + 20$		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.85t_{CY} - 10$	$1.15t_{CY} + 20$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.85t_{CY} - 50$	$1.15t_{CY} + 50$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\uparrow$	t_{RDWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY} + 40$	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$1.15t_{CY} + 40$	$3.15t_{CY} + 40$	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$1.15t_{CY} + 30$	$3.15t_{CY} + 30$	ns

Remarks
1. MCS: Oscillation mode selection register bit 0
2. PCC2 to PCC0: Processor clock control register bit 2 to bit 0
3. $t_{CY} = T_{CY}/4$
4. n indicates number of waits.

(b) When except MCS = 1, PCC2 to PCC0 = 000B (Ta = –40 to + 85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}	V_{DD} = 2.7 to 6.0 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address setup time	t_{ADS}	V_{DD} = 2.7 to 6.0 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address hold time	t_{ADH}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} – 10		ns
			0.37t_{CY} – 40		ns
Data input time from address	t_{ADD1}	V_{DD} = 2.7 to 6.0 V		(3+2n)t_{CY}–160	ns
				(3+2n)t_{CY}–320	ns
	t_{ADD2}	V_{DD} = 2.7 to 6.0 V		(4+2n)t_{CY}–200	ns
				(4+2n)t_{CY}–300	ns
Data input time from $\overline{RD}$↓	t_{RDD1}	V_{DD} = 2.7 to 6.0 V		(1.4+2n)t_{CY}–70	ns
				(1.37+2n)t_{CY}–120	ns
	t_{RDD2}	V_{DD} = 2.7 to 6.0 V		(2.4+2n)t_{CY}–70	ns
				(2.37+2n)t_{CY}–120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}	V_{DD} = 2.7 to 6.0 V	(1.4+2n)t_{CY}–20		ns
			(1.37+2n)t_{CY}–20		ns
	t_{RDL2}	V_{DD} = 2.7 to 6.0 V	(2.4+2n)t_{CY}–20		ns
			(2.37+2n)t_{CY}–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}	V_{DD} = 2.7 to 6.0 V		t_{CY}–100	ns
				t_{CY}–200	ns
	t_{RDWT2}	V_{DD} = 2.7 to 6.0 V		2t_{CY}–100	ns
				2t_{CY}–200	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}	V_{DD} = 2.7 to 6.0 V		2t_{CY}–100	ns
				2t_{CY}–200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1+2n)t_{CY}	(2+2n)t_{CY}	ns
Write data setup time	t_{WDS}	V_{DD} = 2.7 to 6.0 V	(2.4+2n)t_{CY}–60		ns
			(2.37+2n)t_{CY}–100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}	V_{DD} = 2.7 to 6.0 V	(2.4+2n)t_{CY}–20		ns
			(2.37+2n)t_{CY}–20		ns
$\overline{RD}$↓ delay time from $\overline{ASTB}$↓	t_{ASTRD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} –30		ns
			0.37t_{CY} – 50		ns
$\overline{WR}$↓ delay time from $\overline{ASTB}$↓	t_{ASTWR}	V_{DD} = 2.7 to 6.0 V	1.4t_{CY} –30		ns
			1.37t_{CY} –50		ns

Remarks **1.** MCS: Oscillation mode selection register bit 0

2. PCC2 to PCC0: Processor clock control register bit 2 to bit 0

3. $t_{CY} = T_{CY}/4$

4. n indicates number of waits.

(b) When except MCS = 1, PCC2 to PCC0 = 000B (Ta = –40 to + 85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{ASTB}$↓ delay time from $\overline{RD}$↓ in external fetch	t_{RDAST}		t_{CY} –10	1.15t_{CY} + 20	ns
Address hold time from $\overline{RD}$↓ in external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↓	t_{RDWD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} – 20		ns
			0.37t_{CY} – 40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 2.7 to 6.0 V	0	60	ns
			0	120	ns
Address hold time from $\overline{WR}$↓	t_{WRADH}	V_{DD} = 2.7 to 6.0 V	t_{CY}	t_{CY} + 60	ns
			t_{CY}	t_{CY} + 120	ns
$\overline{RD}$↓ delay time from $\overline{WAIT}$↓	t_{WTRD}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY} + 180	2.6t_{CY} + 180	ns
			0.63t_{CY} + 350	2.63t_{CY} + 350	ns
$\overline{WR}$↓ delay time from $\overline{WAIT}$↓	t_{WTWR}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY} + 120	2.6t_{CY}+ 120	ns
			0.63t_{CY} + 240	2.63t_{CY}+ 240	ns

Remarks
1. MCS: Oscillation mode selection register bit 0
2. PCC2 to PCC0: Processor clock control register bit 2 to bit 0
3. $t_{CY} = T_{CY}/4$
4. n indicates number of waits.

(3) SERIAL INTERFACE (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} ≤ 4.5 V	1600			ns
			3200			ns
$\overline{SCK}$ high/low-level width	t_{KH1},t_{KL1}	V_{DD} = 4.5 to 6.0 V	t_{KCY}1/2-50			ns
			t_{KCY}1/2-100			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} ≤ 4.5 V	150			ns
			300			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}		400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	C = 100 pF*			300	ns

* C is the load capacitance of SO output line.

(b) 3-wire serial I/O mode ($\overline{SCK}$... Internal clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} ≤ 4.5 V	1600			ns
			3200			ns
$\overline{SCK}$ high/low-level width	t_{KH2},t_{KL2}	V_{DD} = 4.5 to 6.0 V	400			ns
		2.7 V ≤ V_{DD} ≤ 4.5 V	800			ns
			1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}		300			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	C = 100 pF*			300	ns

* C is the load capacitance of SO output line.

(c) SBI mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
	t_{KL3}			t_{KCY3}/2-150			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R = 1 kΩ ,	V_{DD} = 4.5 to 6.0 V	0		250	ns
		C = 100 pF*		0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

***** R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(d) SBI mode ($\overline{SCK}$... Internal clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO4}	R = 1 kΩ ,	V_{DD} = 4.5 to 6.0 V	0		3000	ns
		C = 100 pF*		0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns

***** R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(e) 2-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF*	V_{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{SCK}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 6.0 V	t_{KCY5}/2-160			ns
				t_{KCY5}/2-190			ns
$\overline{SCK}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 6.0 V	t_{KCY5}/2-50			ns
				t_{KCY5}/2-100			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 6.0 V	300			ns
			2.7 V ≤ V_{DD} ≤ 4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO5}			0		300	ns

* R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(f) 2-wire serial I/O mode ($\overline{SCK}$... Internal clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY6}	V_{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{SCK}$ high-level width	t_{KH6}	V_{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{SCK}$ low-level width	t_{KL6}	V_{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI6}			t_{KCY6}/2			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns

* R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(g) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK}$...Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY7}	4.5 V - V_{DD} - 6.0 V	800			ns
		2.7 V - V_{DD} - 4.5 V	1600			ns
			3200			ns
$\overline{SCK}$ high/low-level width	t_{KH7} t_{KL7}	V_{DD} = 4.5 to 6.0 V	t_{KCY7}/2-50			ns
			t_{KCY7}/2-100			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK7}	4.5 V - V_{DD} - 6.0 V	100			ns
		2.7 V - V_{DD} - 4.5 V	150			ns
			300			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI7}		400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO7}	C = 100 pF*			300	ns
STB↑ from $\overline{SCK}$↑	t_{SBD}		t_{KCY7}/2–100		t_{KCY7}/2+100	ns
Strobe signal high-level width	t_{SBW}	V_{DD} = 2.7 to 6.0V	t_{KCY7}–30		t_{KCY7}+30	ns
			t_{KCY7}–60		t_{KCY7}+60	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V - V_{DD} - 6.0 V	100			ns
		2.7 V - V_{DD} - 4.5 V	150			ns
			200			ns
$\overline{SCK}$↓ from busy inactive	t_{SPS}				2t_{KCY7}	ns

* C is the load capacitance of the SO output line.

(h) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK}$...External clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY8}	4.5 V - V_{DD} - 6.0 V	800			ns
		2.7 V - V_{DD} - 4.5 V	1600			ns
			3200			ns
$\overline{SCK}$ high/low-level width	t_{KH8} t_{KL8}	4.5 V - V_{DD} - 6.0 V	400			ns
		2.7 V - V_{DD} - 4.5 V	800			ns
			1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK8}		100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KIS8}		400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO8}	C = 100 pF*			300	ns

* C is the load capacitance of the SO output line.

(i) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
Transfer rate		4.5 V - V_{DD} - 6.0 V			78215	bps
		2.7 V - V_{DD} < 4.5 V			39063	bps
					19531	bps

(j) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
ASCK cycle time	t_{KCY9}	4.5 V - V_{DD} - 6.0 V	800			ns
		2.7 V - V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high-/low-level width	t_{KH9}, t_{KL9}	4.5 V - V_{DD} - 6.0 V	400			ns
		2.7 V - V_{DD} < 4.5 V	1000			ns
			1600			ns
Transfer rate		4.5 V - V_{DD} - 6.0 V			39063	bps
		2.7 V - V_{DD} < 4.5 V			19531	bps
					9766	bps

(4) A/D CONVERTER (Ta = –40 to +85 °C, $AV_{DD} = V_{DD}$ = 2.0 to 6.0 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
Resolution			8	8	8	bit
Overall error*		$2.7\ V \le AV_{REF0} \le AV_{DD}$			0.6	%
		$2.7\ V \le AV_{REF0} < 2.7\ V$			1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/fxx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.0		AV_{DD}	V
AV_{REF0} to AV_{SS} current	R_{AIREF0}		4	14		kΩ

* Overroll error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Remarks 1. fxx: Main system clock frequency (fx or fx/2)
2. fx: Main system clock oscillation frequency

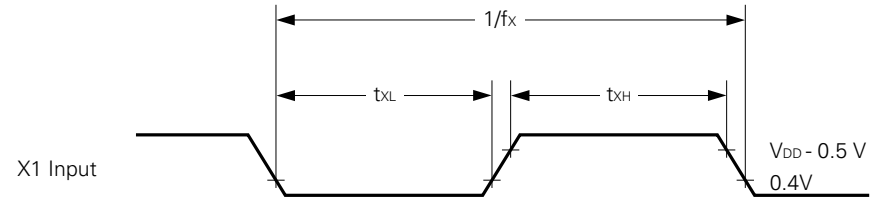
(5) D/A CONVERTER (Ta = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V, $AV_{SS} = V_{SS}$ = 0 V)

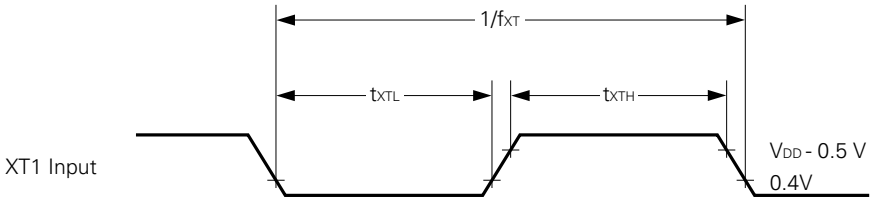
Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	UNIT
Resolution						8	bit
Overall error		R = 2MΩ***1**				1.2	%
		R = 4MΩ***1**				0.8	%
		R = 10MΩ***1**				0.6	%
Settling time		C=30pF*	$4.5\ V \le AV_{REF1} \le 6.0\ V$			10	μs
			$2.7\ V \le AV_{REF1} < 4.5\ V$			15	μs
			$2.0\ V \le AV_{REF1} < 2.7\ V$			20	μs
Output resistance	R_0	DACS0, DACS1 = 55H***2**			10		kΩ
Analog reference voltage	AV_{REF1}			2.0		V_{DD}	V
AV_{REF1} current	I_{REF1}	***2**				1.5	μs

* **1.** R and C denote D/A converter output pin load resistance and load capacitance, respectively.
2. Value for 1 D/A converter channel

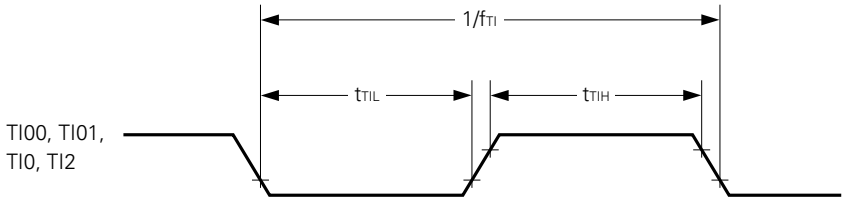
AC Timing Test Point (Excluding X1, XT1 Input)

Clock Timing



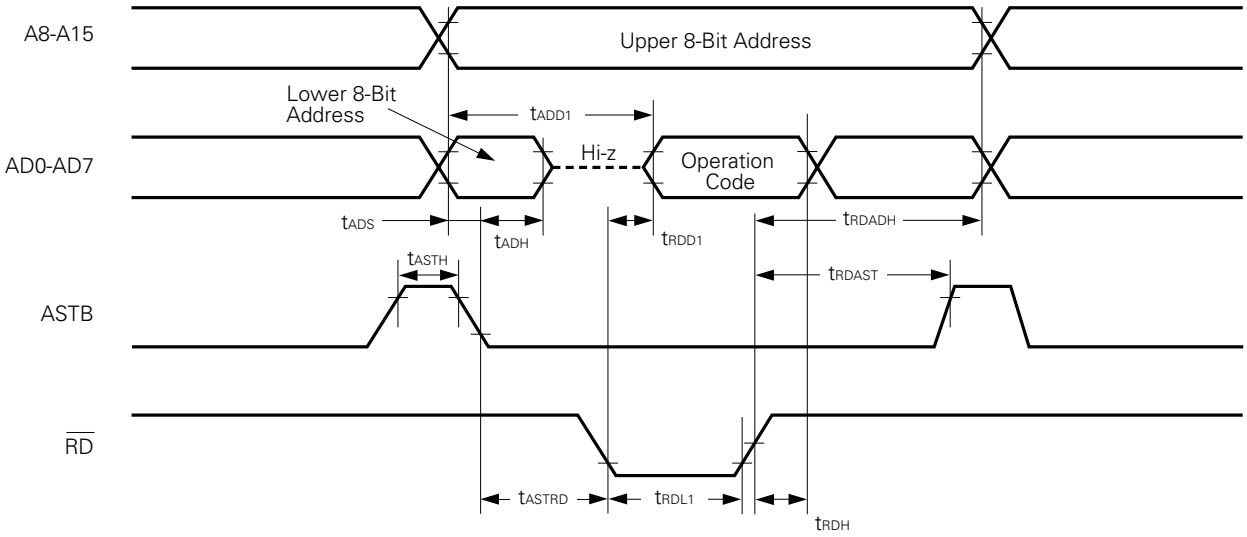


TI Timing

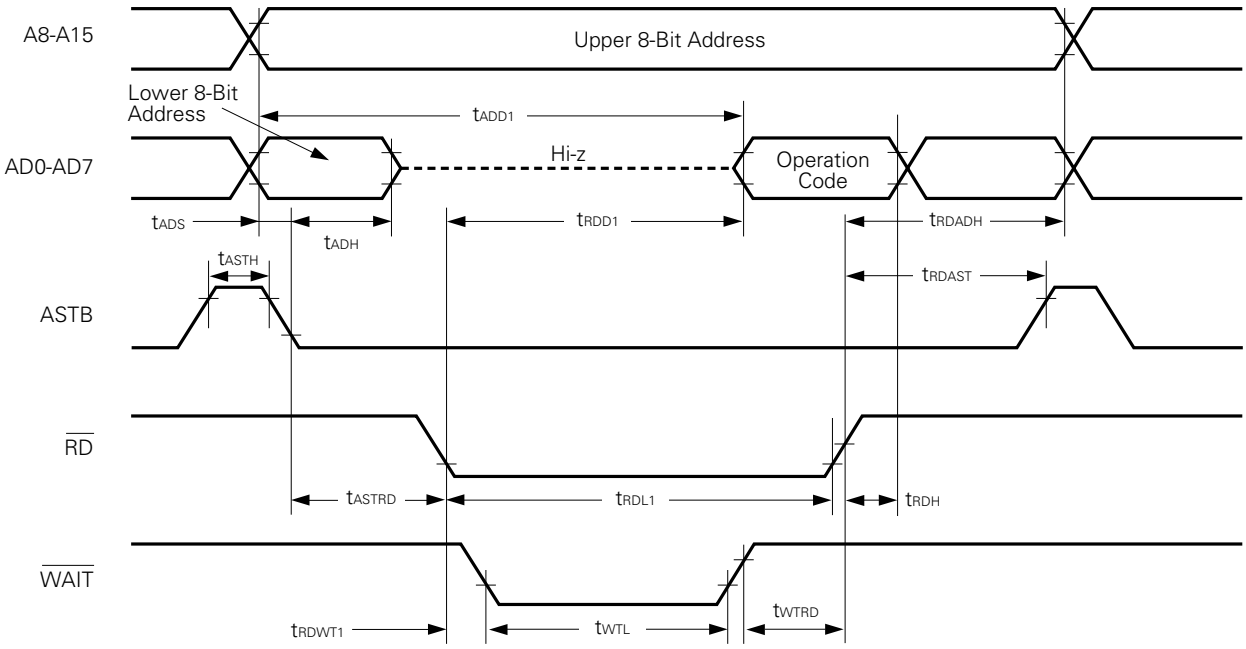


Read/Write Operation

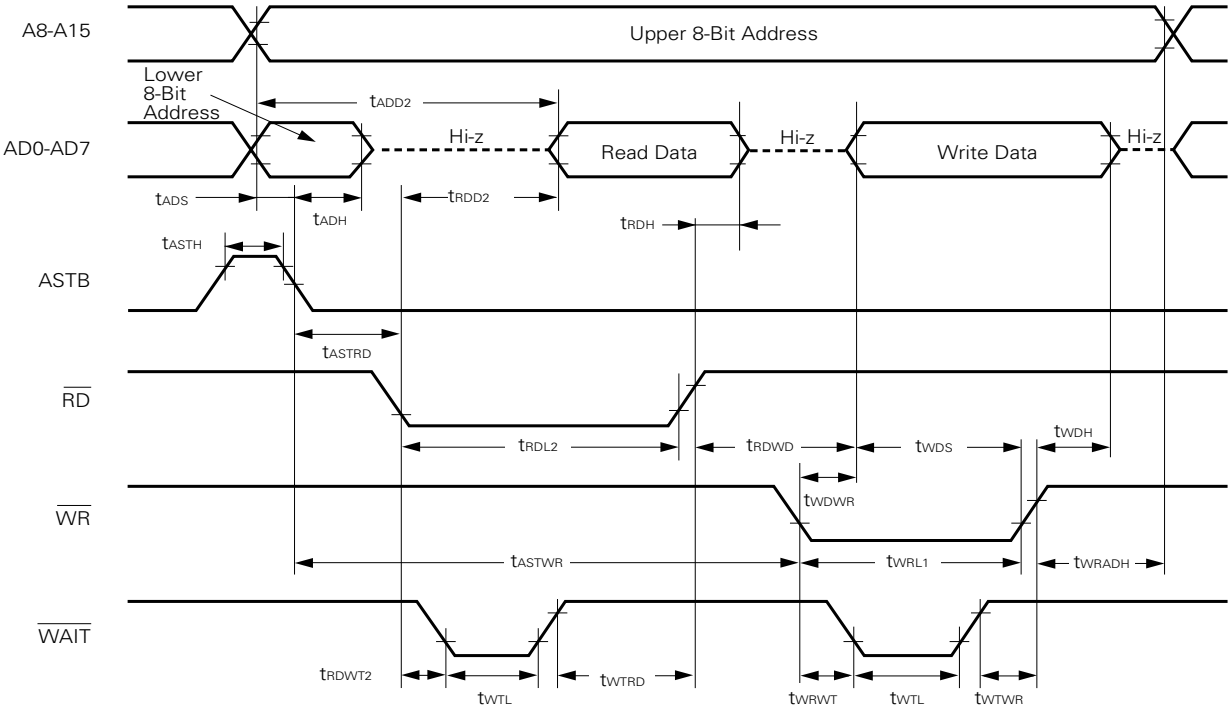
External Fetch (No Wait) :



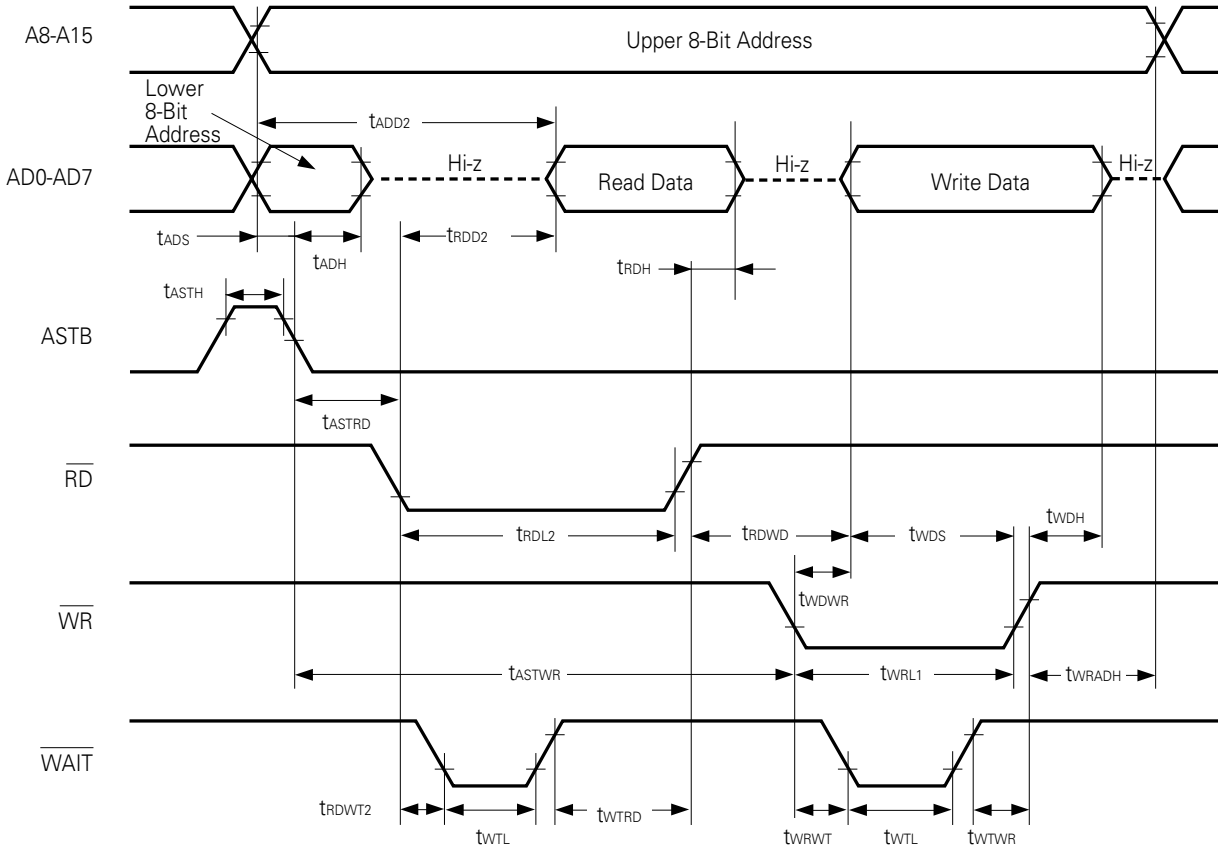
External Fetch (Wait Insertion) :



External Data Access (No Wait) :

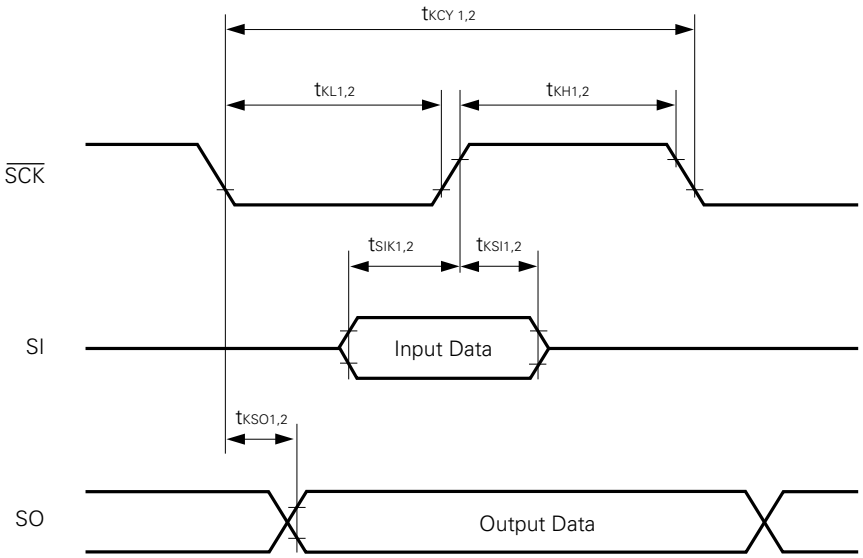


External Data Access (Wait Insertion) :

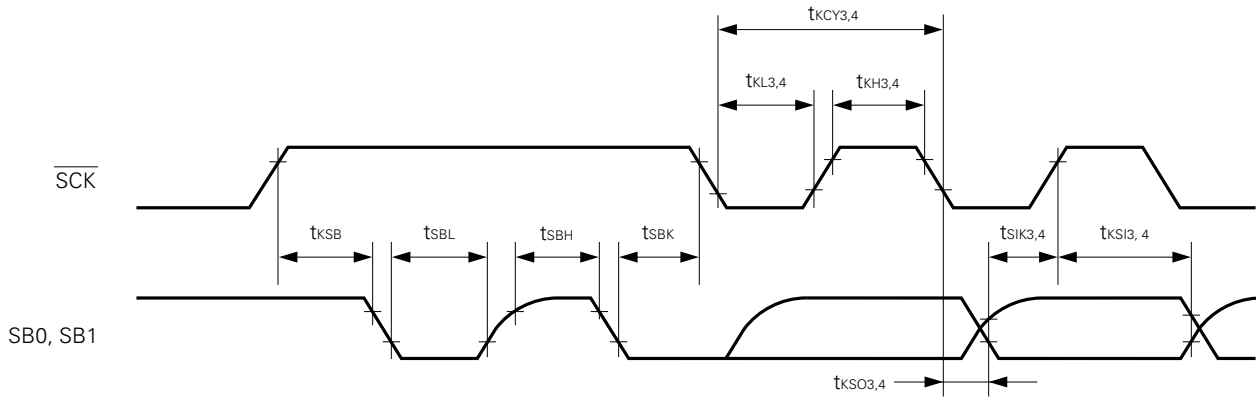


Serial Transfer Timing

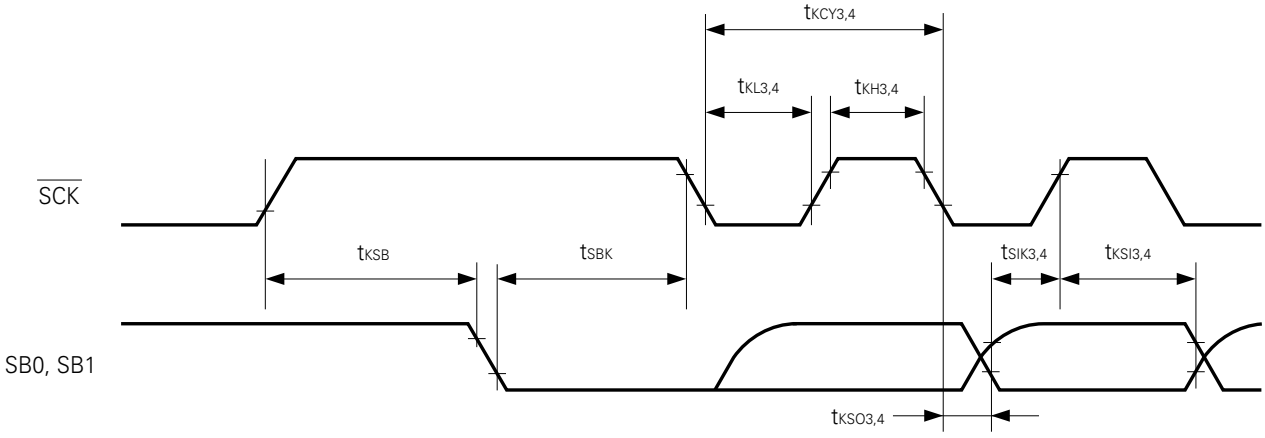
3-Wire Serial I/O Mode :



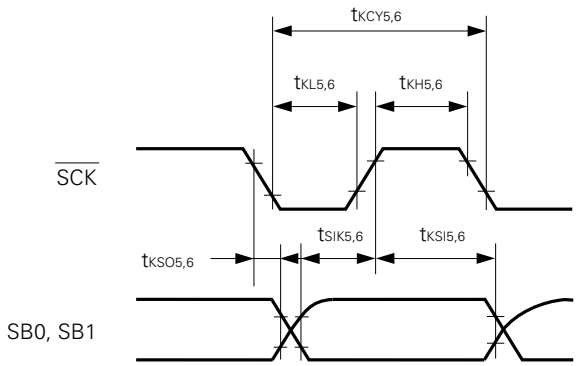
SBI Mode(Bus Release Signal Transfer) :



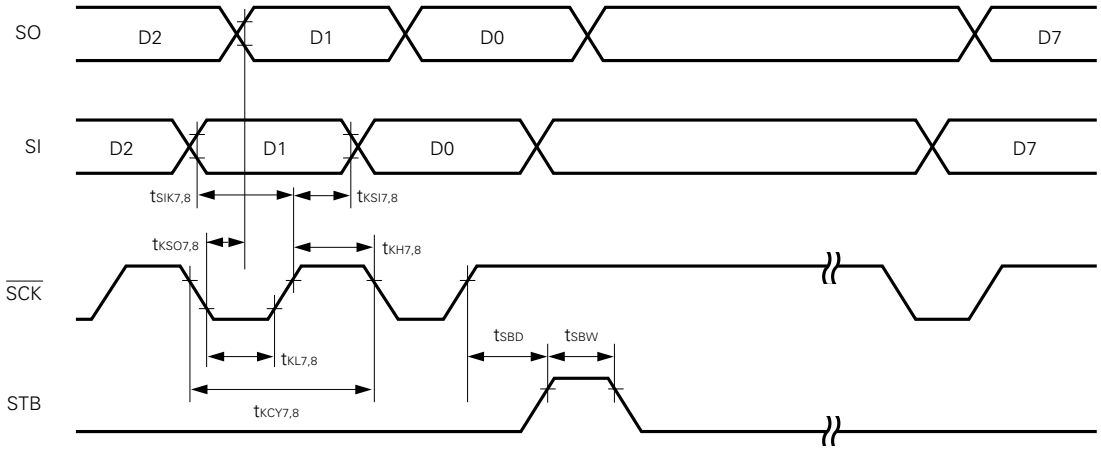
SBI Mode (COmmand Signal Transfer) :



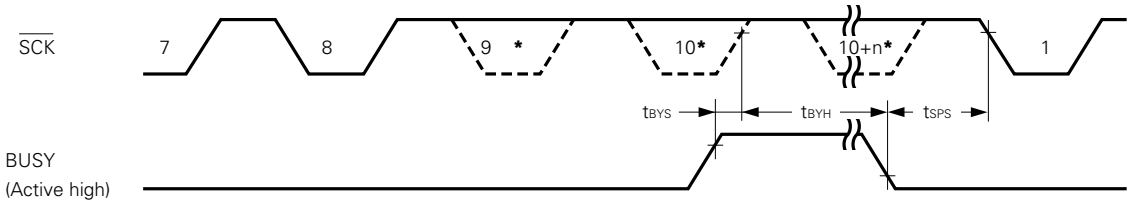
2-Wire Serial I/O Mode :



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function :

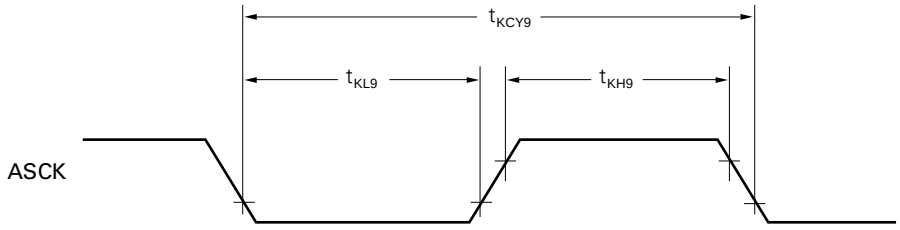


3-Wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing) :



***** The signal is not actually driven low here; it is shown as such to indicate the timing.

UART Mode (External Clock Input) :



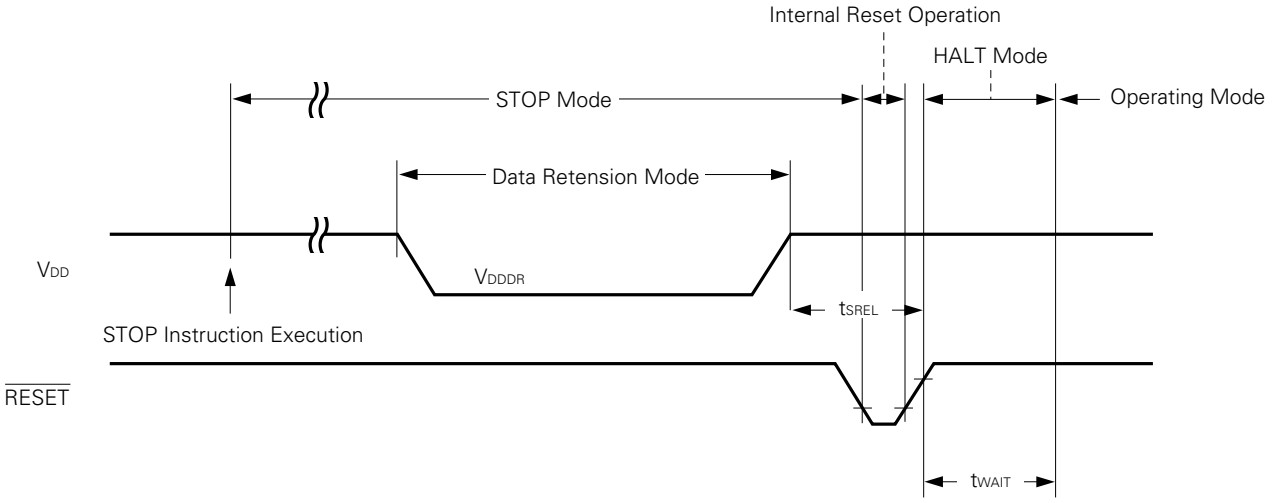
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGEDATA RETENTION CHARACTERISTICS (Ta = –40 to + 85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8	6.0		V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resister disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt		*		ms

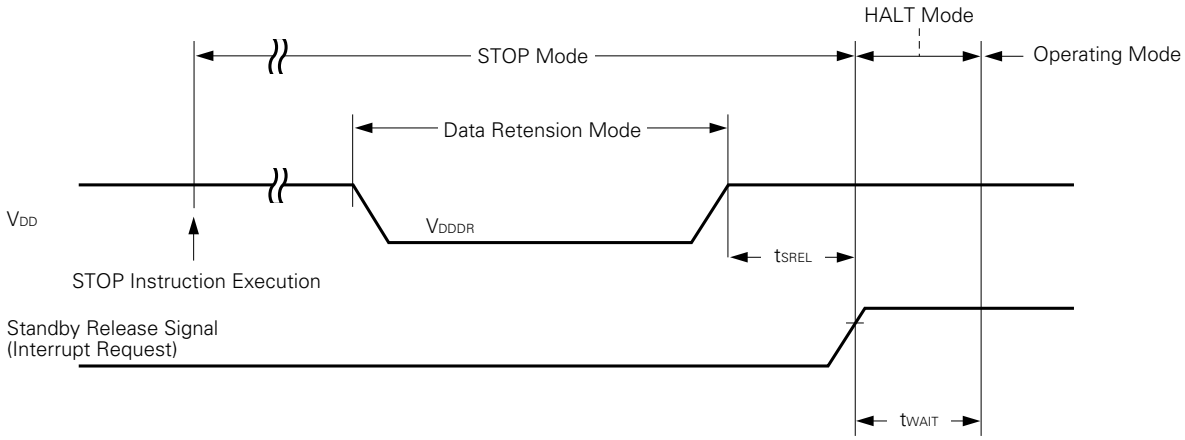
* In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of 2^{12}/fxx and 2^{14}/fxx to 2^{17}/fxx is possible.

Remarks 1. fxx: Main system clock frequency (fx or fx/2)
2. fx: Main system clock oscillatior frequency

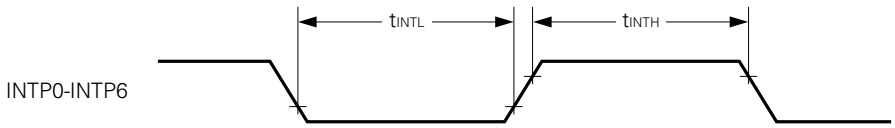
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



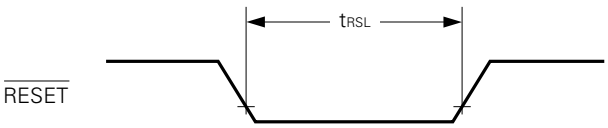
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Interrupt Input Timing

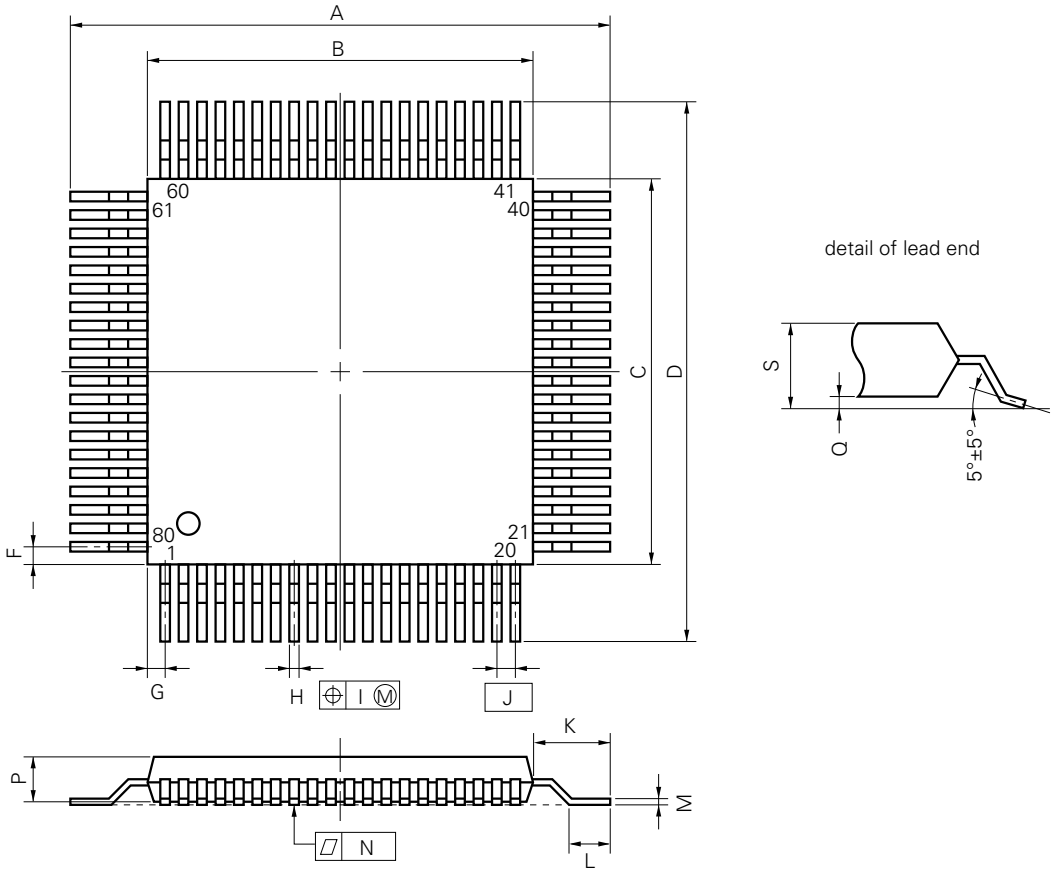


$\overline{\text{RESET}}$ Input Timing



12. PACKAGE INFORMATION

80 PIN PLASTIC QFP (□14) ★



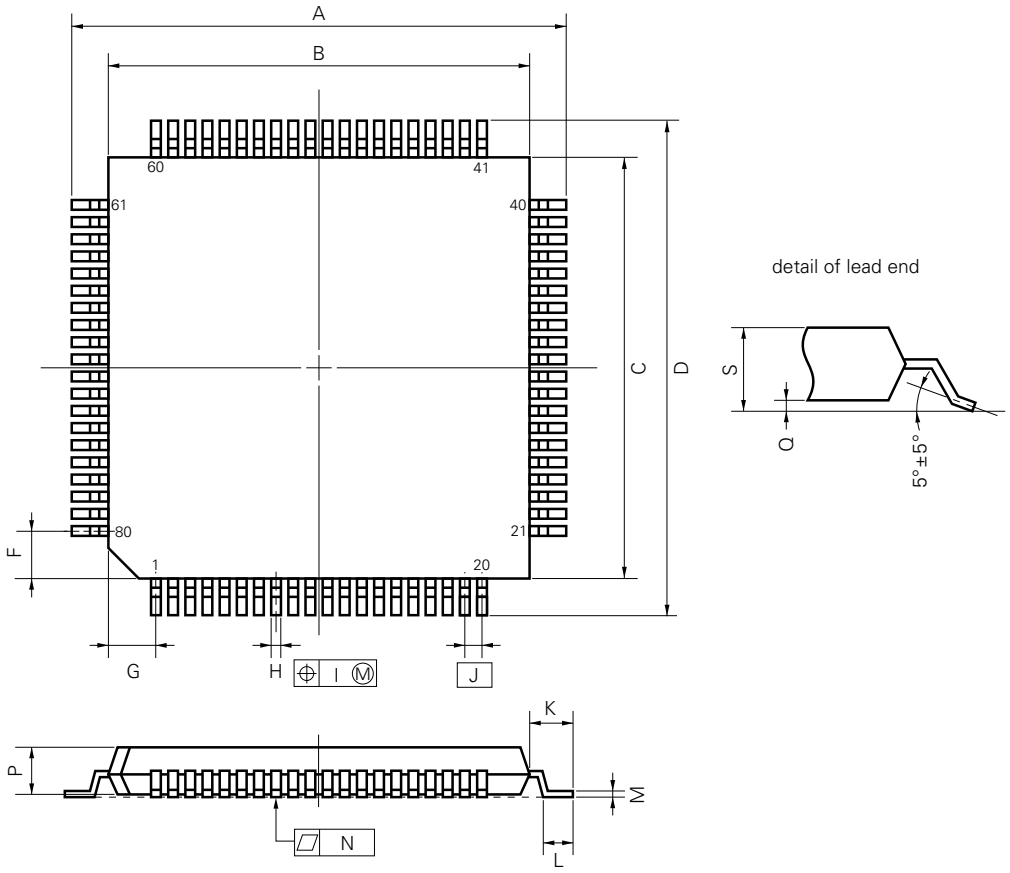
S80GC-65-3B9-3

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



P80GK-50-BE9-3

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.4	0.551±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.4	0.551±0.016
F	1.25	0.049
G	1.25	0.049
H	0.20±0.10	0.008±0.004
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.001}$
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
S	1.27 MAX.	0.05 MAX.

13. RECOMMENDED SOLDERING CONDITIONS ★

This product should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **"Semiconductor Device Mount Manual" (IE-1207)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 13-1 Surface Mounting Type Soldering Conditions (1/2)

(1) μPD78052GC-×××-3B9 : 80-pin plastic QFP (□14 mm)
μPD78053GC-×××-3B9 : 80-pin plastic QFP (□14 mm)
μPD78054GC-×××-3B9 : 80-pin plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max. < precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Twice max. <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature : 260 °C max., Duration : 10 sec. max., Number of times : once, Preheating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Pin Part Heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 13-1 Surface Mounting Type Soldering Conditions (2/2)

(1) μPD78055GC-×××-3B9 : 80-pin plastic QFP (□14 mm)
μPD78056GC-×××-3B9 : 80-pin plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max. < precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Twice max. <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Pin Part Heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

(3) μPD78052GK-×××-BE9 : 80-pin plastic QFP (□12 mm)
μPD78053GK-×××-BE9 : 80-pin plastic QFP (□12 mm)
μPD78054GK-×××-BE9 : 80-pin plastic QFP (□12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max., Time limit: 7 days* (thereafter 10 hours 125 °C prebaking required) < precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-107-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Twice max., Time limit: 7 days* (thereafter 10 hours 125 °C prebaking required) <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-107-2
Pin Part Heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

* For the storage period after dry-pack decompression storage conditions are max. 25 °C, 65 % RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78054.

Language Processing Software

RA78K/0 ***1,2,3***	78K/0 series common assembler package
CC78K/0 ***1,2,3***	78K/0 series common C compiler package
CC78K/0-L ***1,2,3***	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054GK PA-78P054KK-T	Programmer adapters connected to PG-1500
PG-1500 controller ***1,2,4***	PG-1500 control program

Debugging Tools

IE-78000-R	In-circuit emulator common to 78K/0 series
IE-78000-R-BK	Break board common to 78K/0 series ★
IE-78064-R-EM	Emulation board common to μPD78064 subseries
EP-78230GC-R	Emulation probe common to μPD78234 subseries
EP-78054GK-R	Emulation probe for μPD78054 subseries
EV-9200GC-80	Socket to be mounted on the user system board manufactured for 80-pin plastic QFP
EV-9200GK-80	Adapter to be mounted in the user system board manufactured for 80-pin plastic TQFP
SD78K/0***1,2***	IE-78000-R screen debugger
DF78054***1,2***	Device file for μPD78054 subseries

Real-Time OS

RX78K/0 ***1,2,3***	78K/0 series common real-time OS

* **1.** PC-9800 series (MS to DOS™) based
2. IBM PC/AT™ (PC DOS™) based
3. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series™ (EWS-UX/V™) based
4. Under development

Fuzzy Inference Development Support System

FE9000 ***1**/ FE9200 ***2**	Fuzzy knowledge data creation tool
FT9080 ***1**/ FT9085 ***3**	Translator
FI78K/0 ***1,3**	Fuzzy inference module
★ FD78K/0 ***1,3**	Fussy inference debugger

* **1.** PC-9800 series (MS-DOS™) based
2. IBM PC/AT (PC DOS + Windows™) based
3. IBM PC/AT (PC DOS) based

Remarks For third party development tools, see the **78K/0 Series Selection Guide (IF-357)**.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No.
User's Manual		IEU-1356
78K/0 Series Application Note	Introduction (II)	IEA-1299 ★
	Floating point operation program volume	IEA-1289

Development Tool Related Documents (User's Manual)

Document Name		Document No.
RA78K Series Assembler Package	Operation Volume	EEU-1399
	Language Volume	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-1402
CC78K Series C Compiler	Operation Volume	EEU-1280
	Language Volume	EEU-1284
PG-1500 PROM Programmer		EEU-1335
PG-1500 Controller		EEU-1291
IE-78000-R		EEU-1398
IE-78000-R-BK		EEU-1427 ★
IE-78064-R-EM		EEU-1443
SD78K/0 Screen Debugger	Primer	EEU-1414
	Reference	EEU-1413

Other Related Documents

Document Name	Document No.
Package Manual	IEI-1213
Surface Mount Technology Manual	IEI-1207
Quality Grades on Semiconductor Devices	IEI-1209
Semiconductor Devices Quality Guarantee Guide	MEI-1202

Note The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

[MEMO]

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