NEC

MOS INTEGRATED CIRCUIT

μPD78P064Y

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78P064Y is a product in which the I²C bus control function is added to the μPD78P064 and this product is an 8-bit single-chip microcomputer which has on-chip one-time PROM which can be written to once only, or on-chip EPROM which can be programmed, erased, and reprogrammed.

As program write by user is possible, the μPD78P064Y is best suited for evaluation, short-run and multiple-device production, and early rise upon system development.

Please see materials for mask ROM products at the same time when you see this technical data.

FEATURES

- Pin compatible with mask ROM products (except the V_{PP} pin)
- Internal PROM : 32K bytes*
- Internal high-speed RAM : 1024 bytes*
- Connectable to I²C bus interface
- LCD display RAM : 40 × 4 bits
- Operable in the same range of supply voltage as mask ROM products (2.7 to 6.0 V)

* Internal PROM and internal high-speed RAM capacities can be changed by memory size switching register.

Differs from Mask ROM Products in Following Points

- The same memory mapping as mask ROM products is enabled by setting the memory size switching register.
- An LCD drive power supply split resistor is not incorporated.

ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM
μPD78P064YGC-7EA	100-pin plastic QFP (body 14 × 14 mm)	One-Time PROM
μPD78P064YGF-3BA	100-pin plastic QFP (body 14 × 20 mm)	One-Time PROM
μPD78P064YKL-T*	100-pin ceramic LCC with window (body 14 × 20 mm)	EPROM

* In the planning stage

In this document, "PROM" is used in parts common to one-time PROM products and EPROM products.

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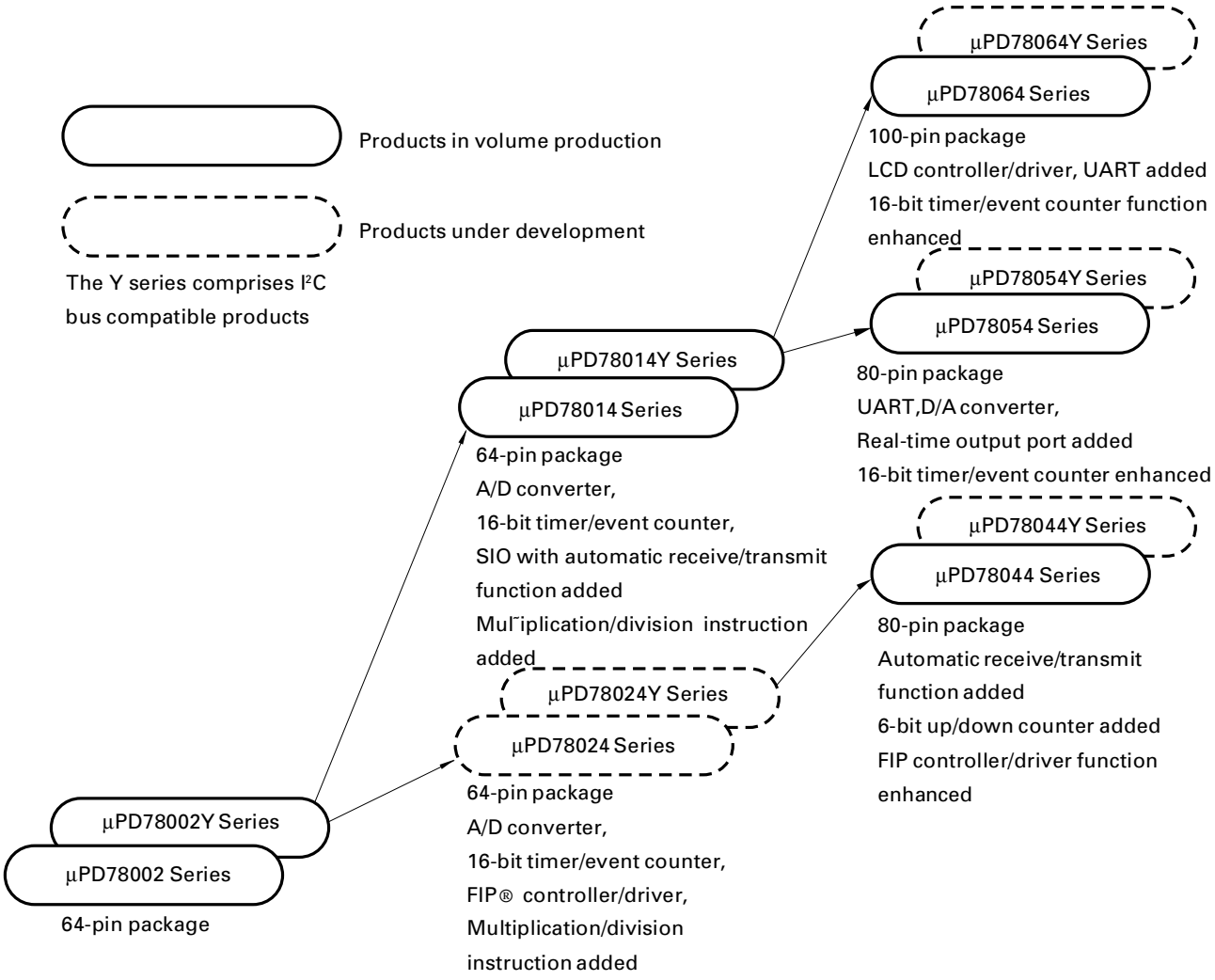
The mark ★ shows major revised points.

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES DEVELOPMENT



FUNCTION DESCRIPTION

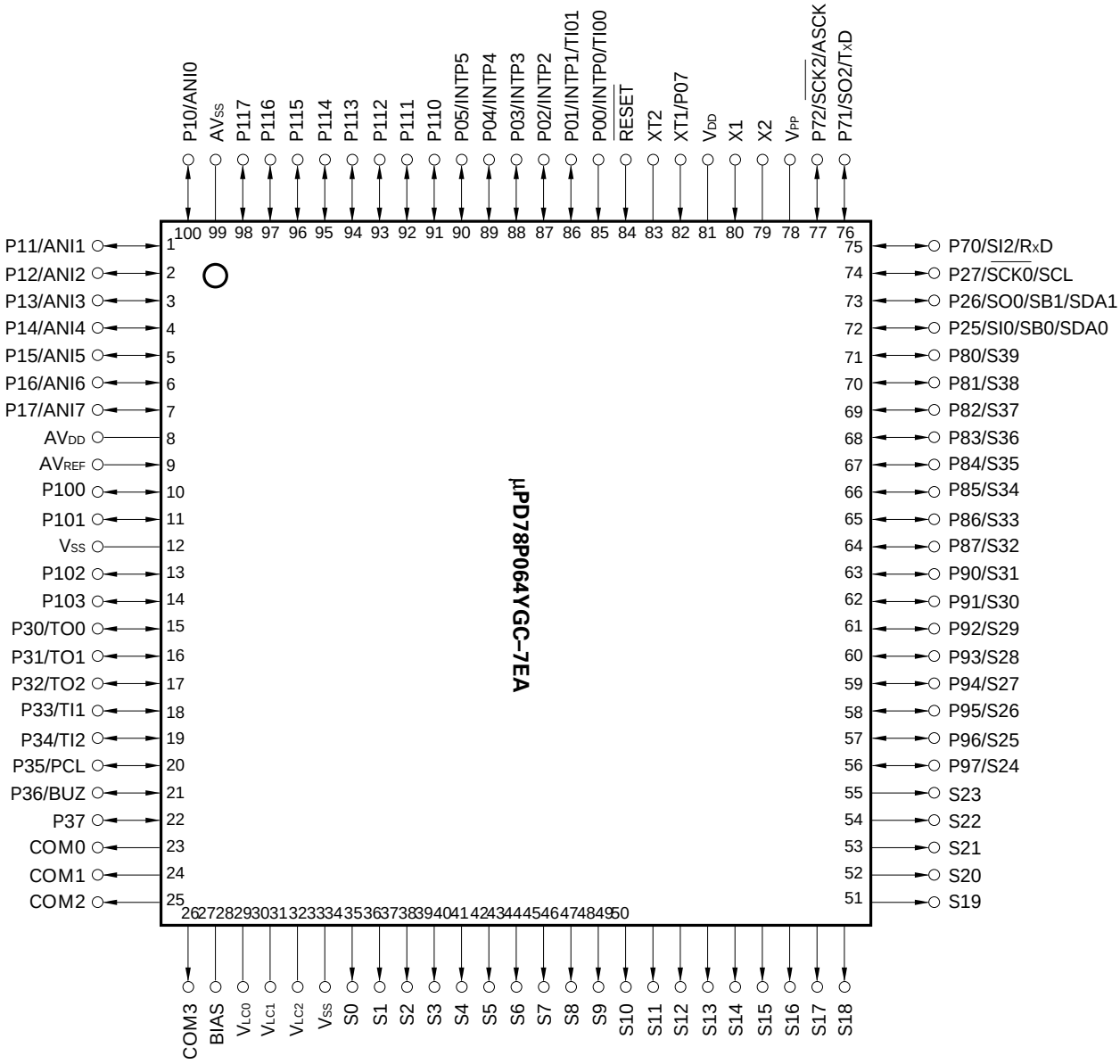
Item		Function
Internal memory		• PROM : 32 K bytes* • RAM Internal high-speed RAM : 1024 bytes* LCD display RAM : 40 × 4 bits
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycles		Instruction execution time variable function is built in.
	When main system clock is selected	0.4μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (when operating at 5.0 MHz)
	When subsystem clock is selected	122 μs (when operating at 32.768 kHz)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.
I/O ports [Include segment signal output dual-function pin]		Total : 57 • CMOS input : 2 • CMOS input/output : 55
A/D converter		• 8-bit resolution × 8 ch
LCD controller/driver		• Segment signal output : 40 max. • Common signal output : 4 max. • Bias : 1/2, 1/3, Bias switchable
Serial interface		• 3-wire/SBI/2-wire /I²C bus mode selectable : 1 ch • 3-wire/UART mode selectable : 1 ch
Timer		• 16-bit timer/event counter : 1 ch • 8-bit timer/event counter : 2 ch • Watch timer : 1 ch • Watchdog timer : 1 ch
Timer output		3 pins (14-bit PWM output enable 1 pin)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 kHz, 2.5 MHz, 5.0 MHz (when operating at main system clock 5.0 MHz) 32.7 kHz (when operating at subsystem clock 32.768 kHz)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (when operating at main system clock 5.0 MHz)
Vectored interrupt	Maskable interrupt	Internal : 12, External : 6
	Non-maskable interrupt	Internal : 1
	Software interrupt	Internal : 1
Test input		Internal : 1, External : 1
Operating voltage range		V_{DD} = 2.0 to 6.0 V ★
Package		• 100-pin plastic QFP (fine pitch) (□ 14 mm) • 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN (14 × 20 mm)

* Internal PROM/internal high-speed RAM capacity can be changed by memory size switching register.

PIN CONFIGURATION (Top View)

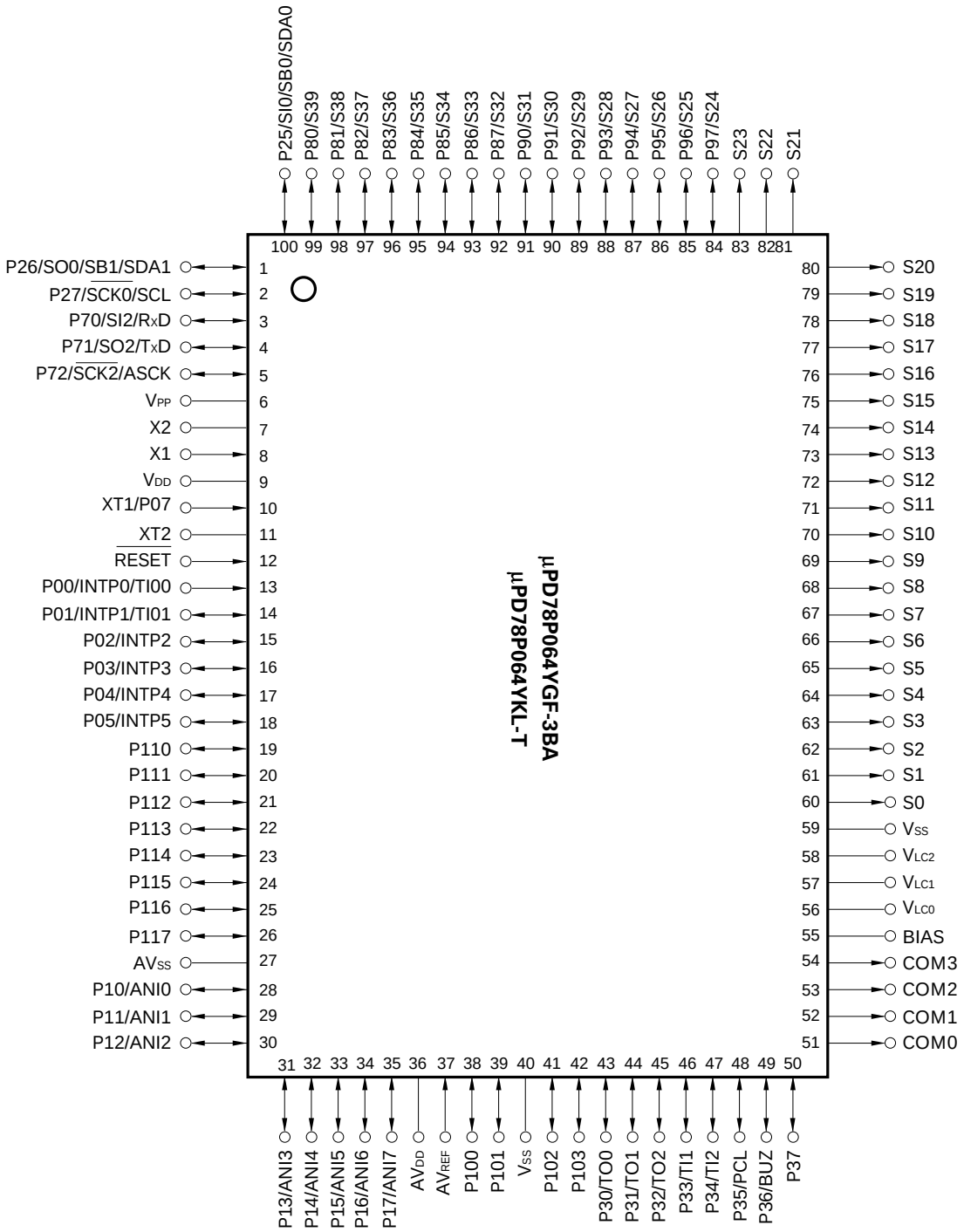
(1) Normal operating mode

100-pin plastic QFP (fine pitch) (□ 14 mm)



Note 1. Connect V_{PP} pin to V_{SS}.
2. Connect AV_{DD} pin to V_{DD}.
3. Connect AV_{SS} pin to V_{SS}.

100-pin plastic QFP (14 × 20 mm)
100-pin ceramic WQFN (14 × 20 mm)



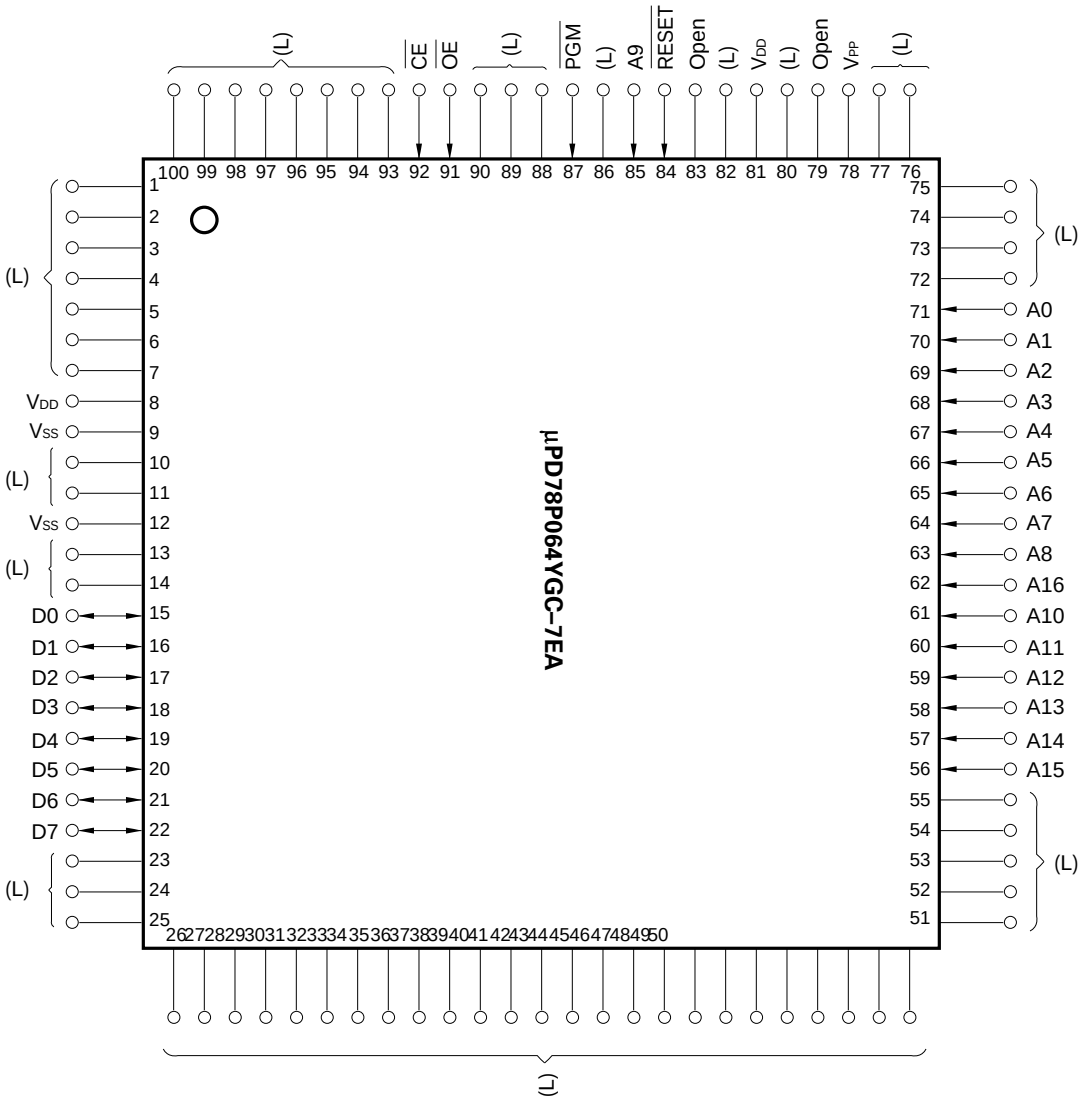
Note 1. Connect V_{PP} pin to V_{SS}.
2. Connect AV_{DD} pin to V_{DD}.
3. Connect AV_{SS} pin to V_{SS}.

P00 to P05, P07 : Port 0
P10 to P17 : Port 1
P25 to P27 : Port 2
P30 to P37 : Port 3
P70 to P72 : Port 7
P80 to P87 : Port 8
P90 to P97 : Port 9
P100 to P103 : Port 10
P110 to P117 : Port 11
INTP0 to INTP5 : Interrupt From Peripherals
TI00, TI01 : Timer Input
TI1, TI2 : Timer Input
TO0 to TO2 : Timer Output
SB0, SB1 : Serial Bus
SI0, SI2 : Serial Input
SO0, SO2 : Serial Output
SCK0, SCK2 : Serial Clock
SCL : Serial Clock
SDA0, SDA1 : Serial Data
RxD : Receive Data
TxD : Transmit Data
ASCK : Asynchronous Serial Clock
PCL : Programmable Clock
BUZ : Buzzer Clock

S0 to S39 : Segment Output
COM0 to COM3 : Common Output
V_{LC0} to V_{LC2} : LCD Power Supply
BIAS : LCD Power Supply Bias Control
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)
RESET : Reset
ANI0 to ANI7 : Analog Input
AV_{DD} : Analog Power Supply
AV_{SS} : Analog Ground
AV_{REF} : Analog Reference Voltage
V_{DD} : Power Supply
V_{PP} : Programming Power Supply
V_{SS} : Ground

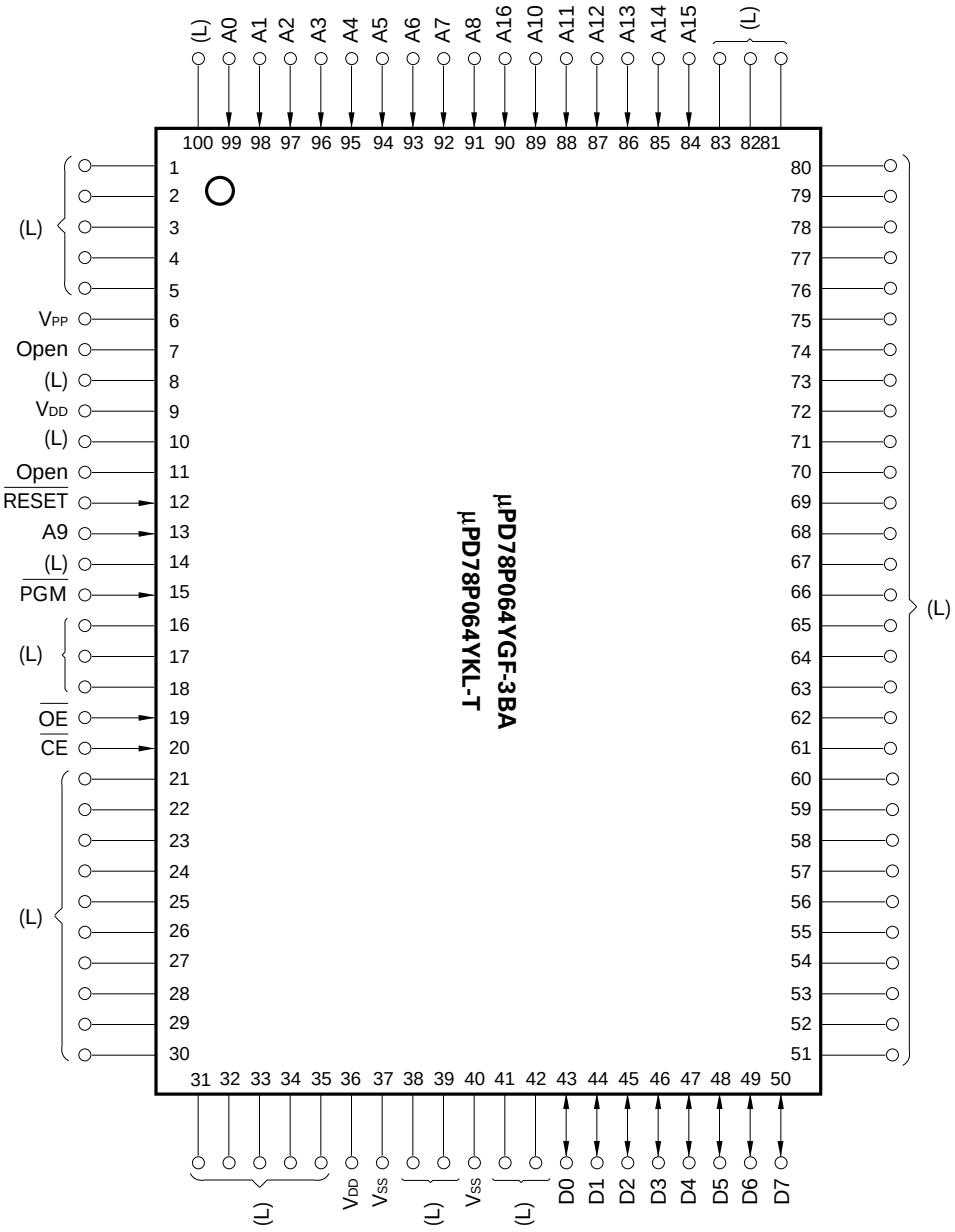
(2) PROM programming mode

100-pin plastic QFP (fine pictch)(□ 14 mm)



Note 1. (L) : Individually connect to Vss via a pull-down resistor.
2. Vss : Connect to GND.
3. RESET : Set to low level.
4. Open : No connection

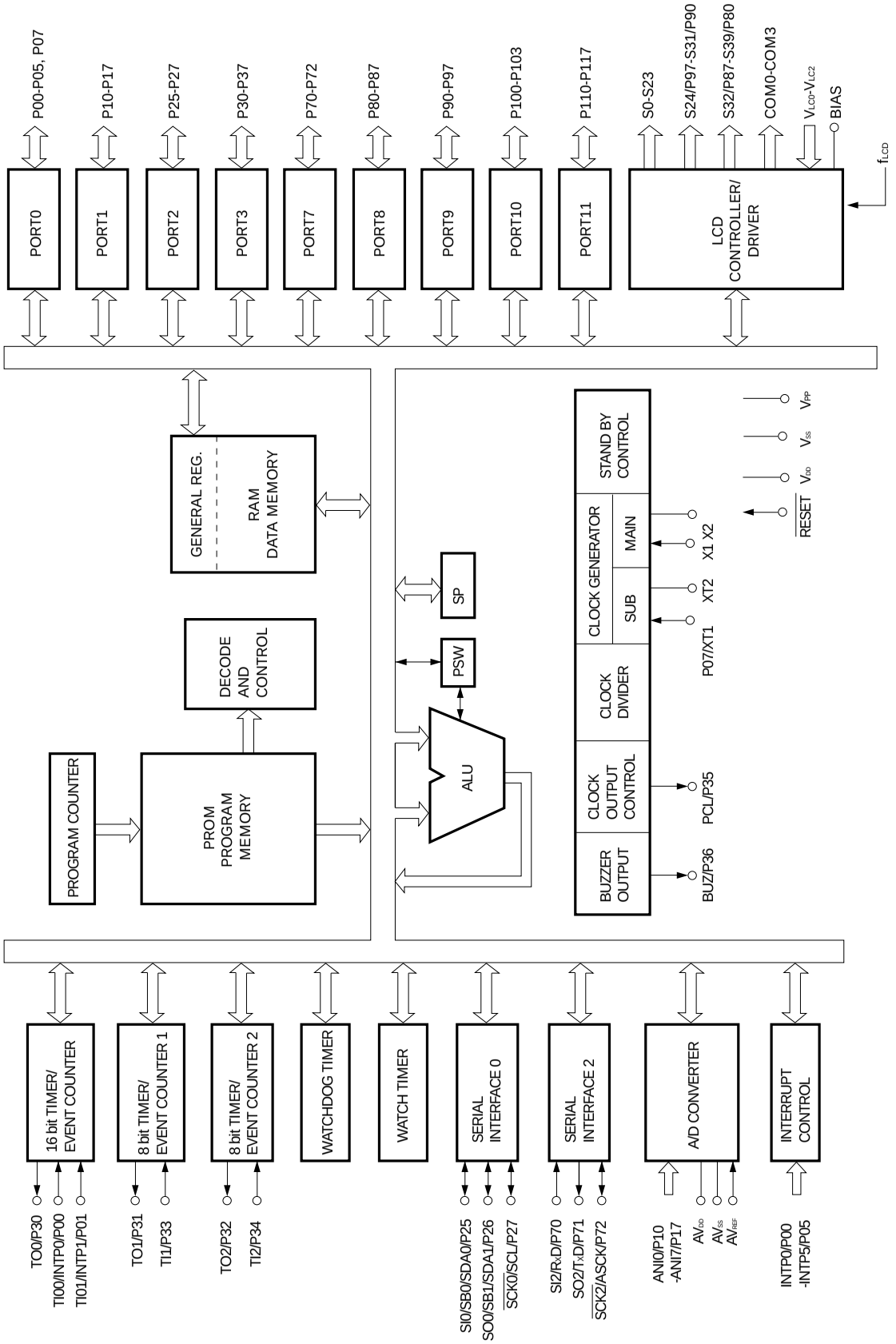
100-pin plastic QFP (14 × 20 mm)
100-pin ceramic WQFN (14 × 20 mm)



Note 1. (L) : Individually connect to Vss via a pull-down resistor.
2. Vss : Connect to GND.
3. RESET : Set to low level.
4. Open : No connection

A0 to A16	: Address Bus	RESET	: Reset
D0 to D7	: Data Bus	VDD	: Power Supply
CE	: Chip Enable	VPP	: Programming Power Supply
OE	: Output Enable	Vss	: Ground
PGM	: Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78P064Y AND MASK ROM PRODUCTS

The μPD78P064Y is a single-chip microcomputer with an on-chip one-time writable PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

It is possible to make all the functions except for PROM specification, and mask option of LCD drive power supply split resistor, to the same as those of mask ROM products by setting the memory size switching register.

Difference between the μPD78P064Y and mask ROM products are shown is Table 1-1.

Table 1-1 Differences between μPD78P064Y and Mask ROM Produts

Item	μPD78P064Y	Mask ROM Products
IC pin	No	Yes
V_{PP} pin	Yes	No
Mask option of LCD drive power supply split resistor	No	Yes

Note For the μPD78P064Y, the internal PROM/internal high-speed RAM capacities can be set by the memory size switching register.
The internal PROM becomes to 32K bytes and the internal high-speed RAM becomes 1K bytes by the RESET input.

2. LIST OF PIN FUNCTIONS

2.1 PINS WHEN NORMAL OPERATING MODE

(1) PORT PINS (1/2)

Pin Name	Input/Output	Function		After RESET	Dual-Function Pin
P00	Input	Part 0 7-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07***1**	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output is speicable bit-wise. When used as the input port, it is possibe to connenct a pull-up resister by software. ***2**		Input	ANI0 to ANI7
P25	Input/output	Port 2 3-bit input/output port. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK0}}$/SCL
P30	Input/output	Port 3 8-bit input /output port. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					——
P70	Input/output	Port 7 3-bit input /output port. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{\text{SCK2}}$/ASCK

* 1. When P07/XT1 pins are used as the input ports, the processor clock control register bit 6 should be set to 1 (the on-chip feedback register of the subsystem clock oscillation circuit should not be used.).

2. When P10/ANI0 to P17/ANI7 pins are used as the ananlog inputs for A/D converter, a pull-up resistor is not automatically used.

(1) PORT PINS (2/2)

Pin Name	Input/Output	Function	After RESET	Dual-Function Pin
P80 to P87	Input/output	Port 8 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-upresistor by software. Input/output port/segment signal output function specifiable as 2-bit unit by LCD control register.	Input	S39 to S32
P90 to P97	Input/output	Port 9 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-upresistor by software. Input/output port/segment signal output function specifiable as 2-bit unit by LCD control register.	Input	S31 to S24
P100 to P103	Input/output	Port 10 4-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-upresistor by software. It is possible to directly drive LED.	Input	——
P110 to P117	Input/output	Port 11 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-upresistor by software. Falling edge detection possible.	Input	——

(2) NON-PORT PINS (1/2)

Pin Name	Input/Output	Function	After RESET	Dual-Function Pin
INTP0	Input	External interrupt input in which valid edges (rising edge, falling edge, and both rising and falling edges) are specifiable.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial data input of the serial interface	Input	P25/SB0/SDA0
SI2				P70/RxD
SO0	Output	Serial data output of the serial interface	Input	P26/SB1/SDA1
SO2				P71/TxD
SB0	Input/output	Serial data input/output of the serial interface	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0	Input/output	Serial data input/output of the serial interface	Input	P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input/output	Serial clock input/output of the serial interface	Input	P27/SCL
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
RxD	Input	Serial data input for asynchronous serial interface	Input	P70/SI2
TxD	Output	Serial data output for asynchronous serial interface	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer output (Dual function as 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
S0 to S23	Output	LCD controller/driver segment signal output	Output	—
S24 to S31			Input	P97 to P90

(2) NON-PORT PINS (2/2)

Pin Name	Input/Output	Function	After RESET	Dual-Function Pin
S32 to S39	Output	LCD controller/driver segment signal output	Input	P87 to P80
COM0 to COM3	Output	LCD controller/driver common signal output	Output	—
V_{LC0} to V_{LC2}	—	LCD drive voltage	—	—
BIAS	—	LCD drive power supply	—	—
ANI0 to ANI7	Input	Analog input of A/D converter	Input	P10 to P17
AV_{REF}	Input	Reference voltage input of A/D converter	—	—
AV_{DD}	—	Analog power supply of A/D converter Should be connected to V_{DD}	—	—
AV_{SS}	—	Ground potential of A/D converter Should be connected to V_{SS}	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Main system clock oscillation crystal connection	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{PP}	—	High-voltage applied during program write/ verification. Normally, connected to V_{SS} in operating mode	—	—
V_{SS}	—	Ground potential	—	—

2.2 PINS UNDER PROM PROGRAMMING MODE

Pin Name	Input/Output	Function
$\overline{RESET}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/ verification
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programing mode.
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.3 PIN INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, see Fig. 2-1.

Table 2-1 Type of Input/Output Circuit of Each Pin (1/2)

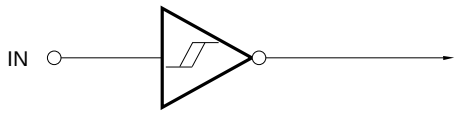
Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connecting Method when Unused
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	Input/output	Input : Connect to V_{SS}. Output: : Leave open.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connect to V_{SS}.
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
P25/SI0/SB0/SDA0	10-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P70/SI2/RxD	8-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		

Table 2-1 Type of Input/Output Circuit of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connecting Method when Unused
P80/S39 to P87/S32	17-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
P90/S31 to P97/S24	17-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
P100 to P103	5-A	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
P110 to P117	5-D	Input/output	Input : Connect to V_{DD} or V_{SS}. Output : Leave open.
S0 to S23	17	Output	Leave open
COM0 to COM3	18		
V_{LC0} to V_{LC2}	——	——	
BIAS			
$\overline{\text{RESET}}$	2	Input	——
XT2	16	——	Leave open
AV_{REF}	——		Connect to V_{SS}
AV_{DD}			Connect to V_{DD}
AV_{SS}			Connect to V_{SS}
V_{PP}			

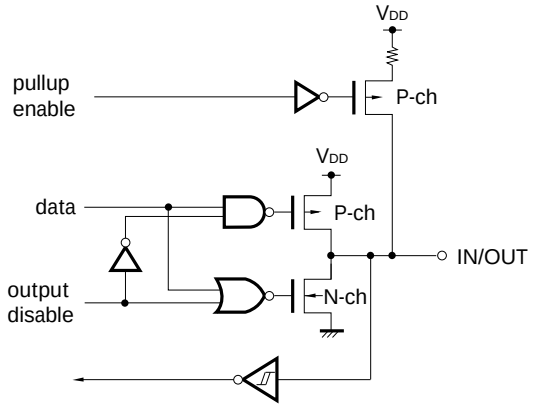
Fig. 2-1 List of Pin Input/Output Circuits (1/2)

Type 2

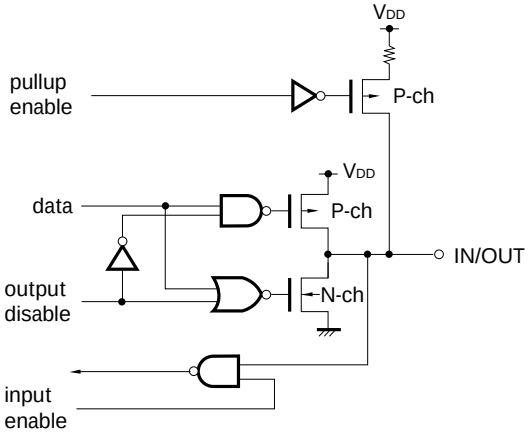


Schmitt-Trigger Input with Hysteresis Characteristic

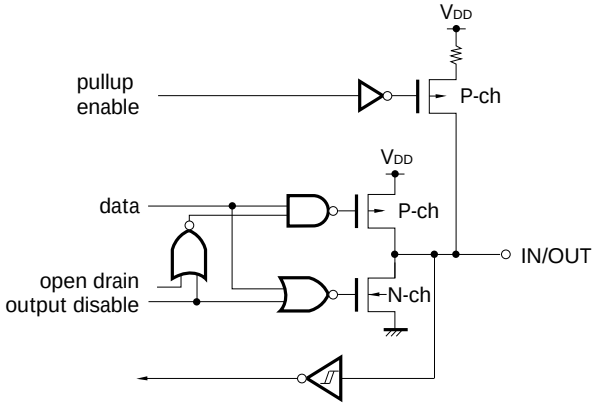
Type 8-A



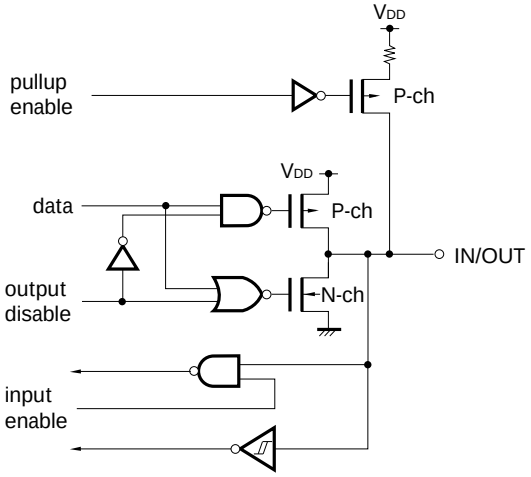
Type 5-A



Type 10-A



Type 5-D



Type 11

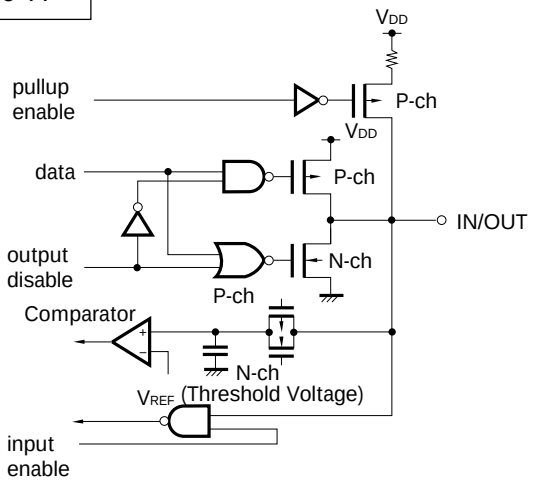
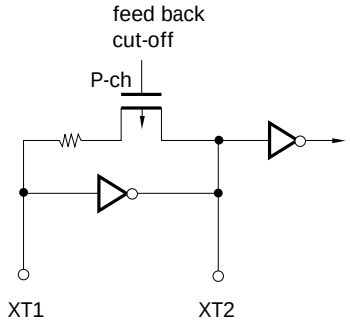
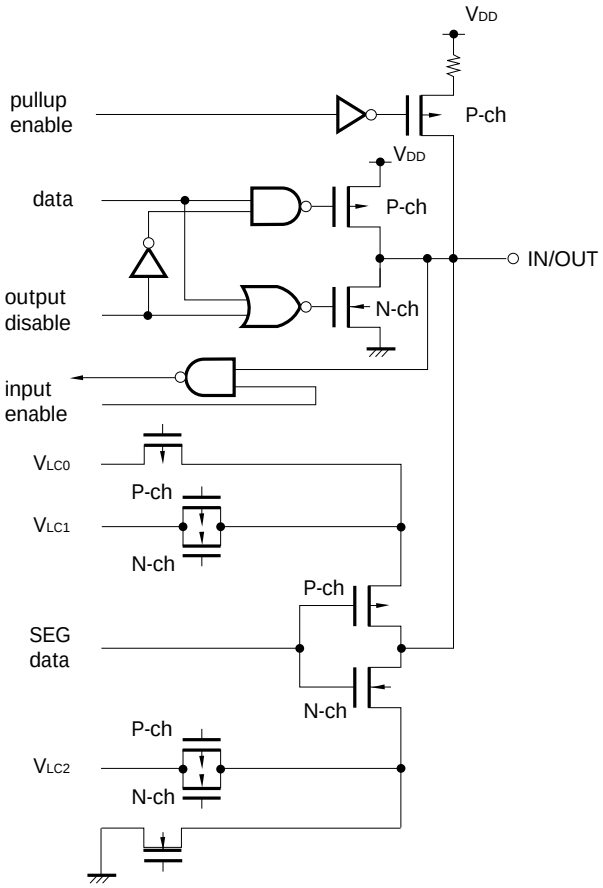


Fig. 2-1 List of Pin Input/Output Circuits (2/2)

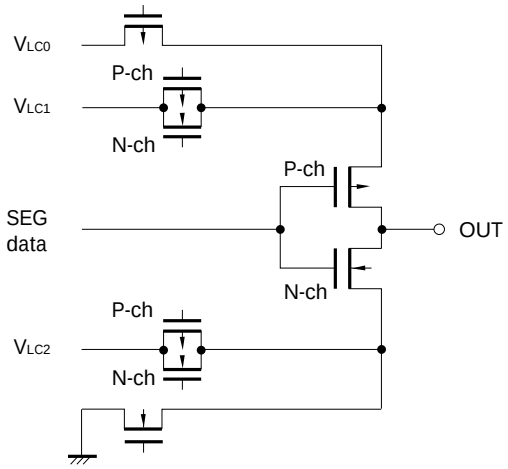
Type 16



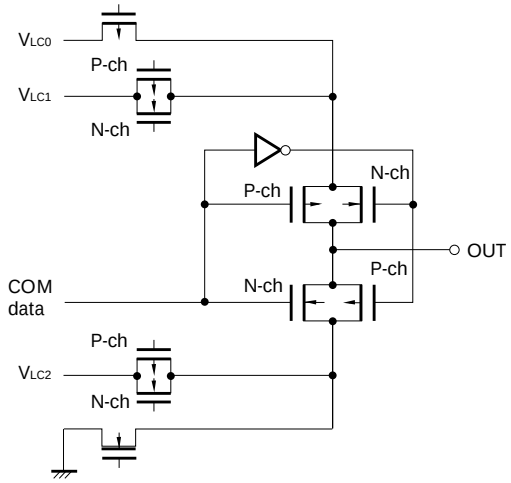
Type 17-A



Type 17



Type 18



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of mask ROM product having different internal memories (ROM, RAM).

The IMS is set up by the 8-bit memory manipulation instruction.

C8H will result by the $\overline{\text{RESET}}$ input.

Fig. 3-1 Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	0	0	16K bytes
0	1	1	0	24K bytes
1	0	0	0	32K bytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the set values of IMS which makes the memory map the same as that of the various mask ROM products.

Table 3-1 Memory Size Switching Register Setting Examples

Target Mask ROM Product	IMS Setting Value
μPD78062Y	44H
μPD78063Y	C6H
μPD78064Y	C8H

4. PROM PROGRAMMING

The μPD78P064Y has an on-chip 32K-byte PROM as a program memory. For programming, set the PROM programming mode by the V_{PP} and $\overline{RESET}$ pins. For processing unused pins, refer to "**PIN CONFIGURATION (2) PROM programming mode**."

4.1 OPERATING MODES

When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 4-1 Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

Remarks ×: L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P064Ys are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X - 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X - 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set. In this mode, check if a write operation is performed correctly, after the write.

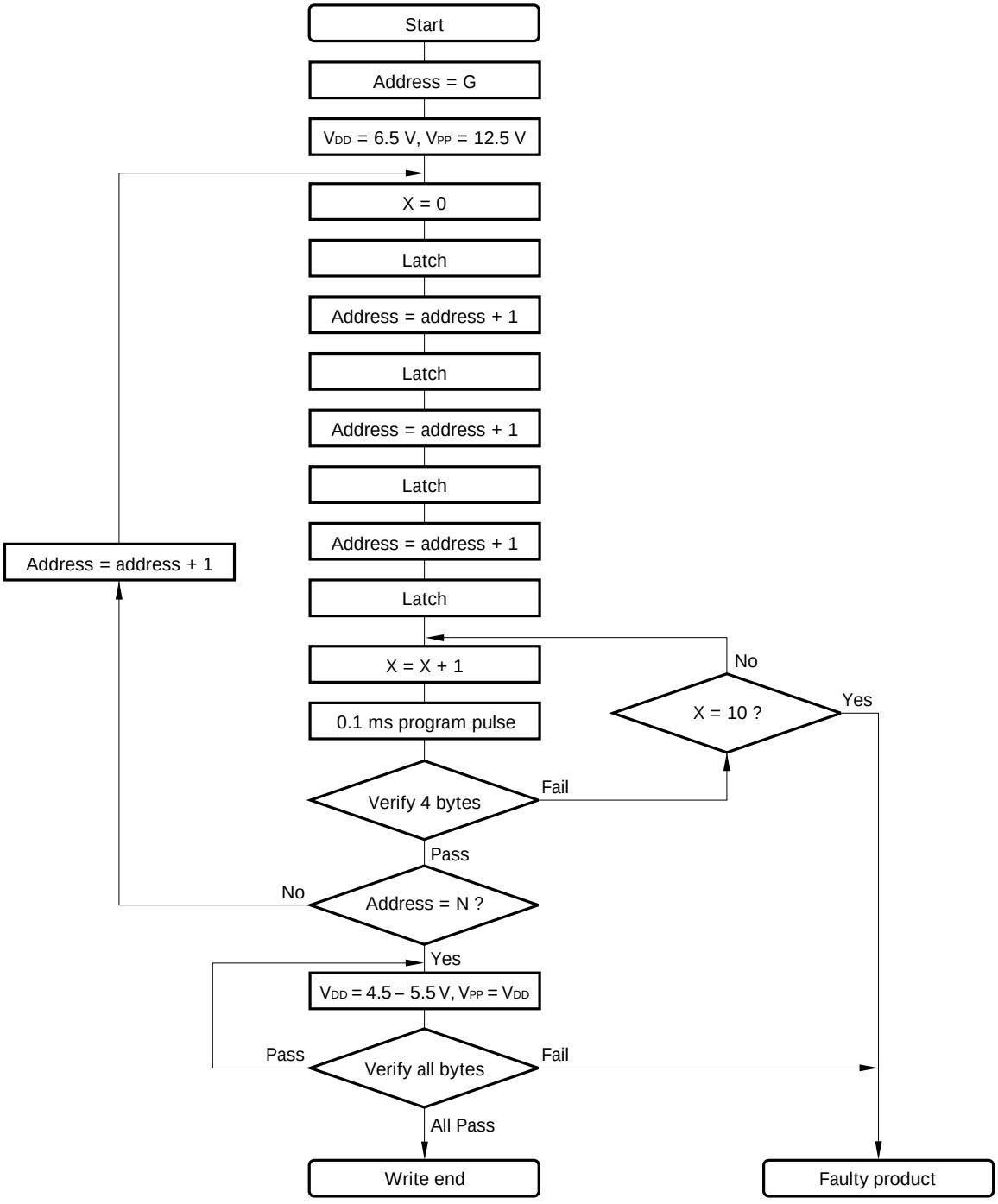
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins of multiple μPD78P064Ys are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

4.2 PROM WRITE PROCEDURE

Fig. 4-1 Page Program Mode Flow Chart



Remarks **1.** G = Start address
2. N = Program last address

Fig. 4-2 Page Program Mode Timing

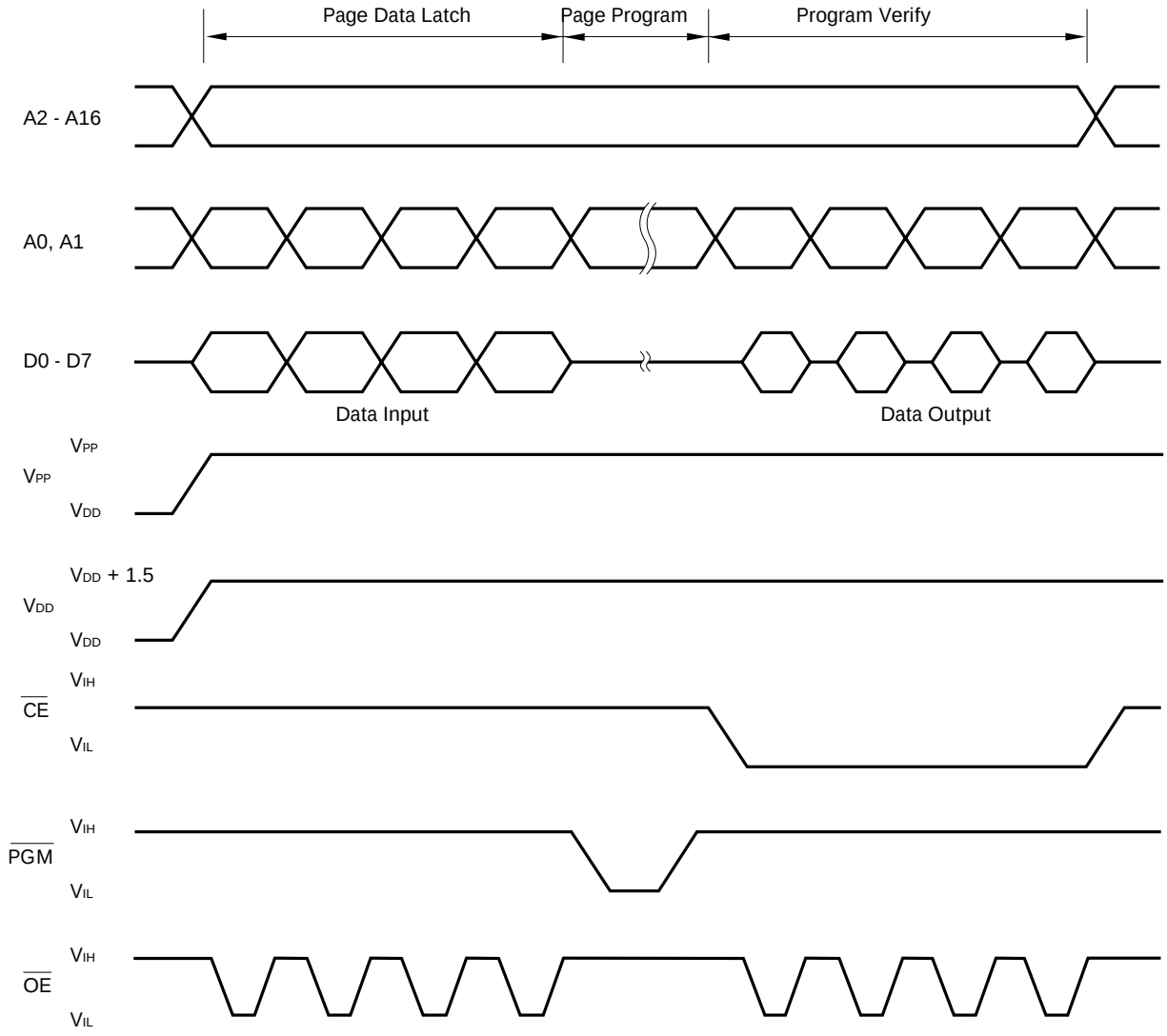
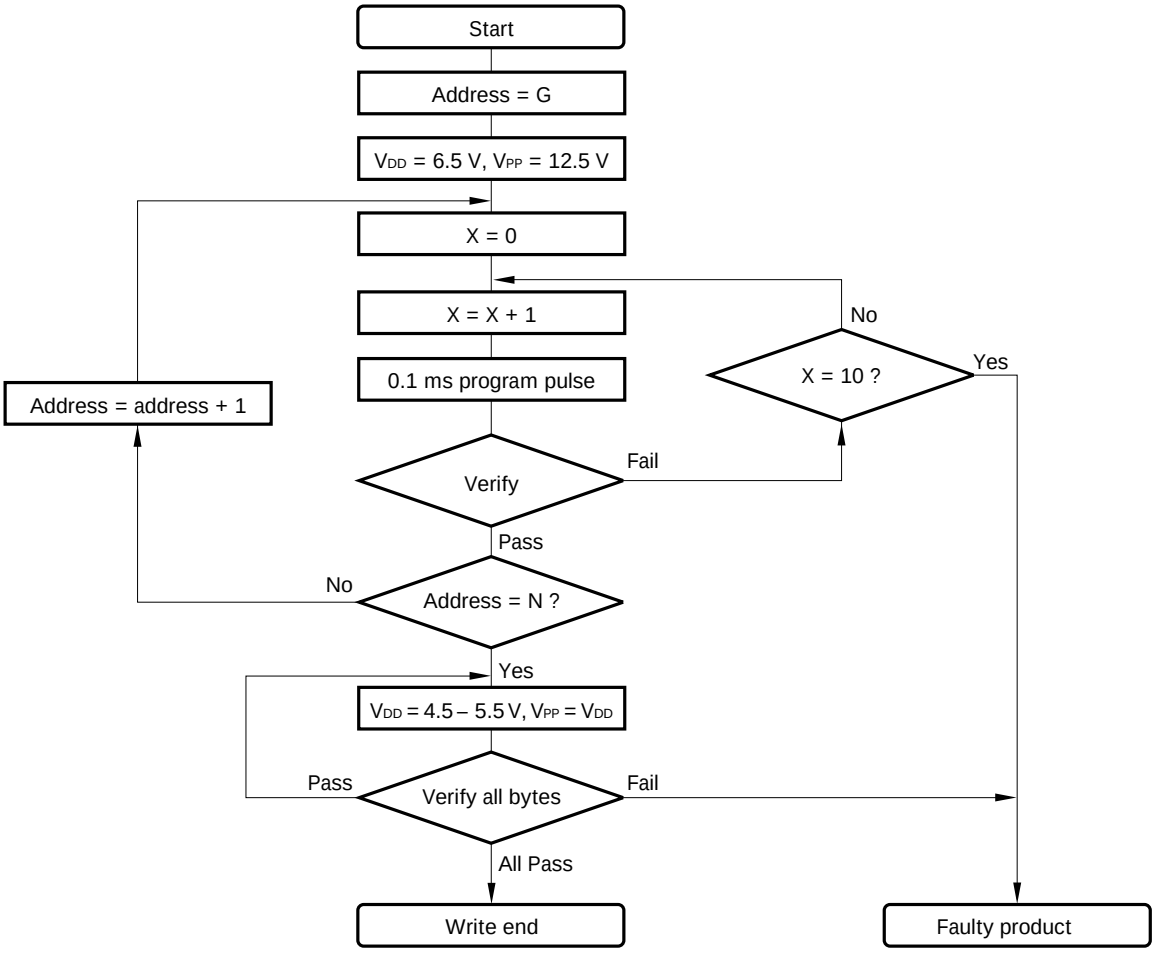


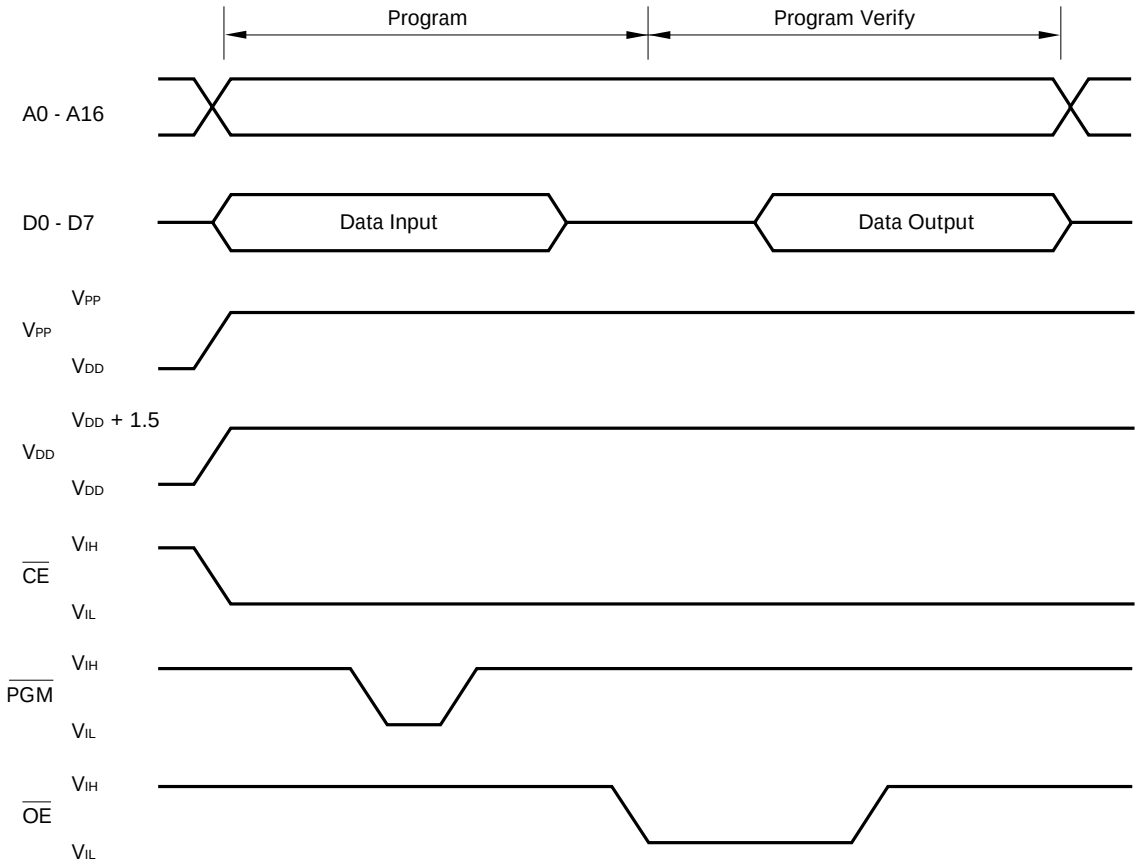
Fig. 4-3 Byte Program Mode Flow Chart



Remarks 1. G = Start address

2. N = Program last address

Fig. 4-4 Byte Program Mode Timing



Note 1. V_{DD} should be applied before V_{PP} and cut after V_{PP}.
2. V_{PP} must not exceed +13.5 V including overshoot.
3. Reliability may be adversely affected of removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

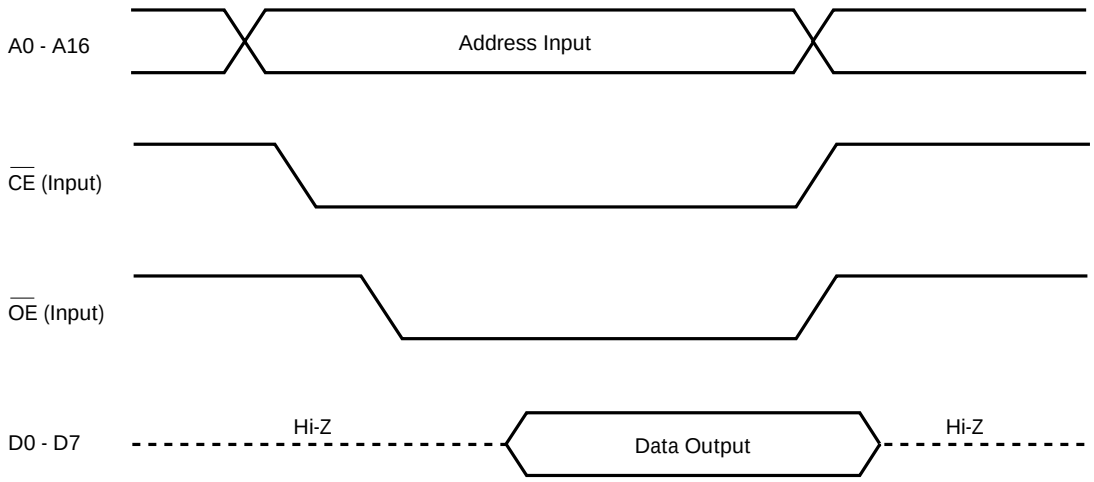
4.3 PROM READ PROCEDURE

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and process all other unused pins as shown in "**PIN CONFIGURATION (2) PROM programming mode**".
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of read data into the A0 to A16 pins.
(4) Read mode
(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Fig. 4-5.

Fig. 4-5 PROM Read Timings



5. ERASURE METHOD (μPD78P064YKL-T ONLY)

The μPD78P064YKL-T is capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the contents of data, irradiate light having a wavelength of less than about 400 nm to the erasing window. Normally, irradiate ultraviolet rays of 254 nm wavelength. Volume of irradiation required to completely erase the contents of data is as follows:

- UV intensity × erasing time : 15 W•s/cm^2 or more
- Erasing time : 15 to 20 min. (When a UV lamp of 12,000 μW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasing window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

6. ERASURE WINDOW SEAL (μPD78P064YKL-T ONLY)

To protect from miserasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, stick a protection seal on the erasure window when EPROM contents erasure is not performed.

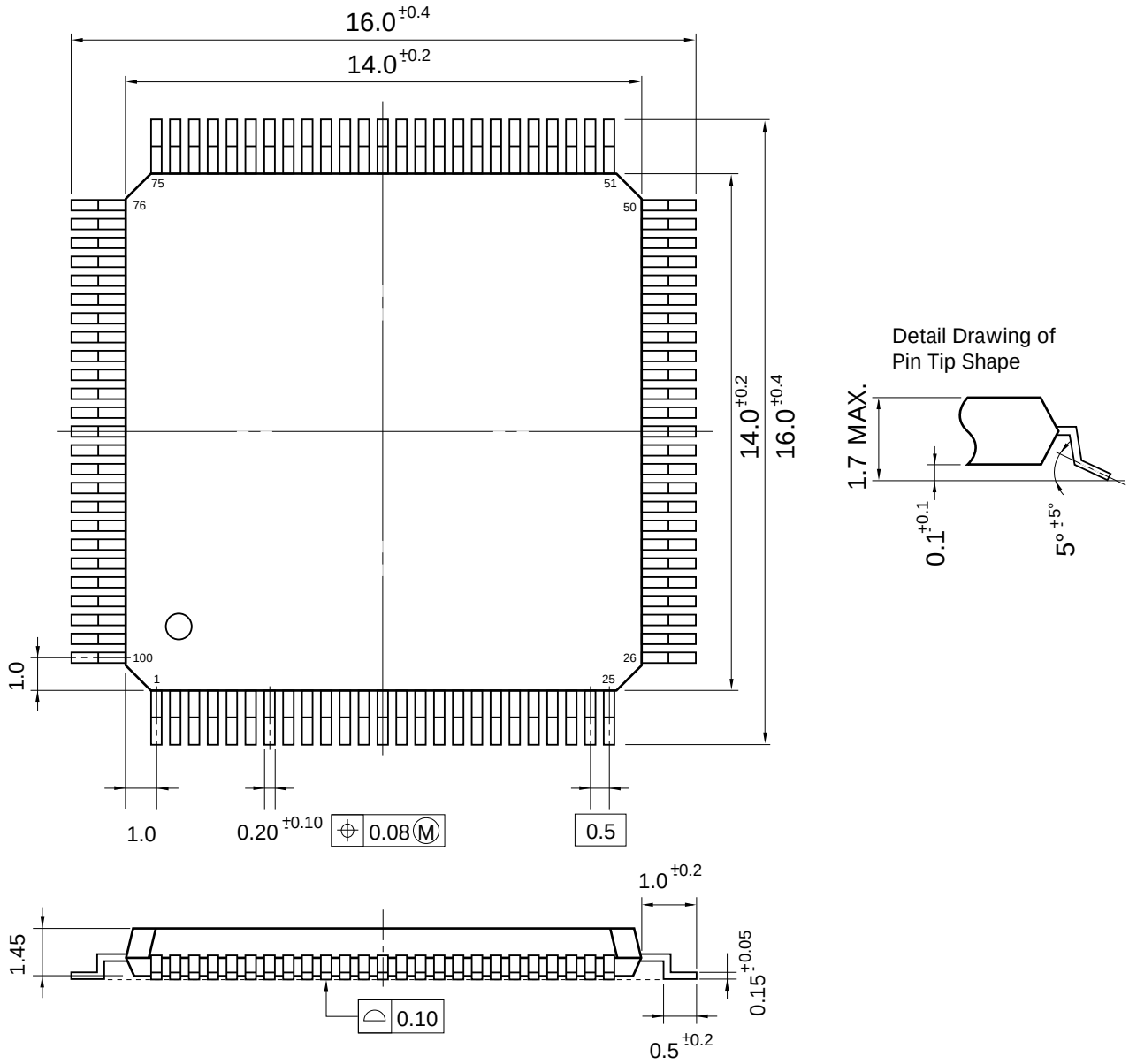
7. ONE-TIME PROM PRODUCTS SCREENING

The one-time PROM product (μPD78P064YGC-7EA, μPD78P064YGF- 3BA) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125 °C	24 hours

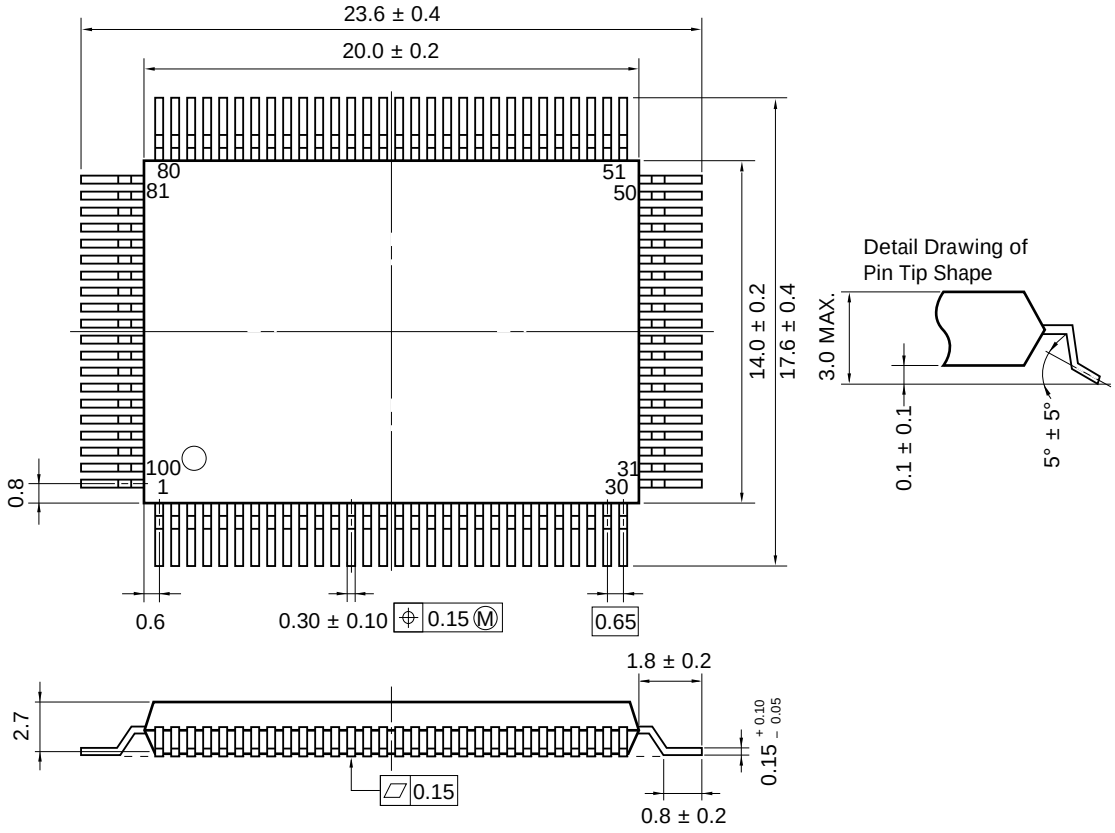
8. PACKAGE INFORMATION

100-Pin Plastic QFP (Fine Pitch) (□14) (Unit: mm)



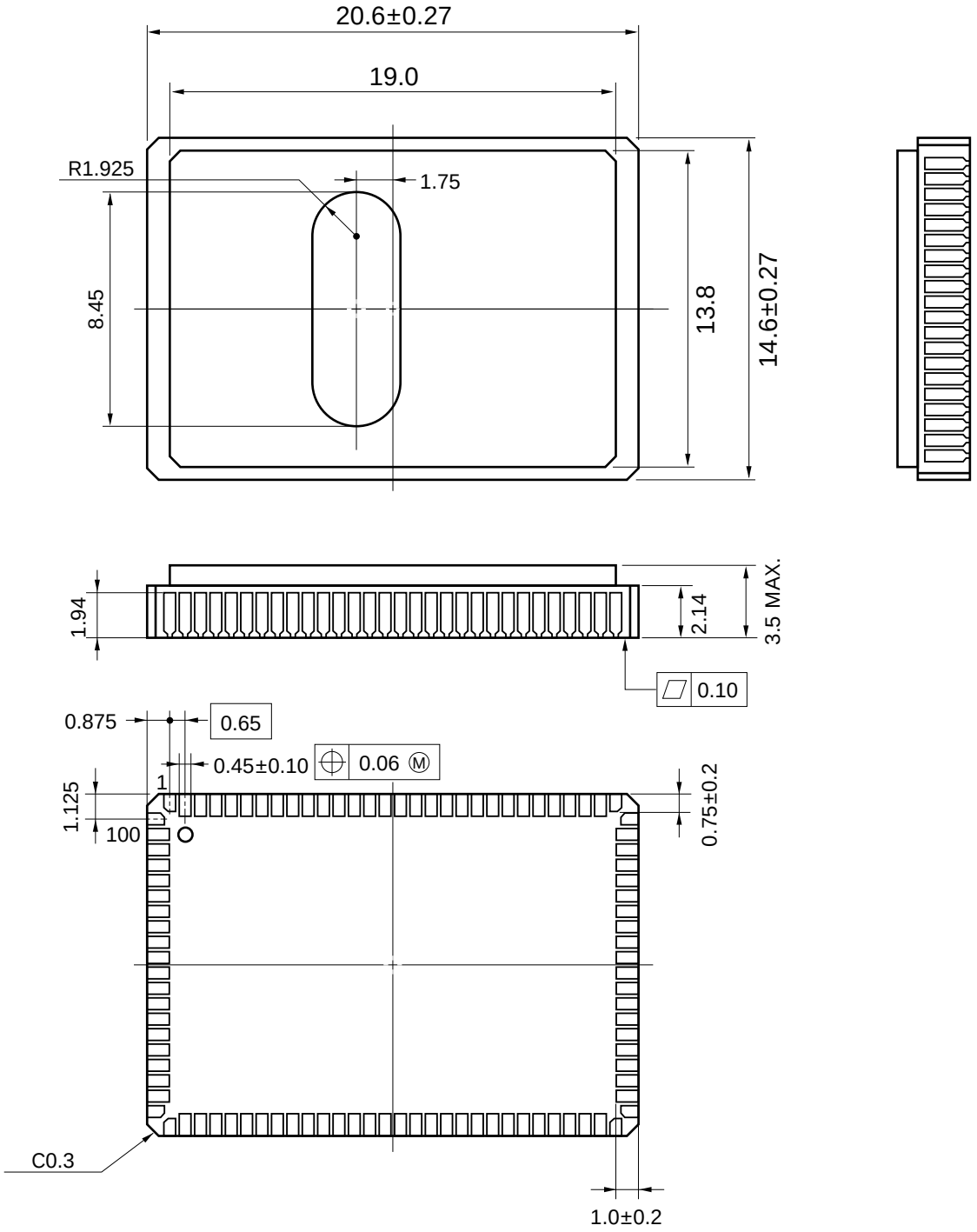
P100GC-50-7EA

100-Pin Plastic QFP (14 × 20) (Unit: mm)



P100GF-65-3BA-2

100-Pin Ceramic WQFN (Unit: mm) ★



X100KL-65A

★ APPENDIX A. DEVELOPMENT TOOLS

The following tools are available for system development using the μPD78P064Y.

Language Processing Software

RA78K/0 ***1, 2**	78K/0 series assembler package
CC78K/0 ***1, 2**	78K/0 series C-compiler package
CC78K/0-L ***1, 2**	78K/0 series C-compiler library source file

PROM Write Tools

PG-1500	PROM programmer
PA-78P064GC PA-78P064GF PA-78P064KL-T	Programmer adapter connecting to PG-1500
PG-1500 controller ***1**	PG-1500 control program

Debugging Tools

IE-78000-R	78K/0 series in-circuit emulator
IE-78000-R-BK	78K/0 series break-board
IE-78064-R-EM	μPD78064 series emulation board
EP-78064GC-R EP-78064GF-R	μPD78064 series emulation probe
EV-9500GC-100	100-pin plastic QFP adapter mounted on user system board
EV-9200GF-100	100-pin plastic QFP socket mounted on user system board
SD78K/0 ***1**	IE-78000-R screen debugger
DF78064 ***1**	μPD78064 series device file

Real-Time OS

RX78K/0 ***1, 2**	78K/0 series real-time OS

***** **1.** PC-9800 series (MS-DOS™) based, IBM PC/AT™(PC DOS™) based
2. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series™(EWS-UX/V™) based

Fuzzy Inference Development Supporting System

FE9000 ***1**	Fuzzy knowledge data creation tool
FT9080 ***1**	Translator
FI78K0 ***1**	Fuzzy inference module
FD78K0 ***1,2**	Fuzzy inference debugger

* **1.** PC-9800 series (MS-DOS) based, IBM PC/AT (PC DOS) based
2. Under development

3rd Party Development Tools

Inquiry Address	Emulator	Assembler	C-Compiler	Simulator	Debugger	Other
Advanced Data Controls Corporation (TEL : 03-3576-5351)	—	—*	● (C-cross78K0 compiler)	● (CXDB/S)	● (CSDB/E)	—
Gaio Technology Corporation (TEL : 03-3662-3041)	—	● (XASS-V)	—	● (XDEB-V)	● (XDDI-V)	—
Data I/O Japan Corporation (TEL : 03-3436-4041)	—	—	—	—	—	PROM Programmer
Lifeboat Inc. (TEL : 03-3293-4714)	—	—*	● (ICC78000)	—	—	—
Yokogawa Digital Computer Corporation (TEL : 0422-56-9101)	● (AD200)	—	—	—	● (μVIEW)	—

* Assembler is attached to C-compiler package.

APPENDIX B. RELATED DOCUMENTATION

Related Documentation for Device

Document Name	Document No.
μPD78064Y Series User's Manual	
78K/0 Series Instruction Applications List	
78K/0 Series Instruction Set	
μPD78064Y Series Special Function Register Applications List	

Related Documentation for Development Tools (User's Manual)

Document Name		Document No.
RA78K Series Assembler Package	Operation	
	Language	
RA78K Series Structured Assembler Preprocessor		
CC78K Series C-Compiler	Operation	
	Language	
CC78K Series Library Source File		
PG-1500 PROM Programmer		
PG-1500 Controller		
IE-78000-R		
IE-78000-R-BK		
IE-78064-R-EM		
SD78/K0 Screem Debugger	Primer	
	Reference	

Note The contents of the above documentation are subject to change without notice. The latest documentation must be used for design, etc.

Related Documentation for Built-In Software (User's Manual)

Document Name		Document No.
78K/0 Series Real-Time OS	Introduction	
	Installation	
	Debugger	
	Technical volume	
Fuzzy Knowledge Data Preparation Tool		
78K/0, 78/II, 87AD Series Fuzzy Inference Development Support System, Translator		
78K/0 Series, Fuzzy Inference Development Support System, Fuzzy Inference Module		
89K/0 Series, Fuzzy Inference Development Support System, Fuzzy Inference Debugger		

Other Documentation

Document Name	Document No.
Package manual	
Sirface mont technology manual	
Quality grade on NEC semiconductor devices	
NEC semiconductor device reliability & quality control	
Electrostatic discharge (ESD) test	
Semiconductor devices quality guide guarantee guide	
MIcrocomputer related products guide. Other manufactures volume	

Note The contents of the above documentation are subject to change without notice. The latest documentation must be used for design, etc.

[MEMO]

NOTE: Purchase if NEC I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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