

# Tech-Info

**Artikel:** Anschluß- und Datenblatt für  
Sharp - LM 4000 1G

**BN:** 9 8 1 2 0

Seite: 01

## Sharp Graphic Display:

Sharp LM 4000 1G ist ein Qualitäts-Display.  
400 x 64 Punkte (HxV).  
Sichtfeld 220 x 35 mm (HxV).

## Wichtiger Hinweis !

... um noch mehr aus dieser Bestellung zu machen...

## Sharp LCD Terminal Kit

Bausatz für LCD Terminal mit Sharp Display LM 4000 1G.

Bauen Sie ein Ausgabeterminal mit 6 Zeilen und 64 Zeichen, ASCII-serielle Ansteuerung 1200/ 2400/ 4800/ 9600 Baud wählbar.

Paßt an jeden Rechner mit serieller Schnittstelle.

Die Schaltung besteht aus Z 80 A Prozessorsystem mit Z 80 A SIO, sowie der Display Treiberschaltung.

Das gelieferte Betriebsprogramm enthält:

- Zeicheneintrag mit Scroll in letzter Zeile
- Cursorbewegung
- Zeichen und Zeilen, Ein- und Ausfügen
- Freie Cursorbewegung:
- Cursor Home
- Line Feed
- Carriage Return
- Löschen von Zeilen, Bildschirmresten und Clear Screen

Bestellnummer: 9 8 1 2 1 ( Display Kit Hi 950 und dazu gibt  
es noch

Bestellnummer: 9 8 1 2 2 ( Spezialbauteile für Bausatz Hi 950-  
CRT- Controller / Quarz )

Preise: BN 98 121 DM 98,-- und BN 98 122 DM 14,50

Wir wünschen Ihnen ein gutes Gelingen und viel Freude  
mit unserem Bausatzangebot !

1. Scope

This specification applies to the 400 x 64 Dot Matrix LCD Unit.

2. Construction and Outline

Construction: 400 x 64 full dot graphic display unit

Outline: See Fig. 8

Connection: See Fig. 8 and Table 4

*8x5 char cell for  
8 line, 20 col. disp*

3. Mechanical Specifications

Table 1

Items	Specifications	Unit
Unit outline dimensions	260(W) x 80(H) x 25(D)	mm
Effective viewing area	226(W) x 43(H)	mm
Display format	400 (W) x 64(H) full dots	-
Dot size	0.475(W) x 0.475(H)	mm
Dot spacing	0.075	mm
Dot color	Dark blue	-
Background color	White	-
Weight	Approx 250	gr

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 2

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage (Logic)	VDD-VSS	0	7.0	V	
Input voltage	VIN	0	VDD	V	
Storage temperature	Tstg	-25	+55	°C	
Operating temperature	Topr	0	+50	°C	

4.2 Electrical Characteristics

Table 3

(Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.25	V
Input signal voltage	VIN	"High" level	0.7VDD	VDD	V
		"Low" level	0	0.3VDD	V
Input leakage current	IIL	VIN = 5.0V	-	10	µA
Power dissipation	Pd	VDD=5V	-	105	mW

10.7,  
5.0  
3.5  
1.5

(Temperature compensation is built-in.)

4.3 Interface Signals

Connector used: MOLEX 5046 10A  
Compatible connector: MOLEX 5051-10

Table 4

Di

Pin No. *1	Symbol	Description	Effective Level
1	S	Scan start-up signal	"H" ✓
2	CP1	Input data latch signal	H + L H
3	CP2	Data input clock signal	H + L PCLK
4	DI1	Display data signal (Upper half of screen)	H(ON), L(OFF) Dφ
5	M	Drive waveform alternating signal	H, L MS
6	VO *2	Bias voltage for LCD drive	—
7	VDD	Power supply for logic circuit	— +V
8	VSS	Ground potential	— GND
9	DI2	Display data signal (Lower half of screen)	H(ON), L(OFF) D1
10	NC		—

(Note) \*1: For the location of Pin Nos., refer to Fig. 8.

\*2: External supply voltage between VDD and GND.  
Contrast of LCD shall be controlled from external portion by changing this voltage value.

### 4.4 Interface Timing

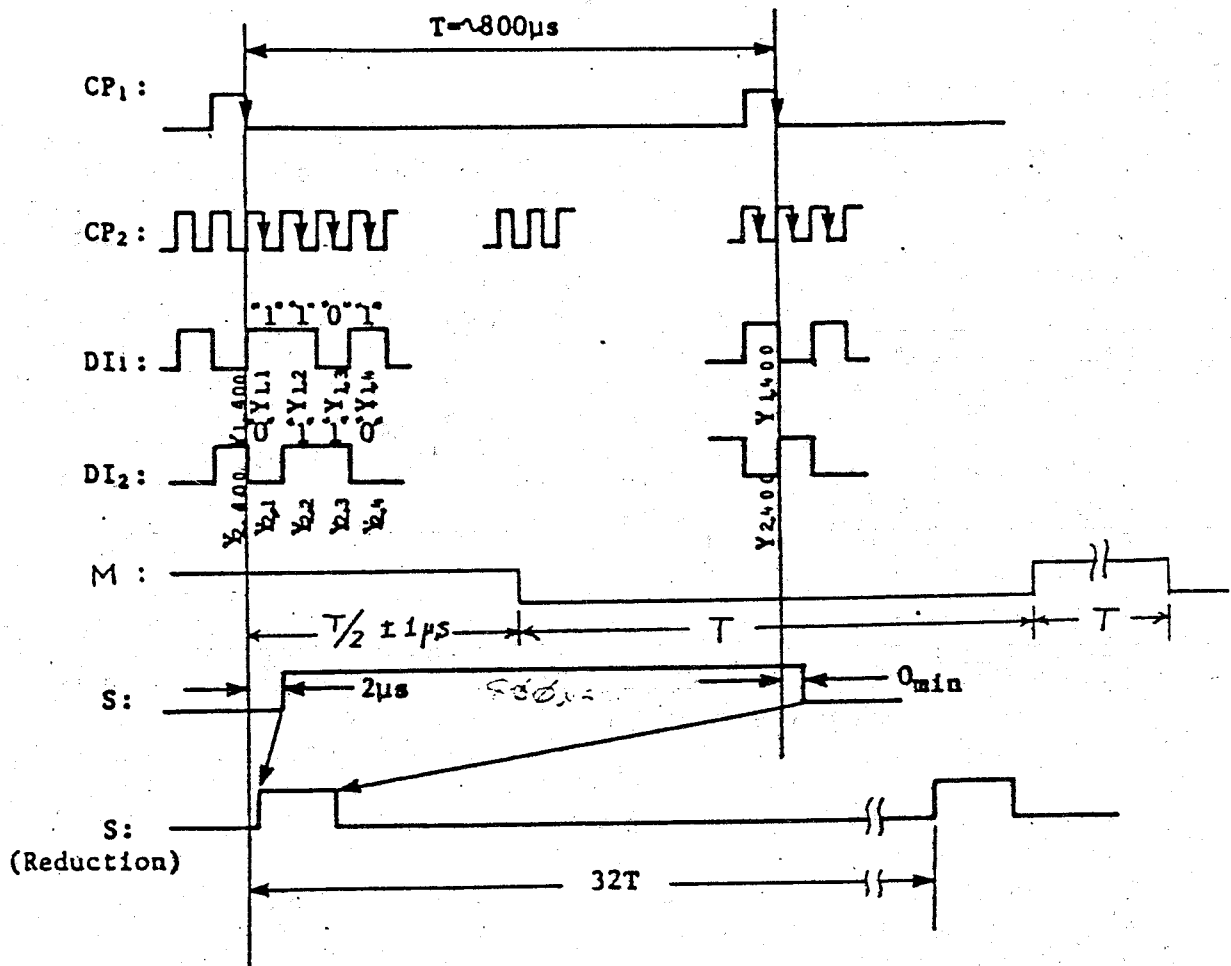


Fig. 1 Interface Timing Chart

## 5. Unit Driving Method

### 5.1. Circuit Configuration

Fig. 5 shows the block diagram of the Unit's circuitry,

### 5.2. Display Face Configuration

Because of the nature of its circuit configuration, the Unit has a two-part display face consisting of upper and lower halves, each of 400 x 32 dots. Display input data are entered at  $DI_1$  and  $DI_2$  input pins that correspond to the upper and lower halves of the display face. These two display data are input to the two parts of the display face concurrently since a set of upper and lower lines of horizontal electrodes (scan side), which correspond to the same rows of the upper and lower halves of the display face, are driven at the same time. (Thus the input pins other than  $DI_1$  and  $DI_2$  are common to the two parts of the display face.)

### 5.3. Input Data and Control Signals

Input data for the upper and lower halves of the display face, along with clock pulse  $CP_2$ , are entered at  $DI_1$  and  $DI_2$  sequentially row by row, starting from the top left of display face. This data input is implemented in the form of 1-bit serial data (high level turn off).

On the falling edge of  $CP_2$  clock, the input data is sequentially transferred via the shift register in the signal electrode driver. After one row of data (400 dots) are entered, they are latched in the form of parallel data corresponding to 400 lines of signal electrodes, then sent to the signal electrodes. At this time, scan signal  $S$  has been transferred from the scan signal driver to the lat row scan electrodes, and the contents of data signals on  $DI_1$  and  $DI_2$  pins are displayed on the 1st rows of the upper and lower halves of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the 1st rows of data are being displayed, the 2nd rows of data are entered to  $DI_1$  and  $DI_2$  pins. When 400 dots of data have been transferred then latched on the falling edge of  $CP_1$  clock, the display face proceeds to the 2nd rows of display.

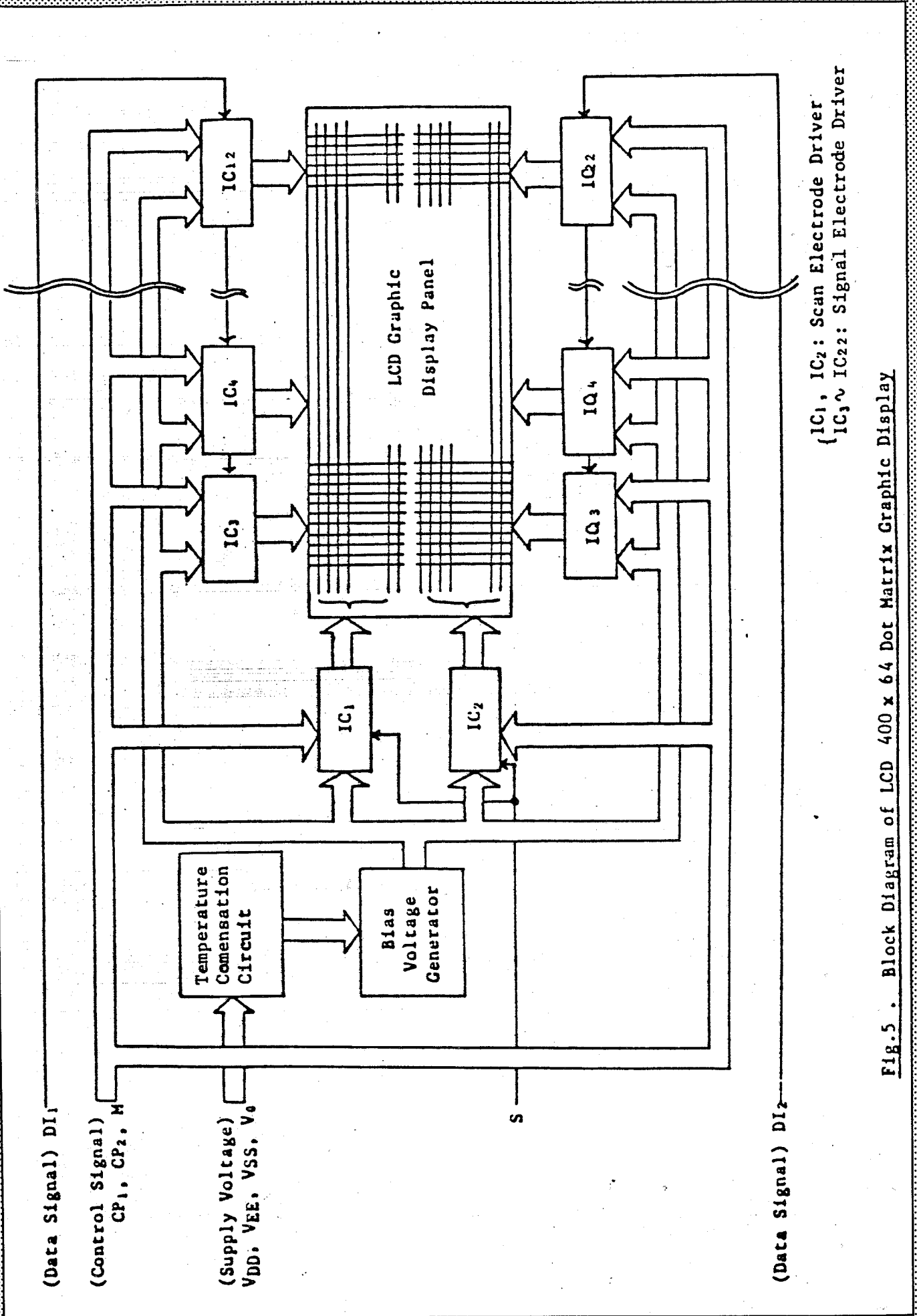
Drive waveform alternating signal  $M$  is a kind of control signal which provides alternating drive waveform necessary for prolonged operating life of the LCD by alternating the drive waveform according to its high and low levels.

This signal is that level alternates in the middle of fall of  $CP_1$  and entered with the repetitive frequency of  $1/2$  of  $CP_1$  and the waveform of  $1/2$  duty so as to alternate drive waveform during the display time of one row of data.

The display input described above is repeated up to the 32nd row to complete the whole area of display. Then data input proceeds to the next display face.

Since this Graphic Display Unit contains no refresh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals is shown in Fig. 1 .



{ IC1, IC2: Scan Electrode Driver  
 IC3, ~ IC22: Signal Electrode Driver

Fig.5 . Block Diagram of LCD 400 x 64 Dot Matrix Graphic Display