CONTENTS

1 FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a 40 lead DIP or 44 lead QFP package
- 16 kbytes ROM, expandable externally to 64 kbytes
- 256 bytes RAM, expandable externally to 64 kbytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128 kbytes external ROM up to 64 kbytes and/or RAM up to 64 kbytes
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- I^2C-bus interface for serial transfer on two lines
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8 byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8 to 6.0 V
- Frequency range of DC to 12 MHz
- Very low current consumption
- Operating temperature:
  - 83CL781: –40 to +85 °C
  - 83CL782: –25 to +55 °C.

2 GENERAL DESCRIPTION

The term P83CL781 is used throughout this data sheet to refer to both the P83CL781 and P83CL782; differences between the devices are highlighted in the text.

The P83CL781 is manufactured in an advanced CMOS technology. The instruction set of the P83CL781 is based on that of the 8051. The P83CL781 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the P85CL781 (Piggy-back version) with 256 bytes of RAM is recommended. The P83CL781 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The P83CL781 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

The P83CL782 is a faster version of the P83CL781 and operates at a maximum frequency of 12 MHz at $V_{DD} \geq 3.1$ V.

This data sheet details the specific properties of the P83CL781; for details of the P83CL781 core and all the I^2C-bus functions see *"Data Handbook IC20"*. This handbook may be ordered using the code 9398 181 30011.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL781HFP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P83CL782HDP			
P83CL781HFH	QFP44(1)	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1
P83CL782HDH			
P83CL781HFH	QFP44(1)	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
P83CL781HDH			

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

4 BLOCK DIAGRAM

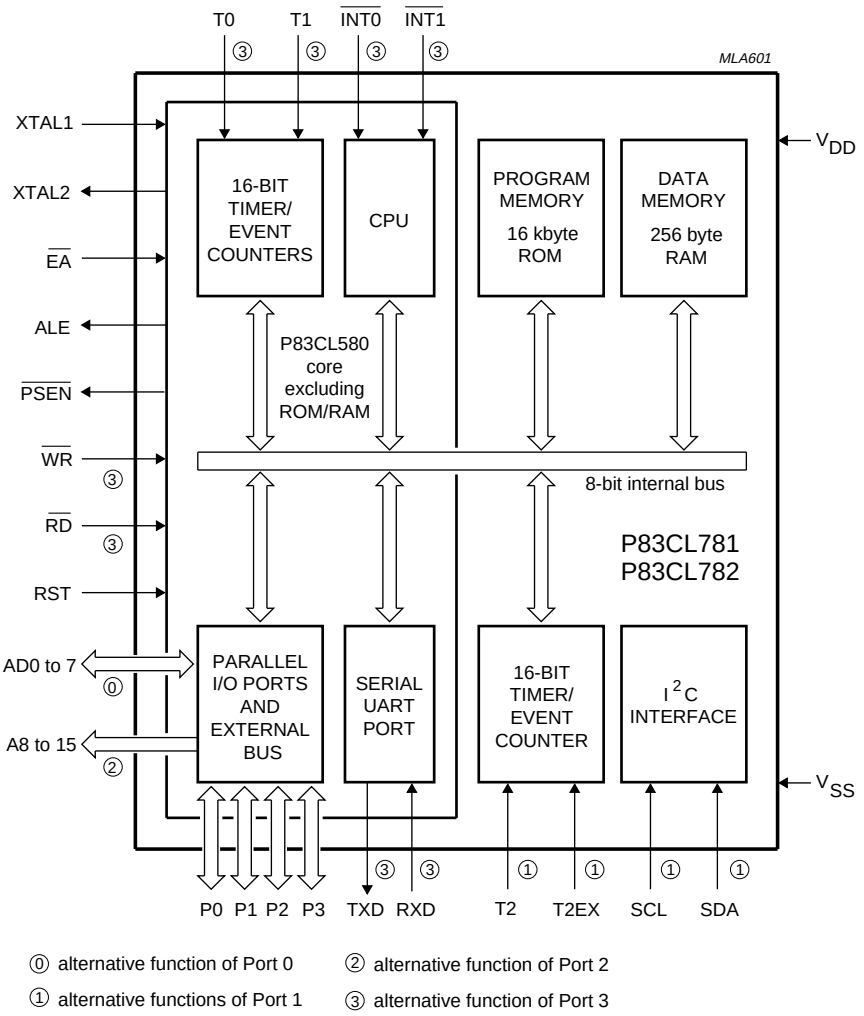

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

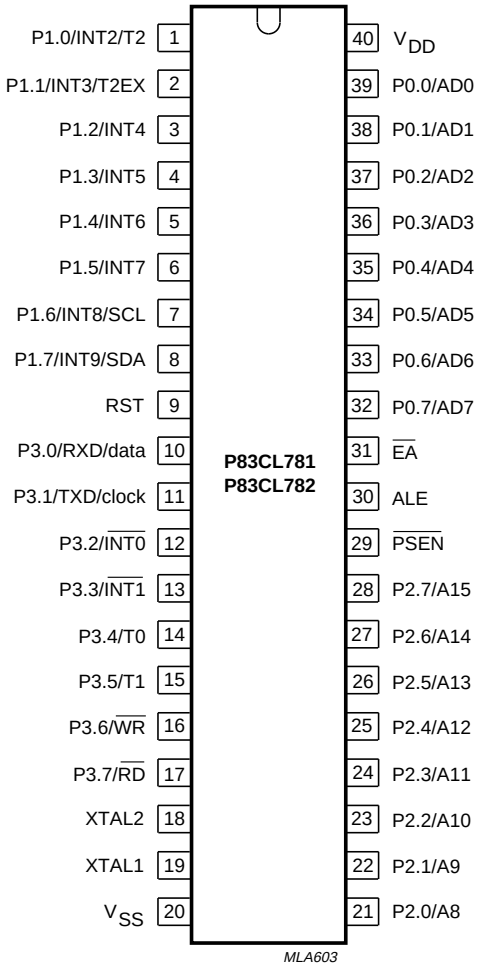

Fig.2 Pin configuration for DIP package.

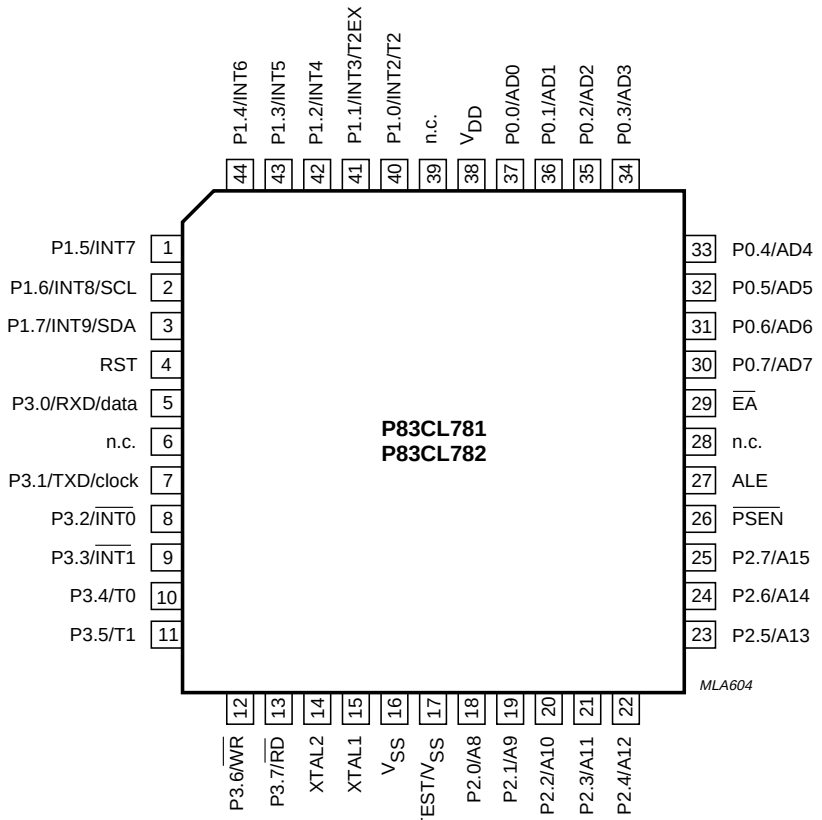

Fig.3 Pin configuration for QFP packages.

5.2 Pin description

Table 1 QFP packages (SOT205 and SOT307)

SYMBOL	PIN	DESCRIPTION
P1.0/INT2/T2	40	**Port 1:** 8-bit bidirectional I/O port with alternative functions. Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) due to the internal pull-ups. Port 1 output buffers can sink/source 4 LS TTL loads. Port 1 also serves the alternative functions INT2 to INT9 and Timer T2 external input.
P1.1/INT3/T2EX	41	
P1.2/INT4	42	
P1.3/INT5	43	
P1.4/INT6	44	
P1.5/INT7	1	
P1.6/INT8/SCL	2	
P1.7/INT9//SDA	3	
RST	4	**Reset:** A HIGH level on this pin for two machine cycles while the oscillator is running, resets the device.
n.c.	6	Not connected.
P3.0/RXD/data	5	**Port 3:** 8-bit bidirectional I/O port with alternative functions. Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, port pins that are externally pulled LOW will source current (I_{IL}) due to the internal pull-ups. Port 3 output buffers can sink/source 4 LS TTL loads. RXD/data is the serial port receiver data input (asynchronous) or data I/O (synchronous). TXD/clock is the serial port transmitter data output (asynchronous) or clock output (synchronous). $\overline{INT0}$ and $\overline{INT1}$ are external interrupt lines. T0 and T1 are external inputs for Timer 0 and Timer 1 respectively. $\overline{WR}$ is the external memory write strobe and $\overline{RD}$ is the external memory read strobe.
P3.1/TXD/clock	7	
P3.2/$\overline{INT0}$	8	
P3.3/$\overline{INT1}$	9	
P3.4/T0	10	
P3.5/T1	11	
P3.6/$\overline{WR}$	12	
P3.7/$\overline{RD}$	13	
XTAL2	14	**Crystal Output:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
XTAL1	15	**Crystal Input:** Input to the inverting amplifier that forms the oscillator, also the input for an externally generated clock source.
V_{SS}	16	**Ground:** Circuit ground potential.
TEST/V_{SS}	17	**Test Input:** Must be connected to V_{SS} or left open.
P2.0/A8	18	**Port 2:** 8-bit bidirectional I/O port with alternative functions. Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. Port 2 output buffers can sink/source 4 LS TTL loads. Port 2 emits the high order address byte during accesses to external memory that use 16-bit addresses (MOVX@DPTR). In this application it uses the strong internal pull-ups when emitting logic 1's. During accesses to external memory that use 8-bit addresses (MOVX@Ri), Port 2 emits the contents of the P2 Special Function Register.
P2.1/A9	19	
P2.2/A10	20	
P2.3/A11	21	
P2.4/A12	22	
P2.5/A13	23	
P2.6/A14	24	
P2.7/A15	25	

SYMBOL	PIN	DESCRIPTION
$\overline{PSEN}$	26	**Program Store Enable:** Read strobe to external program memory. When executing code out of external program memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external data memory two $\overline{PSEN}$ activations are skipped.
ALE	27	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods and may be used for external timing or clocking purposes.
n.c.	28	Not connected.
$\overline{EA}$	29	**External Access:** When $\overline{EA}$ is held HIGH, the CPU executes out of the internal program memory (unless the Program Counter exceeds 3FFFH). When $\overline{EA}$ is held LOW, the CPU executes out of external program memory regardless of the value of the program counter.
P0.7/AD7	30	**Port 0:** 8-bit open drain bidirectional I/O port with alternative functions. P0.7 to P0.0 provide the 8-bit I/O port. As an open-drain output port it can sink/source 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in this state will function as high-impedance inputs. AD7 to AD0 provide the multiplexed low-order address and data bus during accesses to external memory. In this application it uses the strong internal pull-ups when emitting logic 1s.
P0.6/AD6	31	
P0.5/AD5	32	
P0.4/AD4	33	
P0.3/AD3	34	
P0.2/AD2	35	
P0.1/AD1	36	
P0.0/AD0	37	
V_{DD}	38	**Power supply**
n.c.	39	Not connected.

6 FUNCTIONAL DESCRIPTION

6.1 General

The P83CL781 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products. The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of program memory and/or up to 64 kbytes of data storage.

The P83CL781 contains a non-volatile 16 kbyte read-only program memory; a static 256 byte read/write data memory; 32 I/O lines; three 16-bit timer/event counters; a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The device has two software selectable modes of reduced activity for power reduction; Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Two serial interfaces are provided on-chip; a standard UART serial interface and an I^2C-bus serial interface. The I^2C-bus serial interface has byte orientated master and slave functions allowing communication with the whole family of I^2C-bus compatible devices.

6.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency is 12 MHz.

6.3 Memory organization

The P83CL781 has a 16 kbyte Program Memory (ROM) plus 256 bytes of Data Memory (RAM) on-chip. The device has separate address spaces for Program and Data Memory (see Fig.4). Using Ports P0 and P2, the P83CL781 can address up to 64 kbytes of external memory. The CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

6.3.1 PROGRAM MEMORY

The P83CL781 contains 16 kbytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 16 kbytes of Program Memory can be implemented in either on-chip ROM or external memory. If the $\overline{EA}$ pin is strapped to V_{DD}, then program memory fetches from addresses 0000H through to 3FFFH are directed to the internal ROM. Fetches from addresses 4000H through to FFFFH are directed to external ROM. Program Counter values greater than 3FFFH are automatically addressed to external memory regardless of the state of the $\overline{EA}$ pin.

6.3.2 DATA MEMORY

The P83CL781 contains 256 bytes of internal RAM and 34 Special Function Registers (SFRs). Figure 4 shows the internal Data Memory space divided into the lower 128 bytes the upper 128 bytes and the SFR space. Internal RAM locations 0 to 27 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The Special Function Register locations 128 to 255 bytes are only directly addressable.

6.3.3 SPECIAL FUNCTION REGISTERS

The upper 128 bytes are the address locations of the Special Function Registers. Figures 6 and 7 show the Special Function Registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 addressable locations in the SFR address space (SFRs with addresses divisible by eight).

6.4 Addressing

The P83CL781 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

The first three methods can be used for addressing destination operands. Most instructions have a ‘destination/source’ field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register Direct or Register-Indirect
- 256 bytes of internal data RAM through Direct or Register-Indirect
- Special Function Registers through Direct
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register plus Index-Register-Indirect.

The P83CL781 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

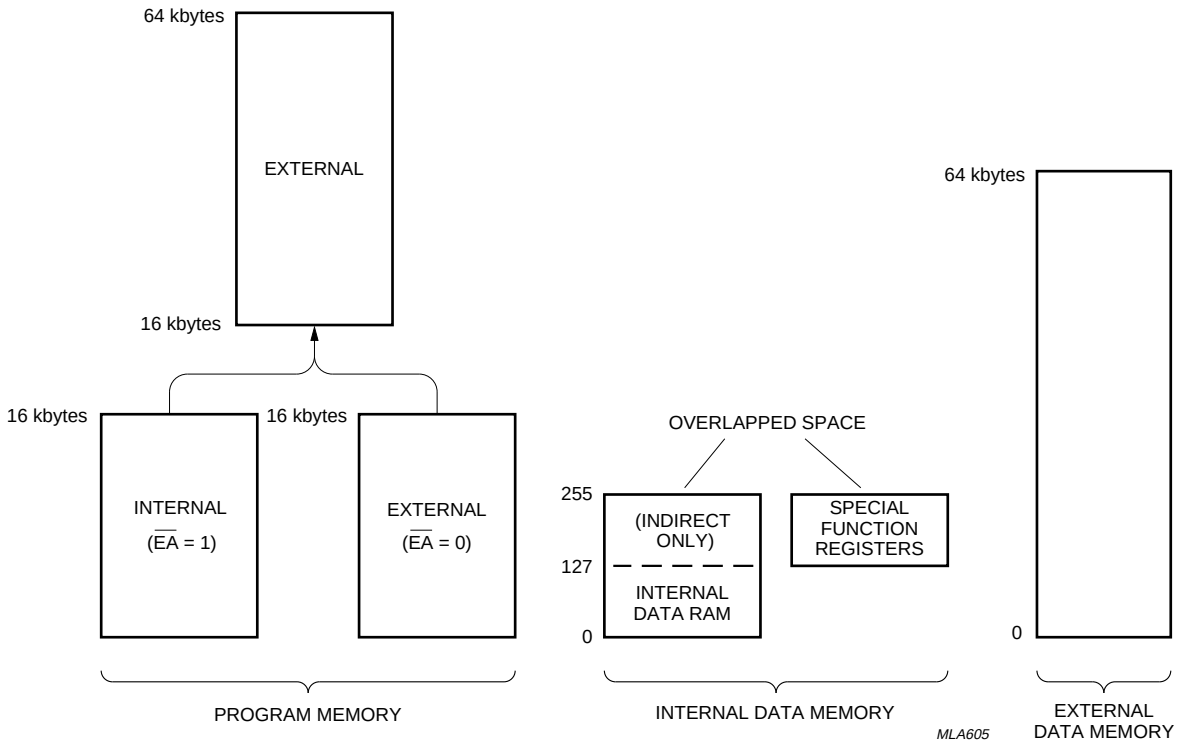

Fig.4 Memory map.

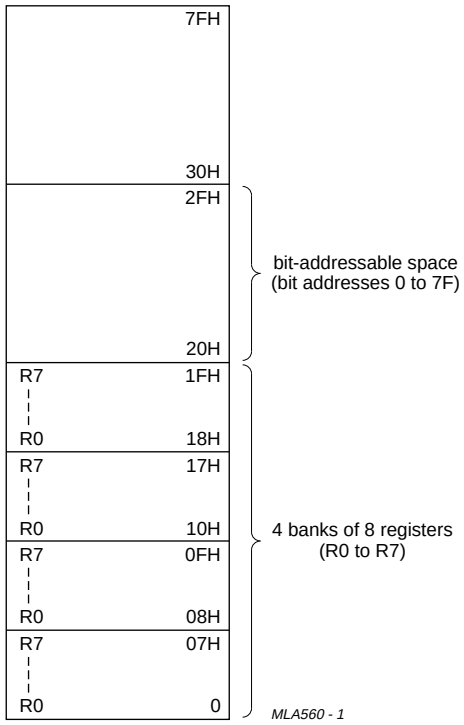

Fig.5 The lower 128 bytes of internal RAM.

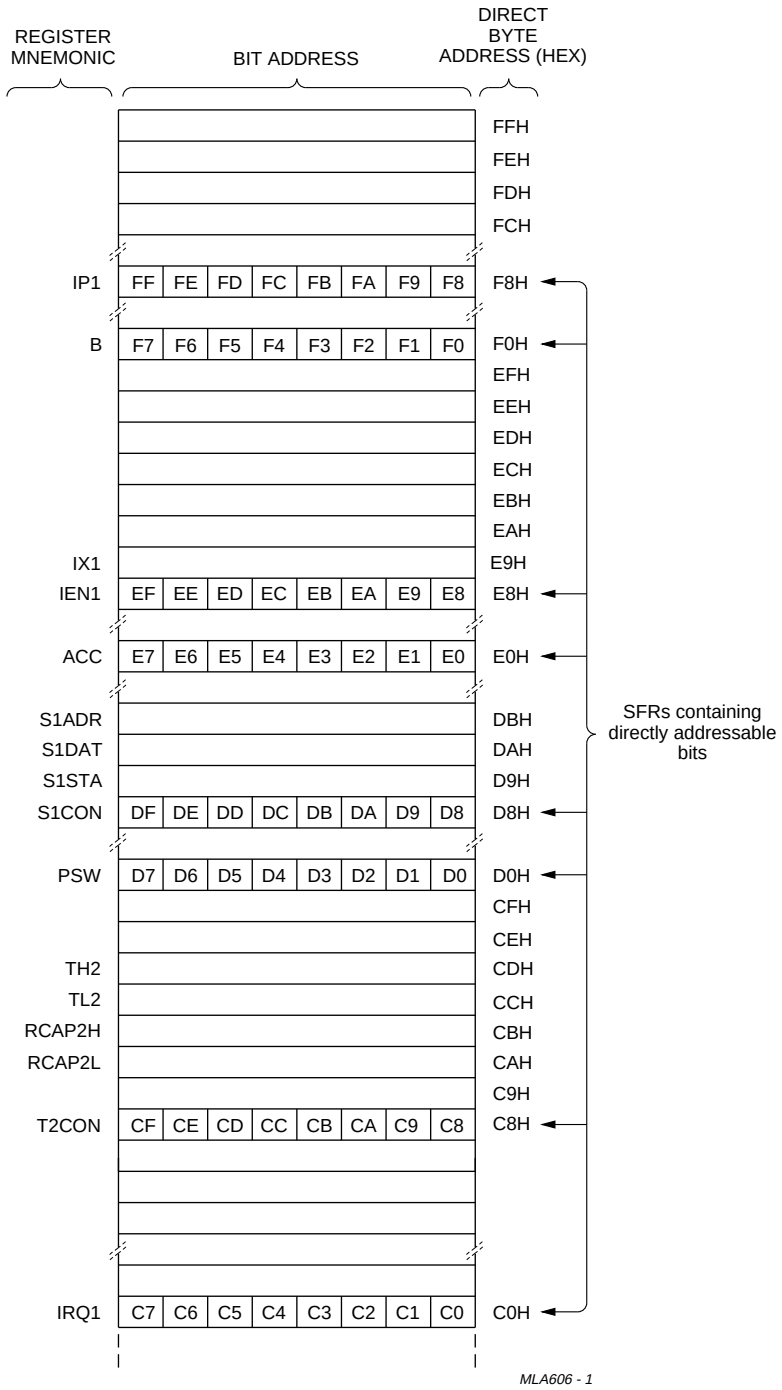

Fig.6 Special Function Register memory map (continued in Fig.7).

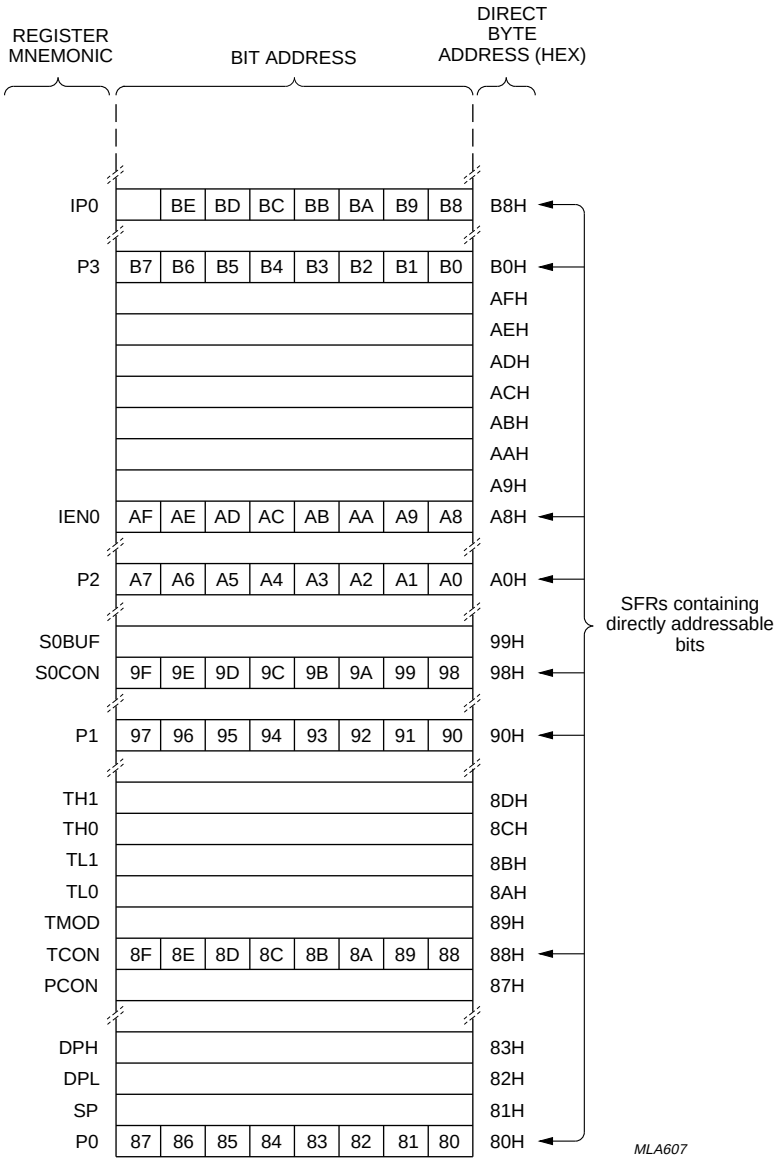

Fig.7 Special Function Register memory map (continued from Fig.6).

6.5 I/O facilities

6.5.1 PORTS

The P83CL781 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- Provides the inputs for the external interrupts INT2 to INT9
- External counter/capture of Timer 2
- SCL and SDA for the I^2C-bus interface.

Port 2 Provides the high-order address bus when expanding the device with external program memory and/or external data memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs
- Counter inputs
- Serial port receiver input and transmitter output (UART)
- Control signals to read and write to external memories.

To enable a Port 3 pin alternative function, the Port 3 bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. Ports 1, 2 and 3 have internal pull-ups. Figure 8a shows that the strong transistor p1 is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter. This inverter and p3 form a latch which holds the logic 1. In Port 0 the pull-up p1 is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 1 bit latch leaves both output transistors switched off so that the pin can be used as an high-impedance input.

6.5.2 PORT OPTIONS

30 of the 32 port pins (excluding P1.6 and P1.7 with option 2S only) may be individually configured with one of the following options. These options are also shown in Fig.8.

Option 1 Standard Port; quasi-bidirectional I/O with pull-up. The strong booster pull-up p1 is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch (see Fig.8a).

Option 2 Open drain; quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor (see Fig.8c).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option, pins can only be used as outputs (see Fig.8b).

The definition of port options for Port 0 is slightly different. Two cases are examined. First, access to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary) and second, I/O accesses.

6.5.2.1 External Memory Accesses

Option 1 True 0 and 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

6.5.2.2 I/O Accesses

Option 1 When writing a logic 1 to the port latch, the strong pull-up p1 will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open drain; quasi-directional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.8c.

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs.

Individual mask selection of the post-reset state is available with any of the above pins. The required selection is made by appending ‘R’ or ‘S’ to options 1, 2, or 3 above.

Option R RESET, after reset this pin will be initialized LOW.

Option S SET, after reset this pin will be initialized HIGH.

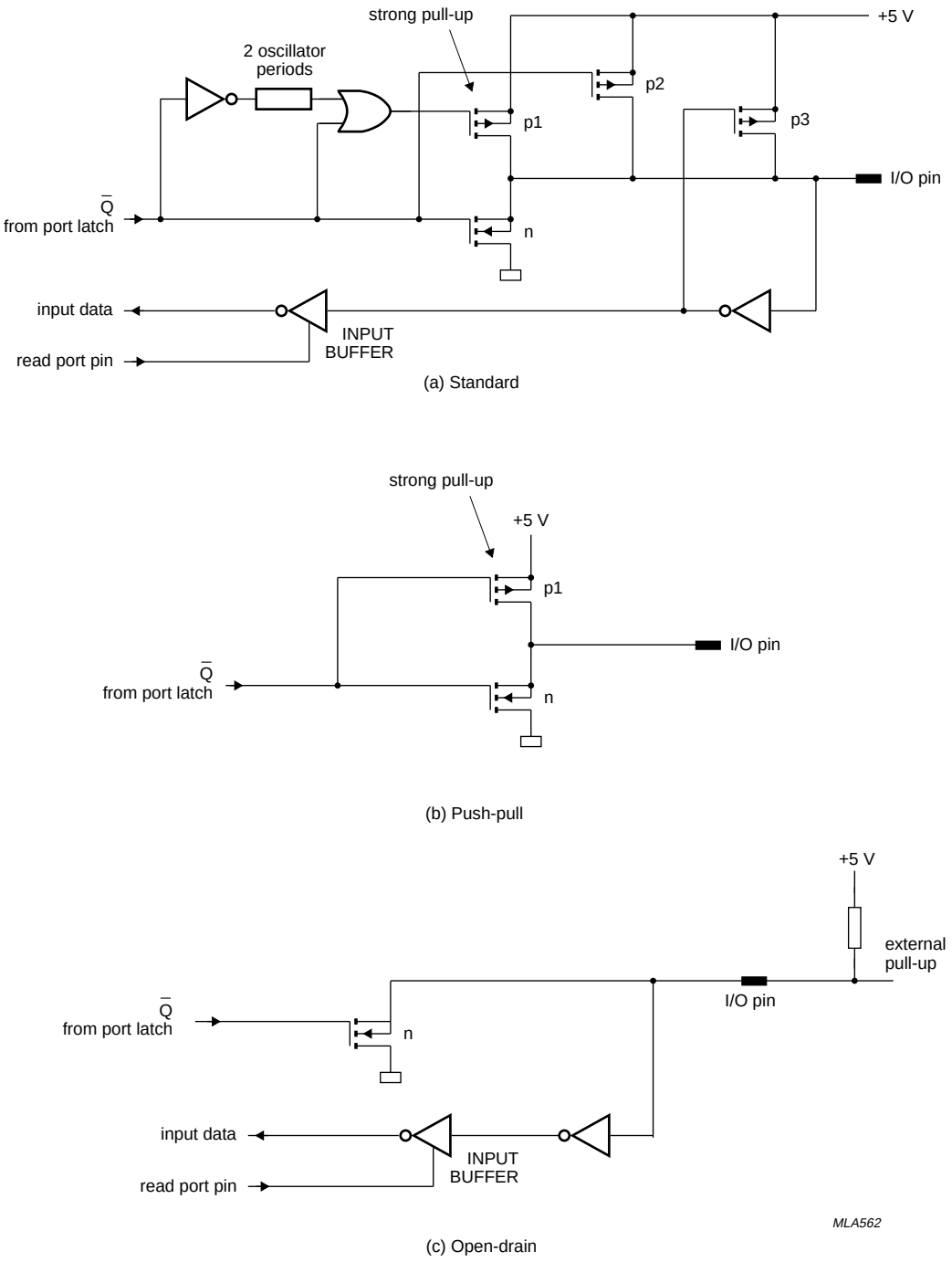

Fig.8 Port configuration options.

6.6 Timer/event counters

The P83CL781 contains three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

In the 'timer' mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $\frac{1}{12}f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{24}f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

6.6.1 TIMER T2

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Three operating modes are available Capture, Auto-Reload and Baud rate generator, these are also selected via the T2CON register.

In the Capture Mode, two options may be selected by the EXEN2 bit in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt. If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt. The Capture Mode is shown in Fig.9.

In the Auto-Reload Mode there are also two options selected by the EXEN2 bit in T2CON. If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software. If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit. The Auto-Reload Mode is shown in Fig.10.

The Baud rate generator Mode is selected when RTCLK = 1. This is described in Section 6.10.

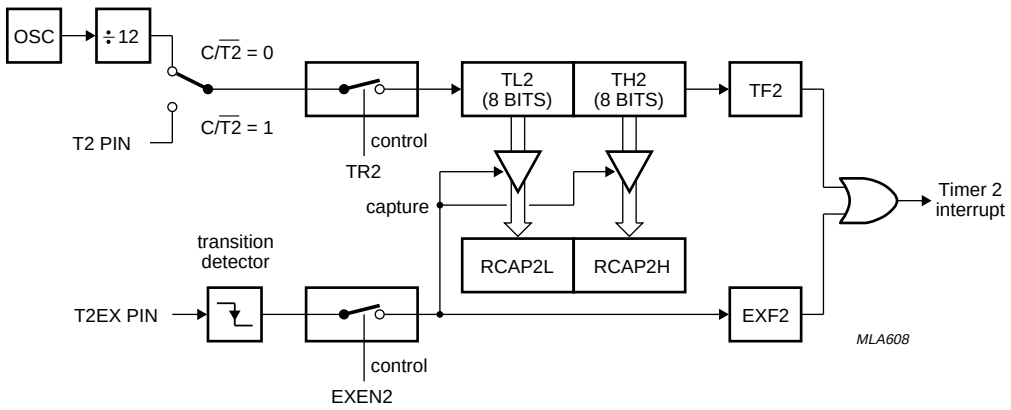

Fig.9 Timer 2 in Capture Mode.

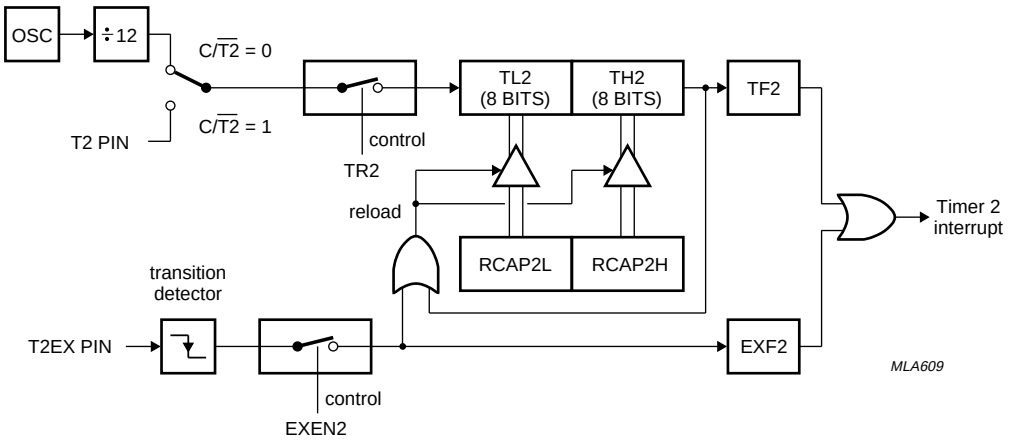

Fig.10 Timer 2 in Auto-Reload Mode.

6.6.2 TIMER/COUNTER 2 CONTROL REGISTER (T2CON)

Table 2 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	GF2	RTCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 3 Description of T2CON bits

BIT	SYMBOL	FUNCTION
T2CON.7	TF2	Timer 2 overflow flag, set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when RTCLK = 1.
T2CON.6	EXF2	Timer 2 external flag is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
T2CON.5	GF2	General purpose flag bit.
T2CON.4	RTCLK	Transmit clock flag. When set, causes the UART serial port to use Timer 2 overflow pulses for its receive and transmit clock in Modes 1 and 3. RTCLK = 0 causes Timer 1 overflows to be used for the receive and transmit clock.
T2CON.3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX, if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
T2CON.2	TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
T2CON.1	C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{12}f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
T2CON.0	CP/$\overline{RL2}$	Capture/reload flag. When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When RTCLK = 1 this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

Table 4 Timer 2 operating modes

RTCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit auto-reload
0	1	1	16-bit capture
1	X	1	baud rate generator
X	X	0	OFF

6.7 Idle and Power-down operation

Idle mode operation permits the interrupt, serial ports and timer blocks to continue to function while the clock to the CPU is halted.

The following functions remain active during the Idle mode. These functions may generate an interrupt or reset; thus ending the Idle mode.

- Timer 0, Timer 1 and Timer 2
- SIO, I^2C-bus interface
- External interrupt.

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register. The Idle and Power-down clock configuration is shown in Fig.11.

6.7.1 IDLE MODE

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 5.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T2. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

6.7.2 POWER-DOWN MODE

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and $\overline{PSEN}$ are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

6.7.3 WAKE-UP MODE

Setting the PD flag in the PCON register forces the controller into the Power-down mode. Setting this flag enables the controller to be woken-up from the Power-down mode with either the external interrupts INT2 to INT9, or a reset operation.

6.7.3.1 Wake-up using INT2 to INT9

If any of the interrupts INT2 to INT9 are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

6.7.3.2 Wake-up using RST

To wake-up the P83CL781, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted. Figure 12 illustrates the two possibilities for wake-up.

6.7.4 STATUS OF EXTERNAL PINS

The status of the external pins during Idle and Power-down mode is shown in Table 5. If the Power-down mode is activated whilst accessing external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig.8a).

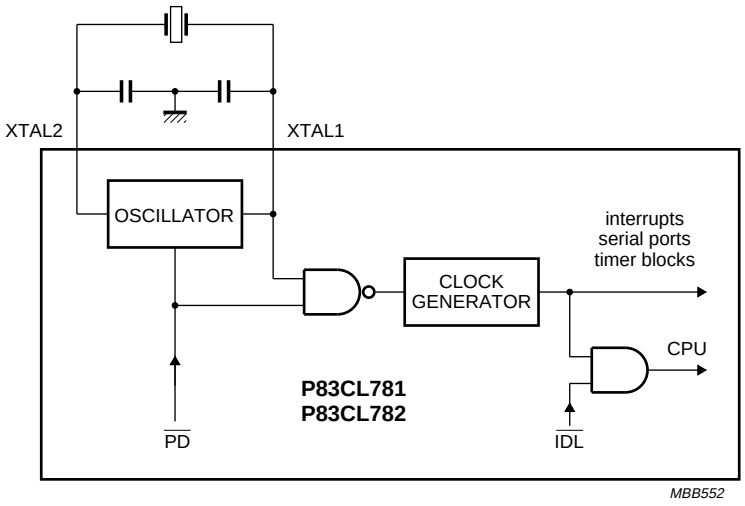

Fig.11 Internal Idle and Power-down clock configuration.

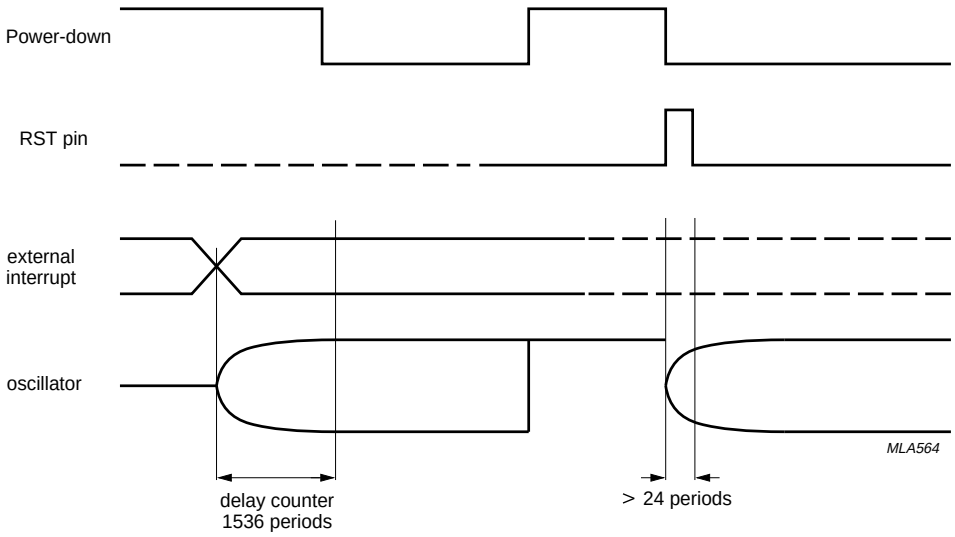

Fig.12 Wake-up operation.

Table 5 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{\text{PSEN}}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	internal	1	1	port data	port data	port data	port data
Idle	external	1	1	floating	port data	address	port data
Power-down	internal	0	0	port data	port data	port data	port data
Power-down	external	0	0	floating	port data	port data	port data

6.7.5 POWER CONTROL REGISTER (PCON)

The reduced power modes are activated by software using this Special Function Register. PCON is not bit addressable.

Table 6 Power Control Register (SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	–	GF1	GF0	PD	IDL

Table 7 Description of PCON bits.

BIT	SYMBOL	FUNCTION
PCON.7	SMOD	Double Baud rate bit. When set to a logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3.
PCON.6	–	Reserved
PCON.5	–	Reserved
PCON.4	–	Reserved
PCON.3	GF1	General purpose flag bit
PCON.2	GF0	General purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates the Power-down mode; see note 1.
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode; see note 1.

Note

1. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

6.8 I²C-bus serial I/O

The serial port supports the twin line I²C-bus. The I²C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the S1CON register. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR the Slave Address Register. Slave address recognition is performed by on-chip hardware. The block diagram of the I²C-bus serial I/O is shown in Fig.13.

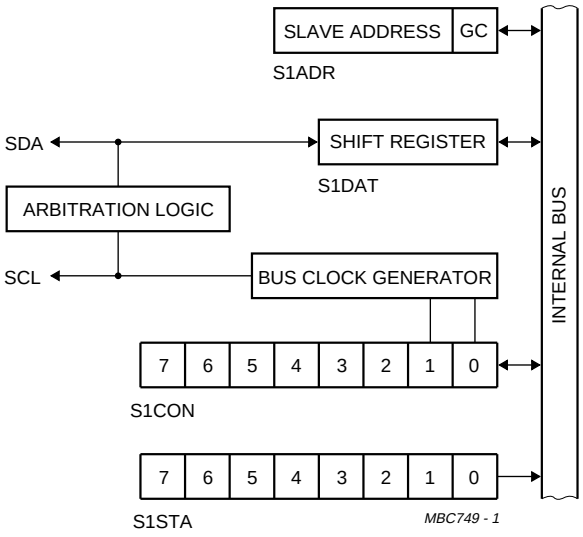

Fig.13 Block diagram of I²C-bus serial I/O.

6.8.1 SERIAL CONTROL REGISTER (S1CON)

Table 8 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 9 Description of S1CON bits

BIT	SYMBOL	FUNCTION
S1CON.7	CR2	This bit along with bits CR1 and CR0 determines the serial clock frequency when SIO is in the Master Mode. See Table 10.
S1CON.6	ENS1	ENABLE serial I/O. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high-impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
S1CON.5	STA	START flag. When this bit is set in Slave Mode, the SIO hardware checks the status of the I^2C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master Mode, SIO will generate a repeated START condition.
S1CON.4	STO	STOP flag. With this bit set while in Master Mode a STOP condition is generated. When a STOP condition is detected on the I^2C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave Mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I^2C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
S1CON.3	SI	SIO interrupt flag. This flag is set, and an interrupt is generated, after any of the following events occur: • A start condition is generated in Master Mode. • Own slave address has been received during AA = 1. • The general call address has been received while S1ADR0 and AA = 1. • A data byte has been received or transmitted in Master Mode (even if arbitration is lost). • A data byte has been received or transmitted as selected slave. • A Stop or Start condition is received as selected slave receiver or transmitter.
S1CON.2	AA	Assert Acknowledge. When this bit is set, an acknowledge (LOW level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received. • General call address is received (S1ADR.0 = 1). • A data byte is received while the device is programmed to be a Master Receiver. • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
S1CON.1	CR1	These two bits along with the CR2 bit determines the serial clock frequency when SIO is in the Master Mode. See Table 10.
S1CON.0	CR0	

Table 10 Selection of the serial clock frequency in the master mode of operation

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE (kHz) at f_{osc}		
				3.58 MHz	6 MHz	12 MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50.0	100
1	1	0	60	59.7	100	–
1	1	1	not allowed	–	–	–

6.8.2 DATA SHIFT REGISTER (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data shifted from left to right.

Table 11 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

6.8.3 ADDRESS REGISTER (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 12 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 13 Description of S1ADR bits

BIT	SYMBOL	FUNCTION
S1ADR.7 to S1ADR.1	SLA6 to 0	Own slave address.
S1ADR.0	GC	This bit is used to determine whether the general CALL address is recognized. When a logic 0, the general CALL address is not recognized. When a logic 1, the general CALL address is recognized.

6.8.4 SERIAL STATUS REGISTER (S1STA)

The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus. S1STA is a read-only register. The status codes for all possible modes of the I^2C-bus interface are given in Tables 16 to 20.

Table 14 Serial Status Register (SFR address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 15 Description of S1STA bits

BIT	SYMBOL	FUNCTION
S1STA.3 to S1STA.7	SC4 to SC0	5-bit status code.
S1STA.0 to S1STA.2	–	These three bits are held LOW.

Table 16 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
18H	SLA and W have been transmitted, ACK has been received.
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received.
28H	DATA of S1DAT has been transmitted, ACK received.
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received.
38H	Arbitration lost in SLA, R/W or DATA.

Table 17 MST/REC mode

S1STA VALUE	DESCRIPTION
38H	Arbitration lost while returning $\overline{\text{ACK}}$.
40H	SLA and R have been transmitted, ACK received.
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received.
50H	DATA has been received, ACK returned.
58H	DATA has been received, $\overline{\text{ACK}}$ returned.

Table 18 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	Own SLA and W have been received, ACK returned.
68H	Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned.
70H	General CALL has been received, ACK returned.
78H	Arbitration lost in SLA, R/W as MST. General CALL has been received.
80H	Previously addressed with own SLA. DATA byte received, ACK returned.
88H	Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned.
90H	Previously addressed with general CALL. DATA byte has been received, ACK has been returned.
98H	Previously addressed with general CALL. DATA byte has been received, $\overline{\text{ACK}}$ has been returned.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

Table 19 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	Own SLA and R have been received, ACK returned.
B0H	Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned.
B8H	DATA byte has been transmitted, ACK received.
C0H	DATA byte has been transmitted, $\overline{\text{ACK}}$ received.
C8H	Last DATA byte has been transmitted (AA = logic 0), ACK received.

Table 20 Miscellaneous

S1STA VALUE	DESCRIPTION
00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition.

Table 21 Symbols used in Tables 16 to 20

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	Read bit
W	Write bit
ACK	Acknowledgement (acknowledge bit = logic 0)
$\overline{\text{ACK}}$	No acknowledgement (acknowledge bit = logic 1)
DATA	8-bit data byte to or from I^2C-bus
MST	Master
SLV	Slave
TRX	Transmitter
REC	Receiver

6.9 Standard serial interface SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at $\frac{1}{12}$ the oscillator frequency.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first) and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $\frac{1}{32}$ or $\frac{1}{64}$ of the oscillator frequency.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

6.9.1 MULTIPROCESSOR COMMUNICATIONS

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.9.2 Serial Port Control Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON; shown in Table 22. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 22 Serial Port Control Register (SFR address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 23 Description of S0CON bits

BIT	SYMBOL	FUNCTION
S0CON.7	SM0	These two bits are used to select the serial port mode. See Table 24.
S0CON.6	SM1	
S0CON.5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid Stop bit was received. In Mode 0, SM2 should be a logic 0.
S0CON.4	REN	Enables serial reception and is set by software to enable reception, and cleared by software to disable reception.
S0CON.3	TB8	Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired.
S0CON.2	RB8	In Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
S0CON.1	TI	The transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
S0CON.0	RI	The receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (for exception see SM2). Must be cleared by software.

Table 24 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	shift register	$\frac{1}{12}f_{osc}$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$\frac{1}{64}f_{osc}$ or $\frac{1}{32}f_{osc}$
1	1	3	9-bit UART	variable

6.10 Baud rates

The baud rate in Mode 0 is fixed and may be calculated as shown below:

$$\text{Baud rate} = \frac{f_{osc}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON. If SMOD = 0, (which is the value on reset), the baud rate is $1/64$ the oscillator frequency. If SMOD = 1, the baud rate is $1/32$ the oscillator frequency. The baud rate in Mode 2 may be calculated as shown below:

$$\text{Baud rate} = \frac{2^{SMOD}}{64} \times f_{osc}$$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

6.10.1 Using Timer 1 to generate baud rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD bit as follows:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 overflow rate}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either ‘timer’ or ‘counter’ operation in any of its 3 running modes. In most typical applications, it is configured for ‘timer’ operation, in the Auto-Reload mode (high nibble of TMOD = 0010B). In this case the baud rate is given by the formula:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times f_{osc} \times \frac{1}{[12 \times (256 - TH1)]}$$

By configuring Timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rates can be achieved. Table 25 lists various commonly used baud rates and how they can be obtained from Timer 1.

Table 25 Timer 1 generated commonly used baud rates

BAUD RATE	f_{osc} (MHz)	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
Mode 0 max: 1 Mbits/s	12	X	X	X	X
Mode 2 max: 375 kbits/s	12	1	X	X	X
Modes 1 and 3: 62.5 kbit/s	12	1	0	2	FFH
19.2 kbits/s	11.059	1	0	2	FDH
9.6 kbits/s	11.059	0	0	2	FDH
4.8 kbits/s	11.059	0	0	2	FAH
2.4 kbits/s	11.059	0	0	2	F4H
1.2 kbits/s	11.059	0	0	2	E8H
137.5 kbits/s	11.986	0	0	2	1DH
110	6	0	0	2	72H
110	12	0	0	1	FEEBH

6.10.2 USING TIMER 2 TO GENERATE BAUD RATES

Timer 2 is selected as a baud rate generator by setting the RTCLK bit in T2CON. The baud rate generator mode is similar to the Auto-Reload mode, in that a roll-over in TH2 causes Timer 2 registers to be reloaded with the 16-bit value held in the registers RCAP2H and RCAP2L, which are preset by software. Baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as specified below.

$$\text{Baud rate} = \frac{\text{Timer 2 overflow rate}}{16}$$

The timer can be configured for either 'timer' or 'counter' operation. In typical applications it is configured for timer operation ($C/\overline{T2} = 0$). Timer operation is slightly different for Timer 2 when it is being used as a baud rate generator. Normally, as a timer it would increment every machine cycle at a frequency of $\frac{1}{12}f_{osc}$. However, as a baud rate generator it increments every state time at a frequency of $\frac{1}{2}f_{osc}$. In this case the baud rate is determined as specified below.

$$\text{Baud rate} = \frac{f_{osc}}{32 \times [65536 - (\text{RCAP2H;RCAP2L})]}$$

Where (RCAP2H;RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The baud rate generator mode for Timer 2 is shown in Fig.14. This figure is only valid if RTCLK = 1. At roll-over TH2 does not set the TF2 bit in T2CON and therefore, will not generate an interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the baud rate generator mode. If EXEN2 is set, a HIGH-to-LOW transition on T2EX will set the EXF2 bit, also in T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2; TL2). Therefore, in this mode T2EX may be used as an additional external interrupt.

When Timer 2 is operating as a timer (TR2 = 1), in the baud rate generator mode, registers TH2 and TL2 should not be accessed. Under these conditions the timer is being incremented every state time and therefore the results of a read or write may not be accurate. The RCAP registers however, may be read but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required Timer 2 should first be turned off by clearing the TR2 bit.

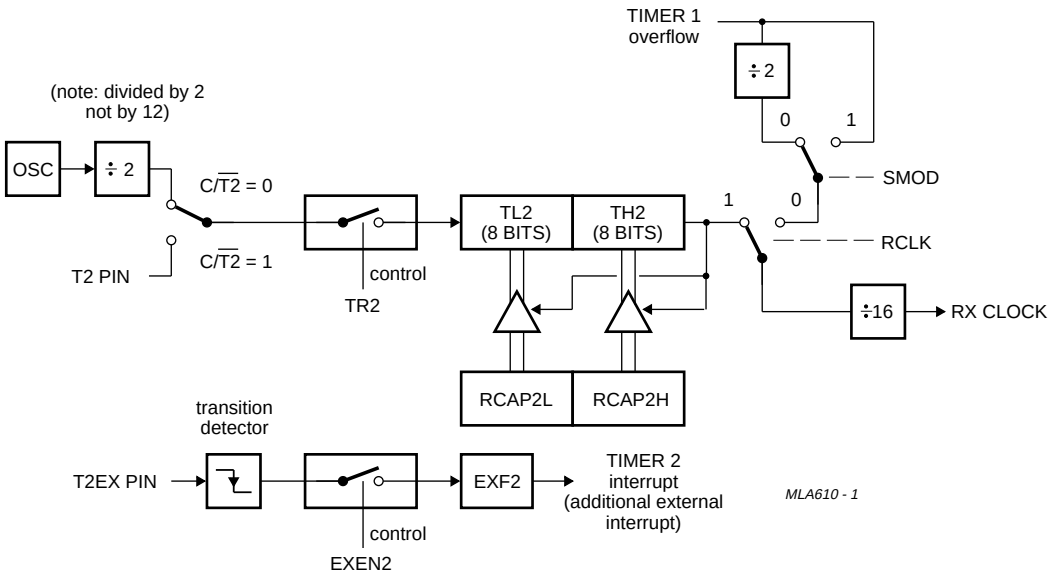

Fig.14 Timer 2 in Baud Rate Generator Mode.

6.11 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronously to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The interrupt system is shown in Fig.15. The P83CL781 acknowledges interrupt requests from fifteen sources as follows:

- INT0 to INT9
- Timer 0, Timer 1 and Timer 2
- I^2C-bus serial I/O
- UART.

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by its corresponding bit in the Interrupt Enable Registers (1EN0 and 1EN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled.

6.11.1 External interrupts INT2 to INT9

Port 1 lines serve an alternative purpose as eight additional interrupts INT2 to INT9. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. The external interrupt configuration is shown in Fig.15.

6.11.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. A low priority interrupt can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

Table 26 shows the interrupt vectors in order of priority. X0 having the highest priority; X9 the lowest. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 26 Interrupt vectors

SOURCE	SYMBOL	VECTOR
External 0	X0	0003H
I^2C-bus port	S1	002BH
External 5	X5	0053H
Timer 0	T0	000BH
Timer 2	T2	0033H
External 6	X6	005BH
External 1	X1	0013H
External 2	X2	003BH
External 7	X7	0063H
Timer 1	T1	001BH
External 3	X3	0043H
External 8	X8	006BH
UART	SO	0023H
External 4	X4	004BH
External 9	X9	0073H

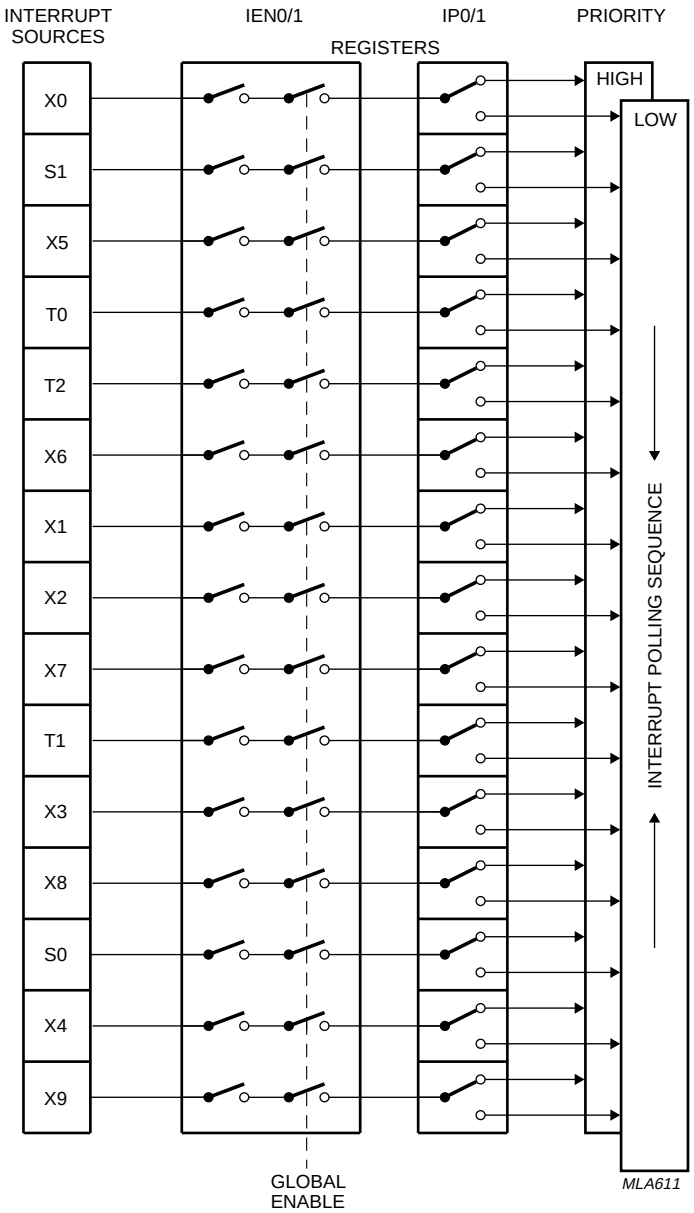

Fig.15 Interrupt system.

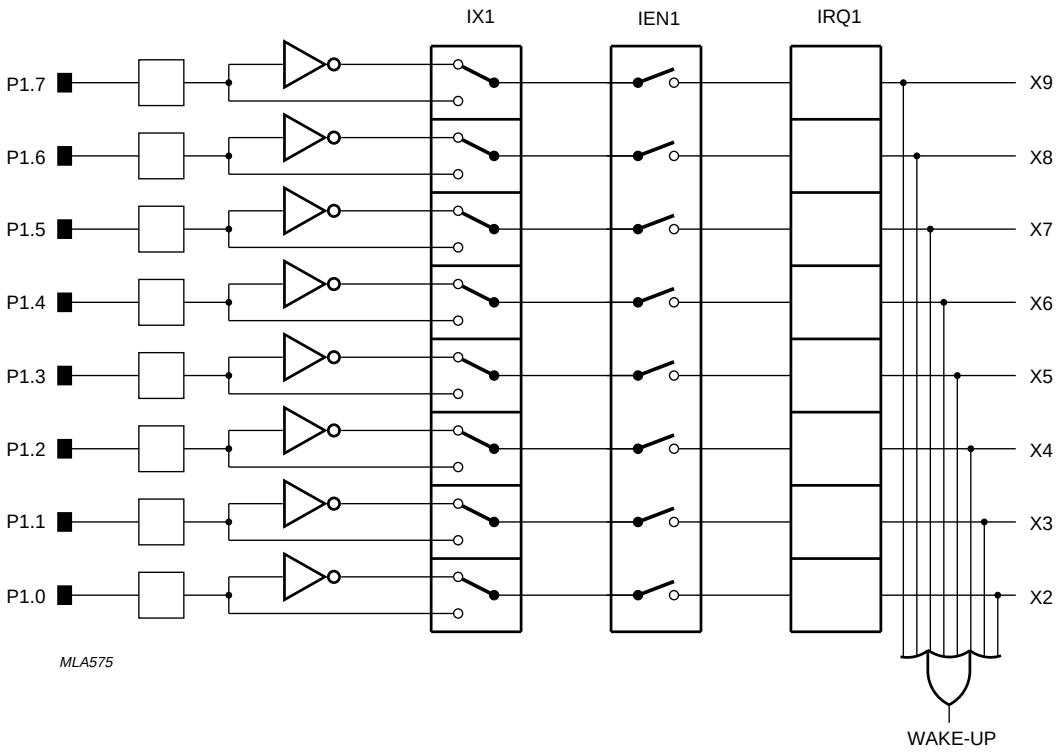

Fig.16 External interrupt configuration.

6.11.3 Interrupt Enable Register (IEN0)

Table 27 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0

Table 28 Description of IEN0 bits

BIT(1)	SYMBOL	FUNCTION
IEN0.7	EA	General enable/disable control. If EA = 0, no interrupt is enabled. If EA = 1, any individually enabled interrupt will be accepted.
IEN0.6	ET2	enable T2 interrupt
IEN0.5	ES1	enable I^2C-bus interrupt
IEN0.4	ES0	enable UART SIO interrupt
IEN0.3	ET1	enable Timer 1 interrupt (T1)
IEN0.2	EX1	enable external interrupt 1
IEN0.1	ET0	enable Timer 0 interrupt (T0)
IEN0.0	EX0	enable external interrupt 0

Note

1. Where: logic 0 = interrupt disabled; logic 1 = interrupt enabled.

6.11.4 Interrupt Enable Register (IEN1)

Table 29 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 30 Description of IEN1 bits

BIT(1)	SYMBOL	FUNCTION
IEN1.7	EX9	enable external interrupt 9
IEN1.6	EX8	enable external interrupt 8
IEN1.5	EX7	enable external interrupt 7
IEN1.4	EX6	enable external interrupt 6
IEN1.3	EX5	enable external interrupt 5
IEN1.2	EX4	enable external interrupt 4
IEN1.1	EX3	enable external interrupt 3
IEN1.0	EX2	enable external interrupt 2

Note

1. Where: logic 0 = interrupt disabled; logic 1 = interrupt enabled.

6.11.5 Interrupt Priority Register (IP0)

Table 31 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	PT2	PS1	PS0	PT1	PX1	PT0	PX0

Table 32 Description of IP0 bits

BIT(1)	SYMBOL	FUNCTION
IP0.7	–	Reserved
IP0.6	PT2	Timer 2 interrupt priority level
IP0.5	PS1	I^2C-bus interrupt priority level
IP0.4	PS0	UART SIO interrupt priority level
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

Note

1. Where: logic 0 = low priority; logic 1 = high priority.

6.11.6 Interrupt Priority Register (IP1)

Table 33 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 34 Description of IP1 bits

BIT(1)	SYMBOL	FUNCTION
IP1.7	PX9	external interrupt 9 priority level
IP1.6	PX8	external interrupt 8 priority level
IP1.5	PX7	external interrupt 7 priority level
IP1.4	PX6	external interrupt 6 priority level
IP1.3	PX5	external interrupt 5 priority level
IP1.2	PX4	external interrupt 4 priority level
IP1.1	PX3	external interrupt 3 priority level
IP1.0	PX2	external interrupt 2 priority level

Note

1. Where: logic 0 = low priority; logic 1 = high priority.

6.11.7 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 35 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 36 Description of IX1 bits

BIT	SYMBOL	FUNCTION
IX1.7	IL9	external interrupt 9 polarity level
IX1.6	IL8	external interrupt 8 polarity level
IX1.5	IL7	external interrupt 7 polarity level
IX1.4	IL6	external interrupt 6 polarity level
IX1.3	IL5	external interrupt 5 polarity level
IX1.2	IL4	external interrupt 4 polarity level
IX1.1	IL3	external interrupt 3 polarity level
IX1.0	IL2	external interrupt 2 polarity level

6.11.8 Interrupt Request Flag Register (IRQ1)

Table 37 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 38 Description of IRQ1 bits

BIT	SYMBOL	FUNCTION
IRQ1.7	IQ9	external interrupt 9 request flag
IRQ1.6	IQ8	external interrupt 8 request flag
IRQ1.5	IQ7	external interrupt 7 request flag
IRQ1.4	IQ6	external interrupt 6 request flag
IRQ1.3	IQ5	external interrupt 5 request flag
IRQ1.2	IQ4	external interrupt 4 request flag
IRQ1.1	IQ3	external interrupt 3 request flag
IRQ1.0	IQ2	external interrupt 2 request flag

6.11.9 RELATED REGISTERS

The following registers are used in conjunction with the interrupt system.

Table 39 Related registers

REGISTER	FUNCTION	SFR ADDRESS
IX1	Interrupt Polarity Register	E9H
IRQ1	Interrupt Request Flag Register	C0H
IEN0	Interrupt Enable Register	A8H
IEN1	Interrupt Enable Register (INT2 to INT9)	E8H
IP0	Interrupt Priority Register	B8H
IP1	Interrupt Priority Register (INT2 to INT9)	F8H

6.12 Oscillator circuitry

The on-chip oscillator circuitry of the P83CL781 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.17. For operation as a standard quartz oscillator, no external components are needed (except at 32 kHz). When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 40 and Fig.18).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator invertor is switched off to ensure no current will flow regardless of the voltage at XTAL1. To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.18f. There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 40 and shown in Fig.18. The required option should be stated when ordering.

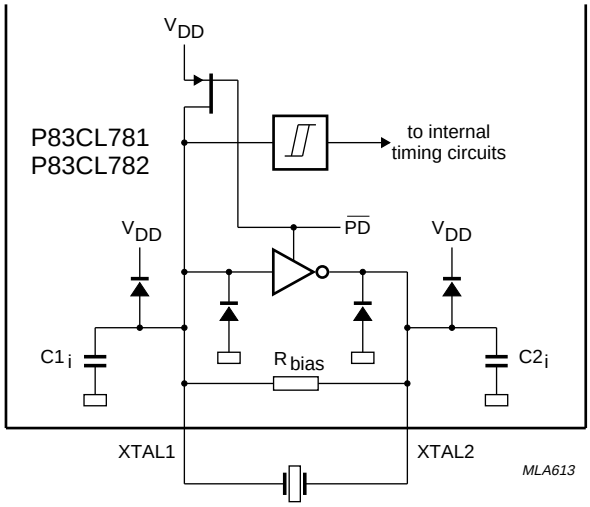

Fig.17 Oscillator.

Table 40 Oscillator options

OSCILLATOR	APPLICATION
Oscillator 1	For 32 kHz clock applications with external trimmer for frequency adjustment. A 4.7 MΩ bias resistor is needed for use in parallel with the crystal. See Fig.18c.
Oscillator 2	For low-power, low-frequency operations using LC components. See Fig.18e.
Oscillator 3	For medium frequency range applications.
Oscillator 4	For high frequency range applications.
RC	RC oscillator configuration. See Fig.18g.

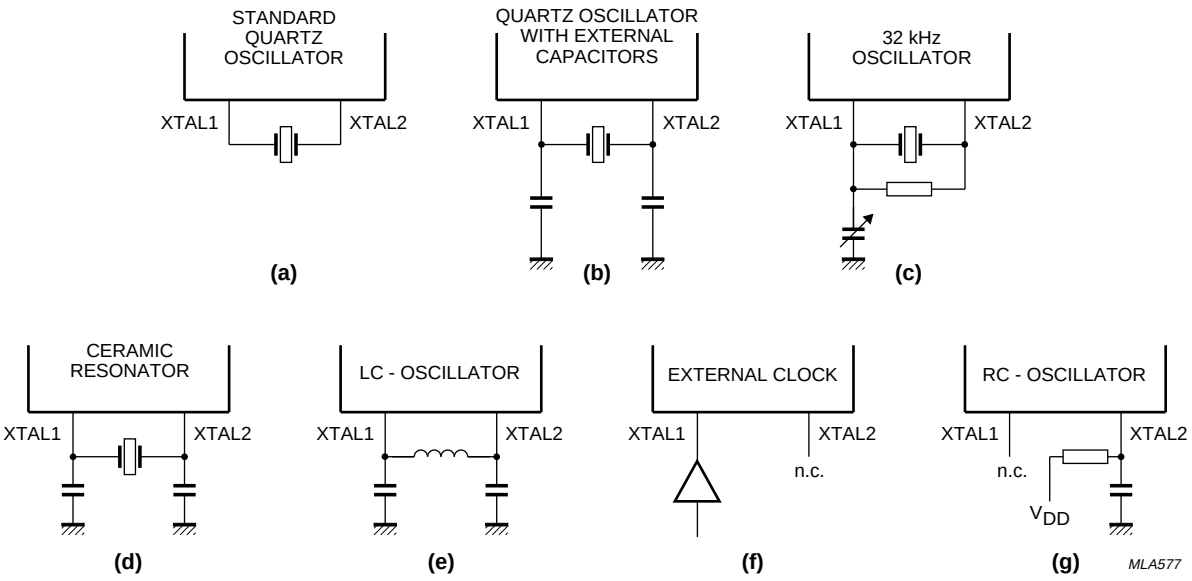

Fig.18 Alternative oscillator configurations.

6.12.1 OSCILLATOR TYPE SELECTION GUIDE

Table 41 Oscillator type selection guide

RESONATOR	FREQUENCY (MHz)	OPTION	C1 ext. (pF)		C2 ext. (pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Osc. 1	0	0	5	15	15 kΩ; note 1
	1.0	Osc. 2	0	30	0	30	600 Ω
	3.58	Osc. 2	0	15	0	15	100 Ω
	4.0	Osc. 2	0	20	0	20	75 Ω
	6.0	Osc. 3	0	10	0	10	60 Ω
	10.0	Osc. 4	0	15	0	15	60 Ω
	12.0	Osc. 4	0	10	0	10	40 Ω
	16.0	Osc. 4	0	15	0	15	20 Ω
PXE	0.455	Osc. 2	40	50	40	50	10 Ω
	1.0	Osc. 2	15	50	15	50	100 Ω
	3.58	Osc. 2	0	40	0	40	10 Ω
	4.0	Osc. 2	0	40	0	40	10 Ω
	6.0	Osc. 2	0	20	0	20	5 Ω
	10.0	Osc. 3	0	15	0	15	6 Ω
	12.0	Osc. 4	10	40	10	40	6 Ω
LC		Osc. 2	20	90	20	90	10 μH = 1 Ω; 100 μH = 5 Ω; 1 mH = 75 Ω

Note

1. 32 kHz quartz crystals with a series resistance higher than 15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5 V.

Table 42 Oscillator equivalent circuit parameters (see note 1)

SYMBOL	PARAMETER	OPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_m	transconductance	Osc. 1	T_{amb} = +25 °C; V_{DD} = 4.5 V	–	15	–	µS
g_{m1}		Osc. 2		200	600	1000	µS
g_{m2}		Osc. 3		400	1500	4000	µS
g_{m3}		Osc. 4		1000	4000	10000	µS
$C1_i$	input capacitance	Osc. 1		–	3.0	–	pF
$C1_{i1}$		Osc. 2		–	8.0	–	pF
$C1_{i2}$		Osc. 3		–	8.0	–	pF
$C1_{i3}$		Osc. 4		–	8.0	–	pF
$C2_i$	output capacitance	Osc. 1		–	23	–	pF
$C2_{i1}$		Osc. 2		–	8.0	–	pF
$C2_{i2}$		Osc. 3		–	8.0	–	pF
$C2_{i3}$		Osc. 4		–	8.0	–	pF
R2	output resistance	Osc. 1		–	3800	–	kΩ
$R2_1$		Osc. 2		–	65	–	kΩ
$R2_2$		Osc. 3		–	18	–	kΩ
$R2_3$		Osc. 4		–	5.0	–	kΩ

Note

1. The equivalent circuit data of the internal oscillator compares with that of matched crystals.

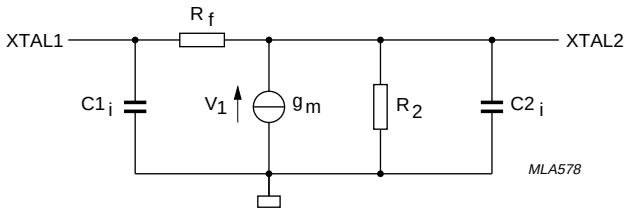

Fig.19 Equivalent circuit diagram.

6.12.2 RC OSCILLATOR

The externally adjustable RC oscillator has a frequency range from 100 to 500 kHz.

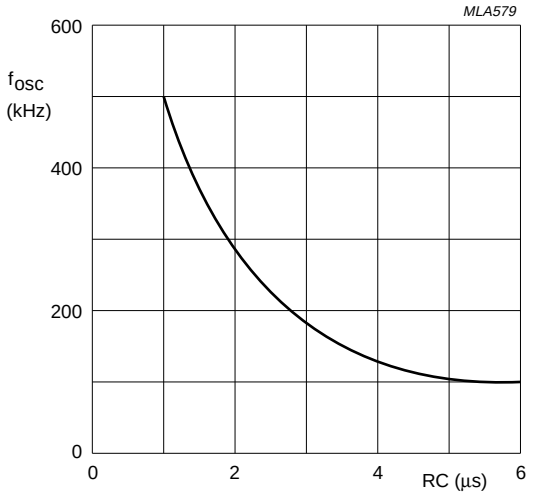

Fig.20 Oscillator frequency as a function of RC.

6.13 Reset

To initialize the P83CL781 a reset is performed by either of two methods:

- Applying an external signal to the RST pin
- Via Power-on reset circuitry.

The reset state of the port pins is mask-programmable and can be defined by the user. The standard reset value for Ports 0 to 3 is FFH. A reset leaves the internal registers as shown in Table 43.

6.13.1 EXTERNAL RESET USING THE RST PIN

The reset input for the P83CL781 is RST; pin 15. A Schmitt-trigger is used at the input for noise rejection. The output of the Schmitt-trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. Port pins adopt their reset state immediately after the RST goes HIGH. During reset, ALE and $\overline{PSEN}$ are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated until RST goes LOW. The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

6.13.2 POWER-ON RESET

The device contains on-chip circuitry which switches the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V; if the mask option ‘ON’ has been chosen. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation. See Fig.23.

The on-chip Power-on reset circuitry can also be switched off via the mask option ‘OFF’. This option reduces the Power-down current to typically 800 nA and can be chosen if external reset circuitry is used.

An automatic reset can be obtained by connecting the RST pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt-trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The Power-on reset circuitry is shown in Fig.22.

Table 43 State of internal registers after a reset

REGISTER	CONTENTS(1)
ACC	0000 0000
B	0000 0000
DPL	0000 0000
DPH	0000 0000
IEN0	0000 0000
IEN1	0000 0000
IP0	XX00 0000
IP1	0000 0000
IX1	0000 0000
IRQ1	0000 0000
PCH	0000 0000
PCL	0000 0000
PCON	0XX0 0000
P0 to P3	1111 1111
S0BUF	XXXX XXXX
S0CON	0000 0000
S1ADR	0000 0000
S1CON	0000 0000
S1DAT	0000 0000
S1STA	1111 1000
SP	0000 0111
TCON	0000 0000
T2CON	0000 0000
T3	0000 0000
TH0, TH1, TH2	0000 0000
TL0, TL1, TL2	0000 0000
TMOD	0000 0000
PSW	0000 0000
RCAP2L	0000 0000
RCAP2H	0000 0000

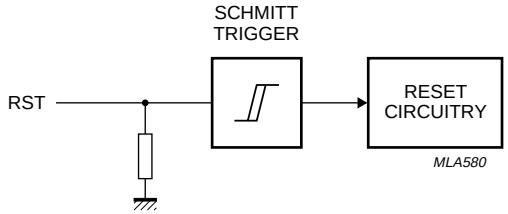

Fig.21 Reset configuration.

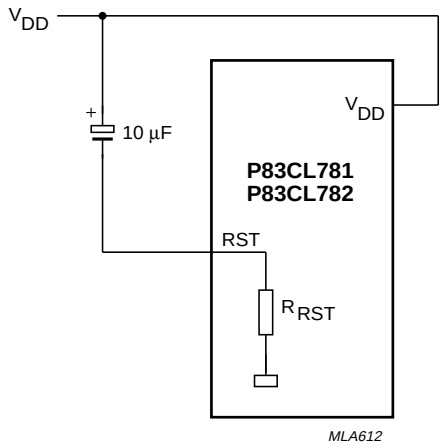

Fig.22 Power-on reset circuitry.

Note

1. Where: X = undefined state.

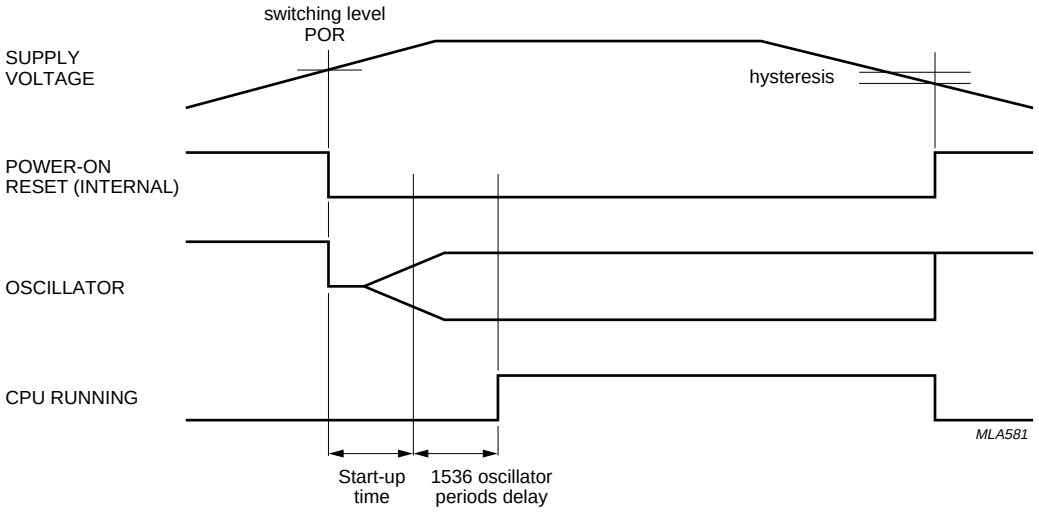

Fig.23 Power-on reset switching level.

7 INSTRUCTION SET

The P83CL781 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

Table 44 Instruction Set

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct**	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct byte	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@RI,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	3	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order nibble indirect RAM with A	1	1	D6, D7

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	•1 addr
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	♦1 addr
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Table 45 Notation for data addressing modes

SYMBOL	DESCRIPTION
Rr	Working registers R0 to R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbyte program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbyte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.

Table 46 Hexadecimal opcode cross-reference

SYMBOL	DESCRIPTION
*	8, 9, A, B, C, D, E, F.
•	11, 31, 51, 71, 91, B1, D1, F1.
♦	01, 21, 41, 61, 81, A1, C1, E1.

7.1 Instruction Map

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr 11	LJMP addr 16	RR A	INC A	INC dir	INC @ Ri		INC Rr							
							0	1	0	1	2	3	4	5	6	7
1	JBC bit, rel	ACALL addr 11	LCALL addr 16	RRC A	DEC A	DEC dir	DEC @ Ri		DEC Rr							
							0	1	0	1	2	3	4	5	6	7
2	JB bit, rel	AJMP addr 11	RET	RL A	ADD A, # data	ADD A, dir	ADD A, @ Ri		ADD A, Rr							
							0	1	0	1	2	3	4	5	6	7
3	JNB bit, rel	ACALL addr 11	RETI	RLC A	ADDC A, # data	ADDC A, dir	ADDC A, @ Ri		ADDC A, Rr							
							0	1	0	1	2	3	4	5	6	7
4	JC rel	AJMP addr 11	ORL dir, A	ORL dir, # data	ORL A, # data	ORL A, dir	ORL A, @ Ri		ORL A, Rr							
							0	1	0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr 11	ANL dir, A	ANL dir, # data	ANL A, # data	ANL A, dir	ANL A, @ Ri		ANL A, Rr							
							0	1	0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr 11	XRL dir, A	XRL dir, # data	XRL A, # data	XRL A, dir	XRL A, @ Ri		XRL A, Rr							
							0	1	0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr 11	ORL C, bit	JMP @ A+DPTR	MOV A, # data	MOV dir, # data	MOV @ Ri, # data		MOV Rr, # data							
							0	1	0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr 11	ANL C, bit	MOVC A, @ A+PC	DIV AB	MOV dir, dir	MOV dir, @ Ri		MOV dir, Rr							
							0	1	0	1	2	3	4	5	6	7
9	MOV DPTR, # data 16	ACALL addr 11	MOV bit, C	MOVC A, @ A+DPTR	SUBB A, # data	SUBB A, dir	SUBB A, @ Ri		SUBB A, Rr							
							0	1	0	1	2	3	4	5	6	7
A	ORL C, / bit	AJMP addr 11	MOV bit, C	INC DPTR	MUL AB		MOV @ Ri, dir		MOV Rr, dir							
							0	1	0	1	2	3	4	5	6	7
B	ANL C, / bit	ACALL addr 11	CPL bit	CPL C	CJNE A, # data, rel	CJNE A, dir, rel	CJNE @ Ri, # data, rel		CJNE Rr, # data, rel							
							0	1	0	1	2	3	4	5	6	7
C	PUSH dir	AJMP addr 11	CLR bit	CLR C	SWAP A	XCH A, dir	XCH A, @ Ri		XCH A, Rr							
							0	1	0	1	2	3	4	5	6	7
D	POP dir	ACALL addr 11	SETB bit	SETB C	DA A	DJNZ dir, rel	XCHD A, @ Ri		DJNZ Rr, rel							
							0	1	0	1	2	3	4	5	6	7
E	MOVX A, @ DPTR	AJMP addr 11	MOVX A, @ Ri		CLR A	MOV A, dir *	MOV A, @ Ri		MOV A, Rr							
			0	1			0	1	0	1	2	3	4	5	6	7
F	MOVX @ DPTR, A	ACALL addr 11	MOVX @ Ri, A		CPL A	MOV dir, A	MOV @ Ri, A		MOV Rr, A							
			0	1			0	1	0	1	2	3	4	5	6	7

MLA632 - 1

* MOV A, ACC is not a valid instruction.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
I_I	DC current on any input	–	+5.0	mA
I_O	DC current on any output	–	–5.0	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature - P83CL781	–40	+85	°C
	operating ambient temperature - P83CL782	–25	+55	°C
T_j	operating junction temperature	–	+125	°C

9 DC CHARACTERISTICS

The DC characteristics apply to both the P83CL781 and the P83CL782 unless otherwise stated. V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C for the P83CL781 and –25 to +55 °C for the P83CL782; all voltages with respect to V_{SS} unless otherwise specified. See notes 1, 2 and 3.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.8	–	6.0	V
V_{DD}	RAM retention voltage in Power-down mode		1.0	–	6.0	V
I_{DD}	supply current operating; P83CL781	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 4	–	17	25	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 4	–	2.4	5	mA
I_{DD}	supply current operating; P83CL782	V_{DD} = 3.1 V; f_{CLK} = 12 MHz; note 4	–	8.4	12	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 4	–	2.4	5	µA
$I_{IDD(ID)}$	supply current Idle mode; P83CL781	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 5	–	5.1	12	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 5	–	0.75	3	mA
$I_{IDD(ID)}$	supply current Idle mode; P83CL782	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 5	–	2.7	5	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 5	–	0.75	3	mA
$I_{IDD(PD)}$	supply current Power-down mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 6	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL}	LOW level input voltage	note 7	V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 7	$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	LOW level input current	V_{DD} = 5 V; V_{IN} = 0.4 V; note 7	–	–	–100	µA
		V_{DD} = 2.5 V; V_{IN} = 0.4 V; note 7	–	–	–50	µA
$I_{IL(T)}$	LOW level input current (HIGH-to-LOW transition)	V_{DD} = 5 V; V_{IN} = $0.5V_{DD}$; note 7	–	–	–1.0	mA
		V_{DD} = 2.5 V; V_{IN} = $0.5V_{DD}$; note 7	–	–	–500	µA
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$; note 7	–	–	±10	µA
Outputs						
I_{OL}	LOW level output current; except SDA and SCL	V_{DD} = 5 V; V_{OL} = 0.4 V	1.6	–	–	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	0.7	–	–	mA
I_{OL1}	LOW level output current; SDA and SCL	V_{DD} = 5 V; V_{OL} = 0.4 V	3.0	–	–	mA
I_{OH}	HIGH level output current (push-pull options only)	V_{DD} = 5 V; $V_{OH} = V_{DD} - 0.4$ V	–1.6	–	–	mA
		V_{DD} = 2.5 V; $V_{OH} = V_{DD} - 0.4$ V	–0.7	–	–	mA
R_{RST}	RST pull-down resistor		10	–	200	kΩ

Notes

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3 pins when these make a HIGH-to-LOW transition during bus operations. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the most adverse conditions (capacitive loading >100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such events it may be required to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.
2. Capacitive loading on Ports 0 and 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9% of V_{DD} specification when the address bits are stabilizing.
3. Circuits with Power-on reset option ‘OFF’ are tested at V_{DDmin} = 1.8 V; with the ‘ON’ option (typically 1.3 V) they are tested at V_{DDmin} = 2.3 V.
4. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ =10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}.
5. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}.
6. The Power-down current is measured with all output pins disconnected; XTAL1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
7. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.

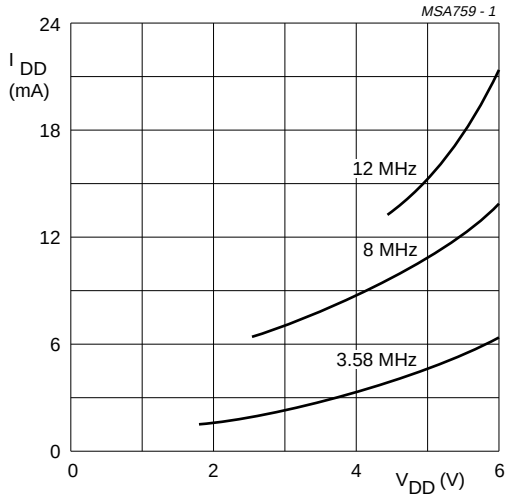

Fig.24 P83CL781: typical operating current as a function of frequency and V_{DD}, T_{amb} = 25 °C, oscillator option Osc.3.

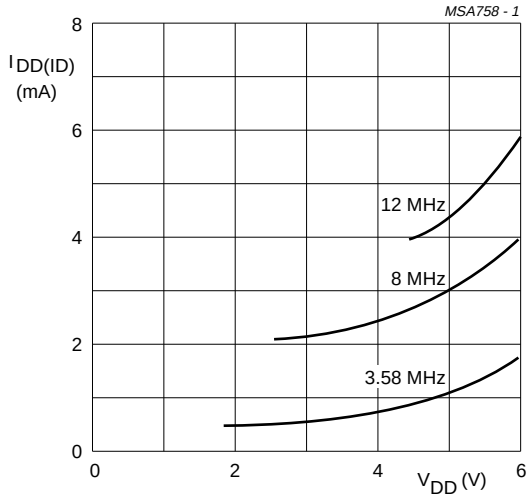

Fig.25 P83CL781: typical Idle current as a function of frequency and V_{DD}, T_{amb} = 25 °C, oscillator option Osc.3.

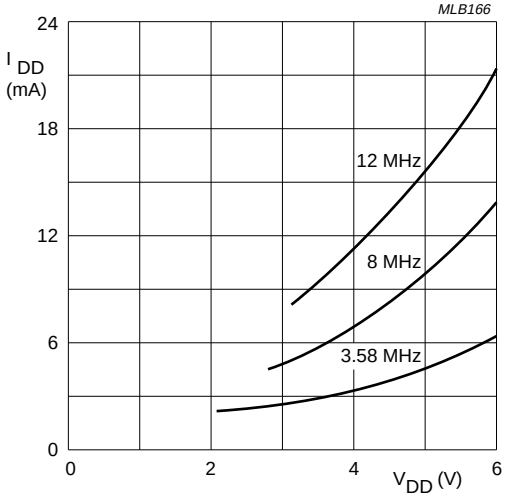

Fig.26 P83CL782: typical operating current as a function of frequency and V_{DD}, T_{amb} = 25 °C, oscillator option Osc.3.

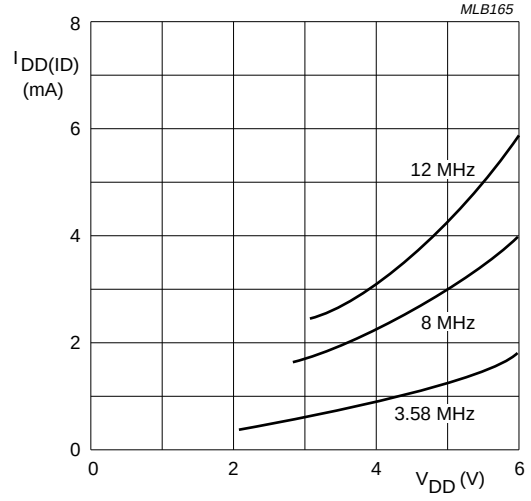

Fig.27 P83CL782: typical Idle current as a function of frequency and V_{DD}, T_{amb} = 25 °C, oscillator option Osc.3.

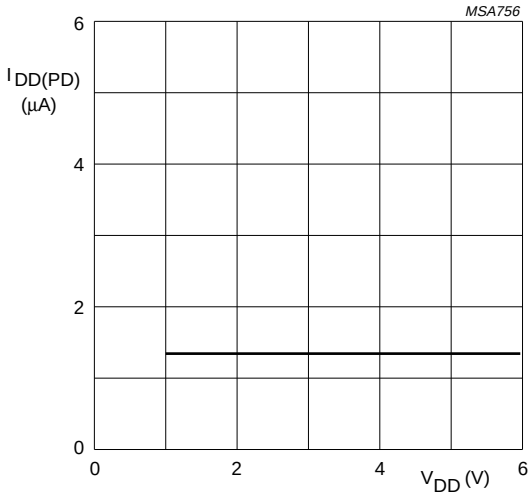

Fig.28 Typical Power-down current as a function of V_{DD}, T_{amb} = 25 °C.

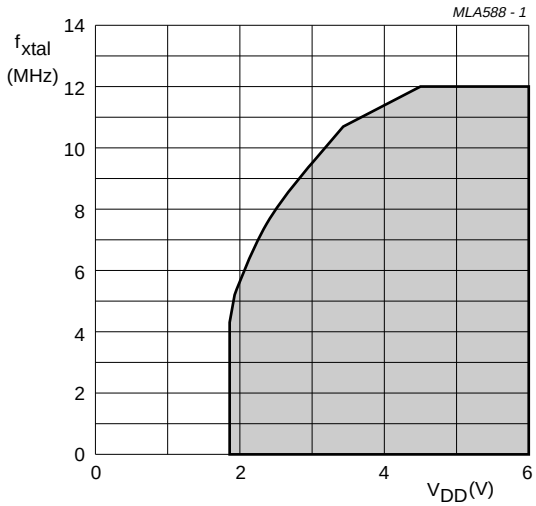

Fig.29 Frequency operating range - P83CL781.

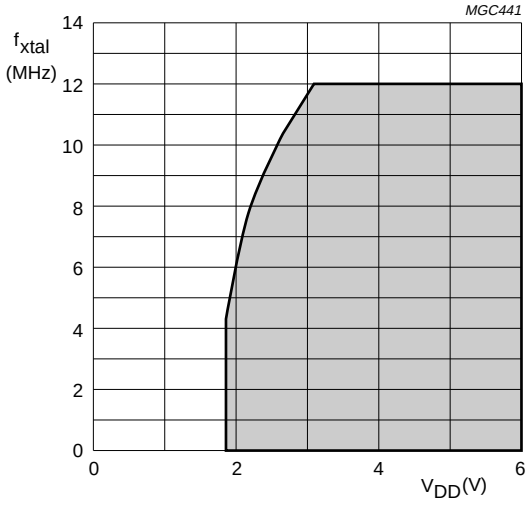

Fig.30 Frequency operating range - P83CL782.

10 AC CHARACTERISTICS

The following AC characteristics apply to both the P83CL781 and P83CL782 unless otherwise stated.

10.1 Program memory

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C for the P83CL781 and –25 to +55 °C for the P83CL782; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless specified. See Fig.31.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{LL}	ALE pulse duration	127	–	$2t_{CK}$ – 40	–	ns
t_{AL}	Address set-up time to ALE	43	–	t_{CK} – 40	–	ns
t_{LA}	Address hold time after ALE	48	–	t_{CK} – 35	–	ns
t_{LIV}	Time from ALE to valid instruction input	–	233	–	$4t_{CK}$ – 100	ns
t_{LC}	Time from ALE to control pulse $\overline{PSEN}$	58	–	t_{CK} – 25	–	ns
t_{CC}	Control pulse duration $\overline{PSEN}$	215	–	$3t_{CK}$ – 35	–	ns
t_{CIV}	Time from $\overline{PSEN}$ to valid instruction input	–	125	–	$3t_{CK}$ – 125	ns
t_{CI}	Input instruction hold time after $\overline{PSEN}$	0	–	0	–	ns
t_{CIF}	Input instruction float delay after $\overline{PSEN}$	–	63	–	t_{CK} – 20	ns
t_{AC}	Address valid after $\overline{PSEN}$	75	–	t_{CK} – 8	–	ns
t_{AIV}	Address to valid instruction input	–	302	–	$5t_{CK}$ – 115	ns
t_{AFC}	Address float delay after $\overline{PSEN}$	12	–	0	–	ns

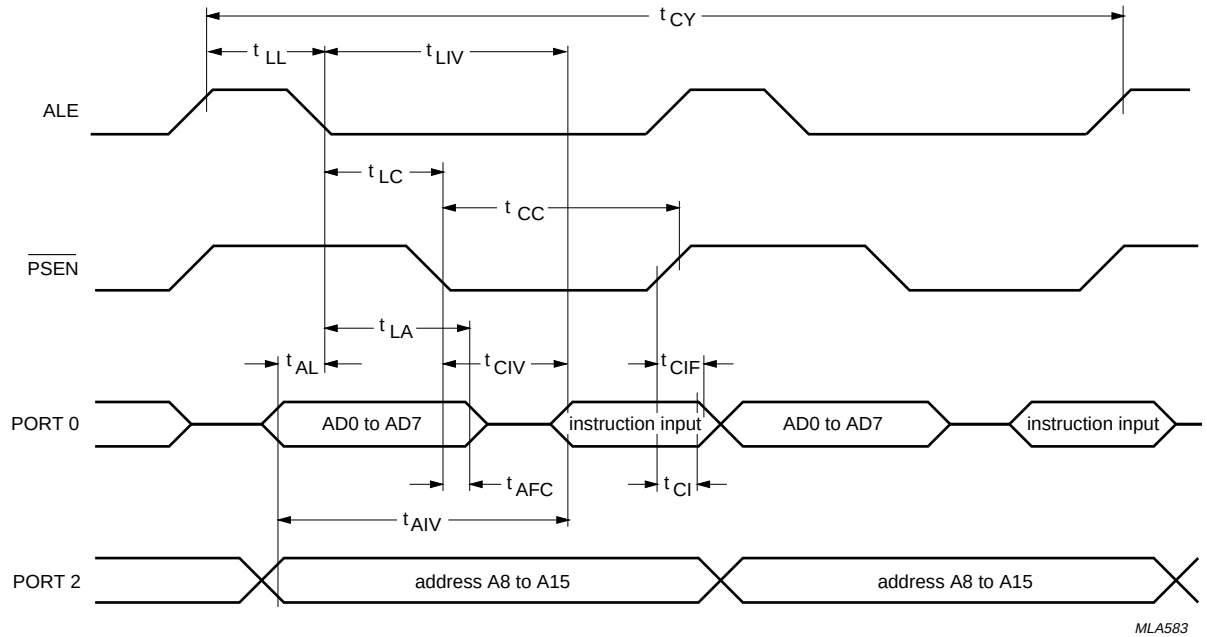

Fig.31 Read from program memory.

10.2 External data memory

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C for P83CL781 and −25 to +55 °C for the P83CL782; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 40 pF for all other outputs unless specified. See note 1 and Figs 32 and 33.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RR}	RD pulse duration	400	–	$6t_{CK}$ – 100	–	ns
t_{WW}	WR pulse duration	400	–	$6t_{CK}$ – 100	–	ns
t_{LA}	Address hold time after ALE	48	–	t_{CK} – 35	–	ns
t_{RD}	RD to valid data input	–	150	–	$5t_{CK}$ – 165	ns
t_{DFR}	Data float delay after $\overline{RD}$	–	97	–	$2t_{CK}$ – 70	ns
t_{LD}	Time from ALE to valid data input	–	517	–	$8t_{CK}$ – 150	ns
t_{AD}	Address to valid data input	–	585	–	$9t_{CK}$ – 165	ns
t_{LW}	Time from ALE to $\overline{RD}$ or $\overline{WR}$	200	300	$3t_{CK}$ – 50	$3t_{CK}$ + 50	ns
t_{AW}	Time from address to $\overline{RD}$ or $\overline{WR}$	203	–	4	–	ns
t_{WHLH}	Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	43	123	t_{CK} – 40	t_{CK} + 40	ns
t_{DWX}	Data valid to $\overline{WR}$ transition	23	–	t_{CK} – 60	–	ns
t_{DW}	Data set-up time before $\overline{WR}$	433	–	$7t_{CK}$ – 150	–	ns
t_{WD}	Data hold time after $\overline{WR}$	33	–	t_{CK} – 50	–	ns
t_{AFR}	Address float delay after $\overline{RD}$	–	12	–	12	ns

Note

1. Interfacing the P83CL781 or the P83CL782 to devices with float times up to 75 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

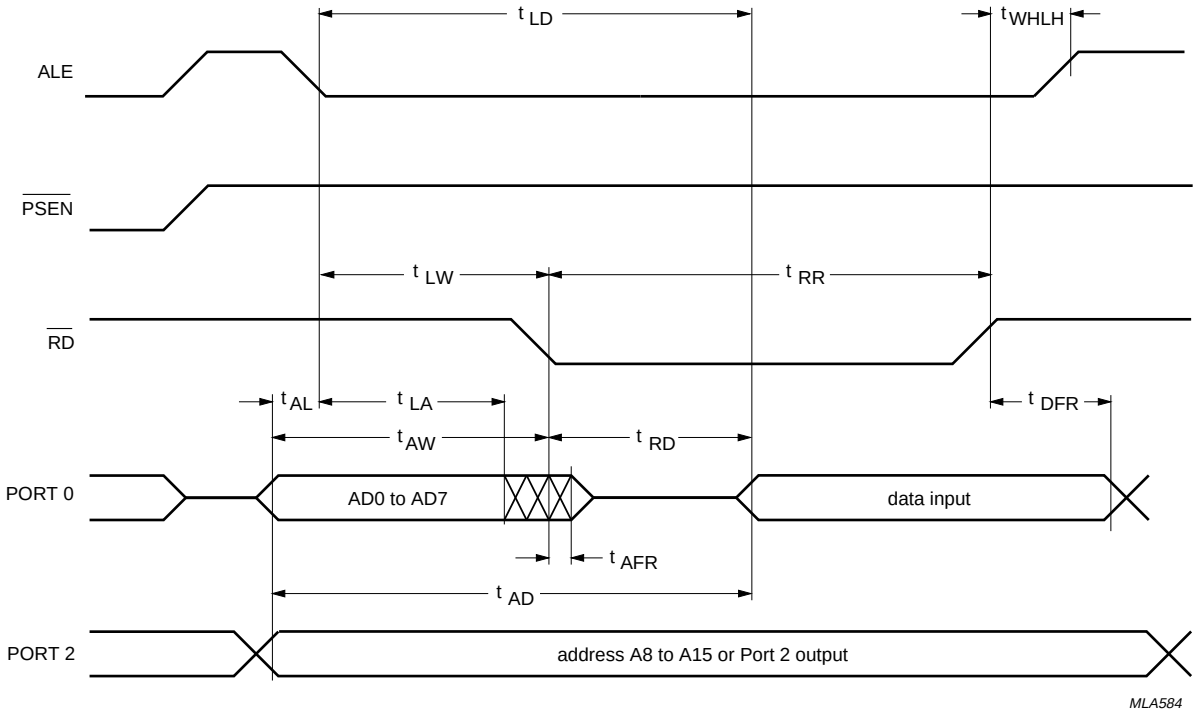

Fig.32 Read from data memory.

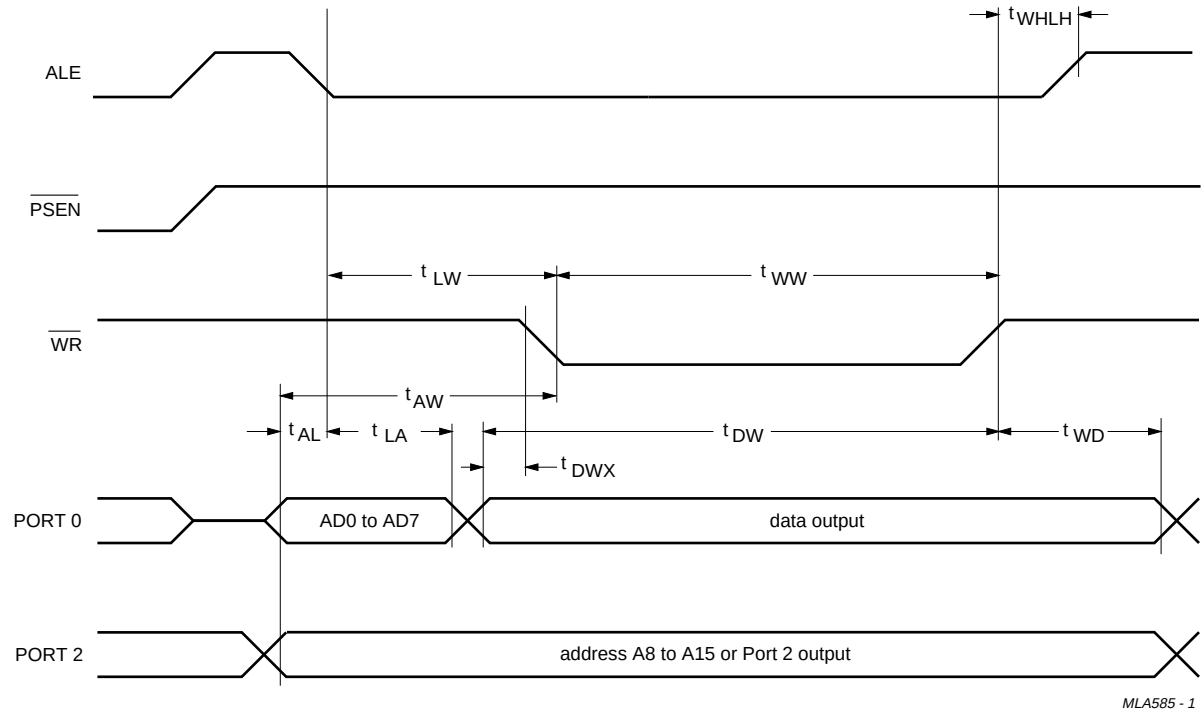

Fig.33 Write to data memory.

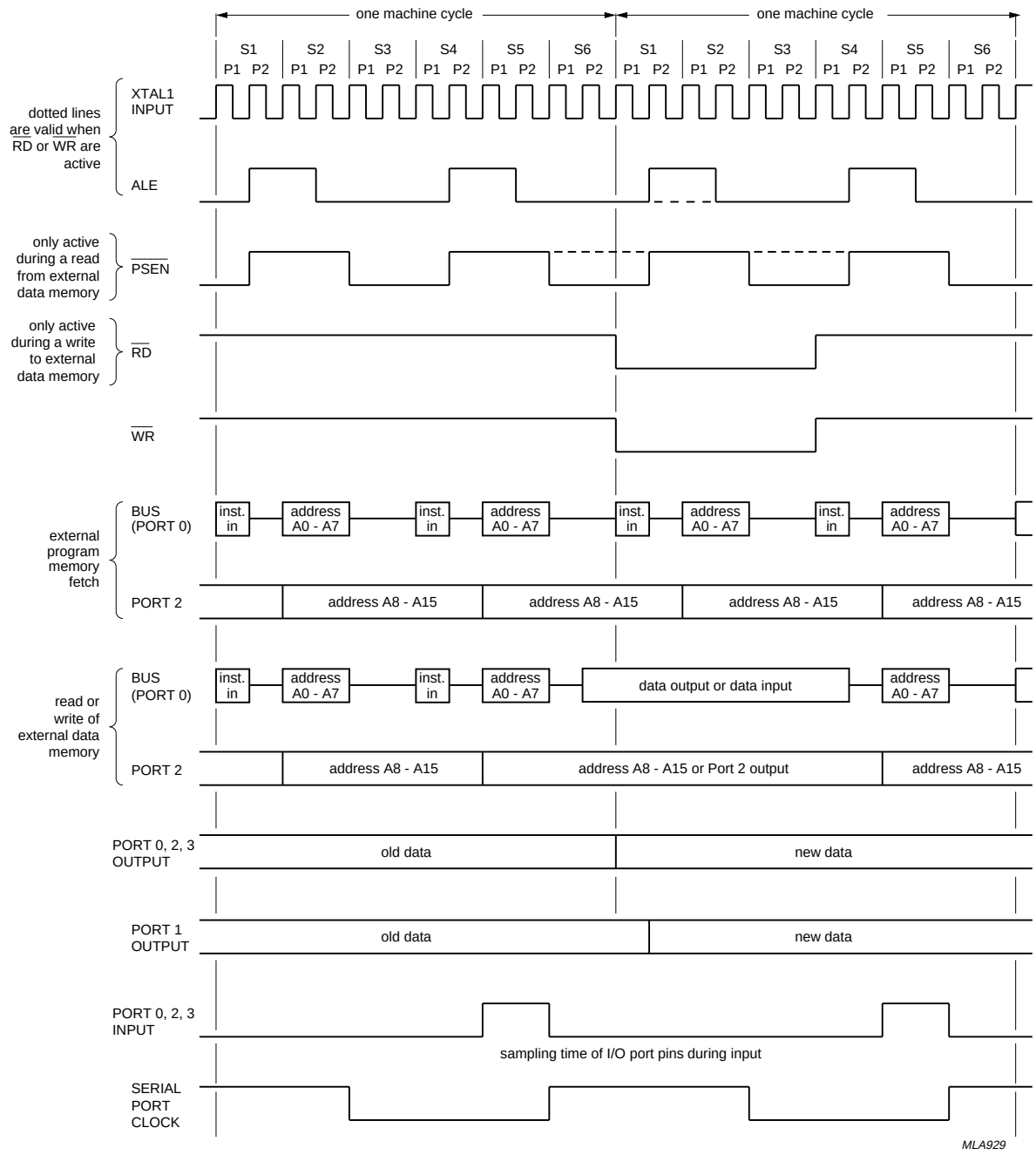

Fig.34 Instruction cycle timing.

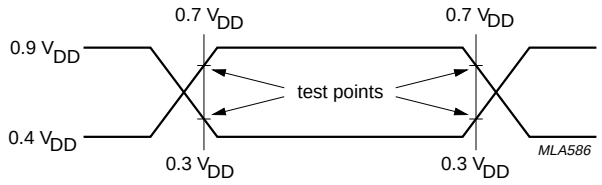

Fig.35 AC testing input waveform.

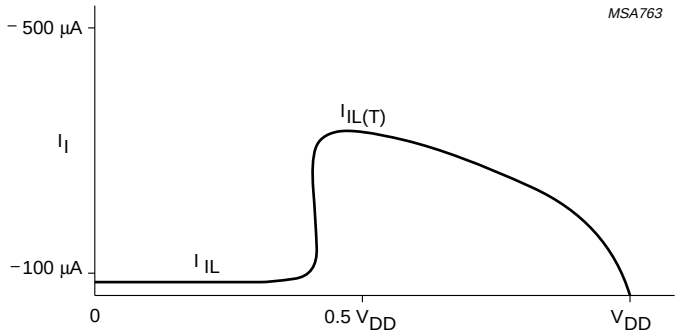

Fig.36 Input current.