DECT burst mode controller PCD5042

1 FEATURES

- On-chip pre-programmed Communication Controller with embedded firmware for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and control of the device's other functional units.
- Fixed Part (FP) modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control (by P00 packets)
- On-chip comparator for receive data slicer function (only available in the LQFP80 package)
- Switches up to12 active speech channels from speech interface to 1152 kbits/s. radio interface, and vice versa
- Dual channel speech/data capability
- RSSI measurement, with on-chip 6-bits peak/hold detector
- Local call switching for up to 6 internal calls on RF side/local call switching on speech side.
- Quality control report
- Digital Phase Locked Loop (DPLL)
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1 kbyte extended RAM memory
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Watchdog with two programmable time-outs
- Low power consumption in standby mode
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

2 GENERAL DESCRIPTION

The PCD5042 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and MAC Layer time-critical functions, for use in DECT base station products which comply with the following standards:

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3 : Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9).

The PCD5042 has interfaces to:

- Up to 4 ADPCM CODECs in a simple base station (with up to 4 analogue lines) without glue logic
- n x 64 kbits/s highway, where n = 1 to 32, for systems requiring more than 4 connections to the network
- A radio transceiver; the interface is fully decoded, and includes power-down signals
- An external microcontroller.

The PCD5042 is designed to be connected to an ADPCM CODEC (Philips' PCD5032, for example) and an 80C51-type microcontroller. Other microcontrollers (e.g. 68000) and CODECs can also be supported.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5042H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2
PCD5042HZ	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 BLOCK DIAGRAM

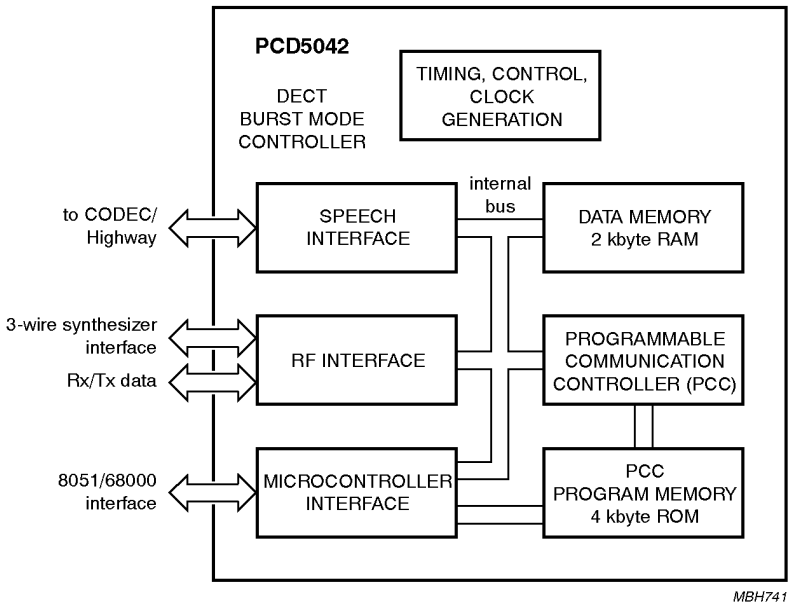

Fig.1 Block diagram.

5 PINNING (see Figs 2 and 3)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
AD0 to AD7	1 to 8	80, 1, and 3 to 7	I/O	address/Data bus
ALE	9	9	I	address latch enable
$\overline{CS}$	10	11	I	chip select (active LOW)
A8 to A10	13 to 11	14 to 12	I	address bus
V_{DD1}	14	15	P	positive supply 1
PROC_CLK	15	16	O	microcontroller clock; programmable from $f_{CLK}/64$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS1}	16	17	P	negative supply 1
XTAL1	17	20	I	crystal oscillator input
XTAL2	18	21	O	crystal oscillator output
V_{SS2}	19	22	P	negative supply
RESET_OUT	20	23	O	watchdog timer output; intended to reset the external microcontroller when expired
$\overline{RD}$	21	24	I	read (active LOW)
$\overline{WR}$	22	25	I	write (active LOW)
$\overline{RDY}$	23	26	O	ready signal (active LOW), to initiate wait states in the microcontroller (open drain)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{INT}$	24	27	O	interrupt (active LOW)
CLK100	25	29	O	100 Hz frame timer
V_{SS3}	26	31	P	negative supply 3
DO	27	32	O	3-state data output on the speech interface
FS3	–	33	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS1	28	34	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS4	–	35	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS2	29	36	O	8 kHz framing signal to ADPCM CODEC 2 in the base station mode
DI	30	37	I	data input on the speech interface
DCK	31	38	O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
CLK3	32	39	O	3.456 MHz clock (nominal value, used to adjust system timing)
ANT_SW	33	40	O	selects one of two antennas
$\overline{T\_ENABLE}$	34	41	O	Transmitter Enable (active LOW)
T_POWER_RMP	35	43	O	Transmitter Power Ramp control
RMT_STAT	36	44	I	serial 8-bit data can be read in for each slot; REMote radio
SYNTH_LOCK	37	45	I	lock indication from synthesizer
V_{SS4}	38	46	P	negative supply 4
REF_CLK	39	47	O	reference frequency for the synthesizer, i.e. the crystal oscillator clock f_{CLK}
V_{DD2}	40	48	P	positive supply 2
S_ENABLE	41	49	O	synthesizer enable
S_CLK	42	51	O	clock signal, to be used with S_DATA
S_DATA	43	52	O	serial data to the synthesizer
S_POWER_DWN	44	53	O	synthesizer power-down control
VCO_BND_SW	45	54	O	VCO bandswitch control signal
1200 HZ	46	55	O	control signal for dual synthesizer schemes
T_DATA	47	56	O	serial output data to transmitter
SET_OFF_IN	48	57	I	switches off the crystal oscillator, and prevents all RF signals from becoming active
TEST1	49	58	I	selects various test modes.; normal operation set to 0
RSSI_AN	50	60	I	analog signal (for basic DECT systems), peak signal strength measured after a lowpass filter
TEST2	51	–	I	selects various test modes; normal operation set to 0
TEST3	52	61	I	selects various test modes; normal operation set to 0
				e data

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{\text{R\_ENABLE}}$	54	64	O	receiver enable (active LOW)
R_POWER_DWN	55	65	O	receiver power-down
$\overline{\text{COMP\_NE}}$	–	66	I	digital input comparator not_enable (active LOW)
SLICE_CTR	56	67	O	slice time constant control
COMP_OUT	–	68	O	digital comparator output
V_{DD3}	57	69	P	positive supply 3
V_{SS5}	58	70	P	negative supply 5
COMP_INM	–	71	I	analog comparator input negative
V_{REF}	59	72	I	reference input for the A/D converter
COMP_INP	–	73	I	analog input positive
$V_{DD(RAM)}$	60	74	P	power supply for data RAM
SYNCPORT	61	76	I/O	in the base station the signal is the SYNCPORT
RESET	62	77	I	BMC master reset signal
MEM_SEL	63	78	I	selects PCC program memory at microcontroller interface
EN_WATCHDOG	64	79	I	enable watchdog input; when HIGH, the watchdog timer of the BMC is enabled

Notes

1. Un-referenced pins for the LQFP80 package are not connected. FS3, FS4 and the comparator signals are only available in the LQFP80 package.
2. **All** signals which are input or I/O, and which can be floating, need to be pulled up to V_{DD} or down to V_{SS} in order to protect the device against cross-currents. Exceptions are VREF and RSSI_AN, which do not have to be protected.

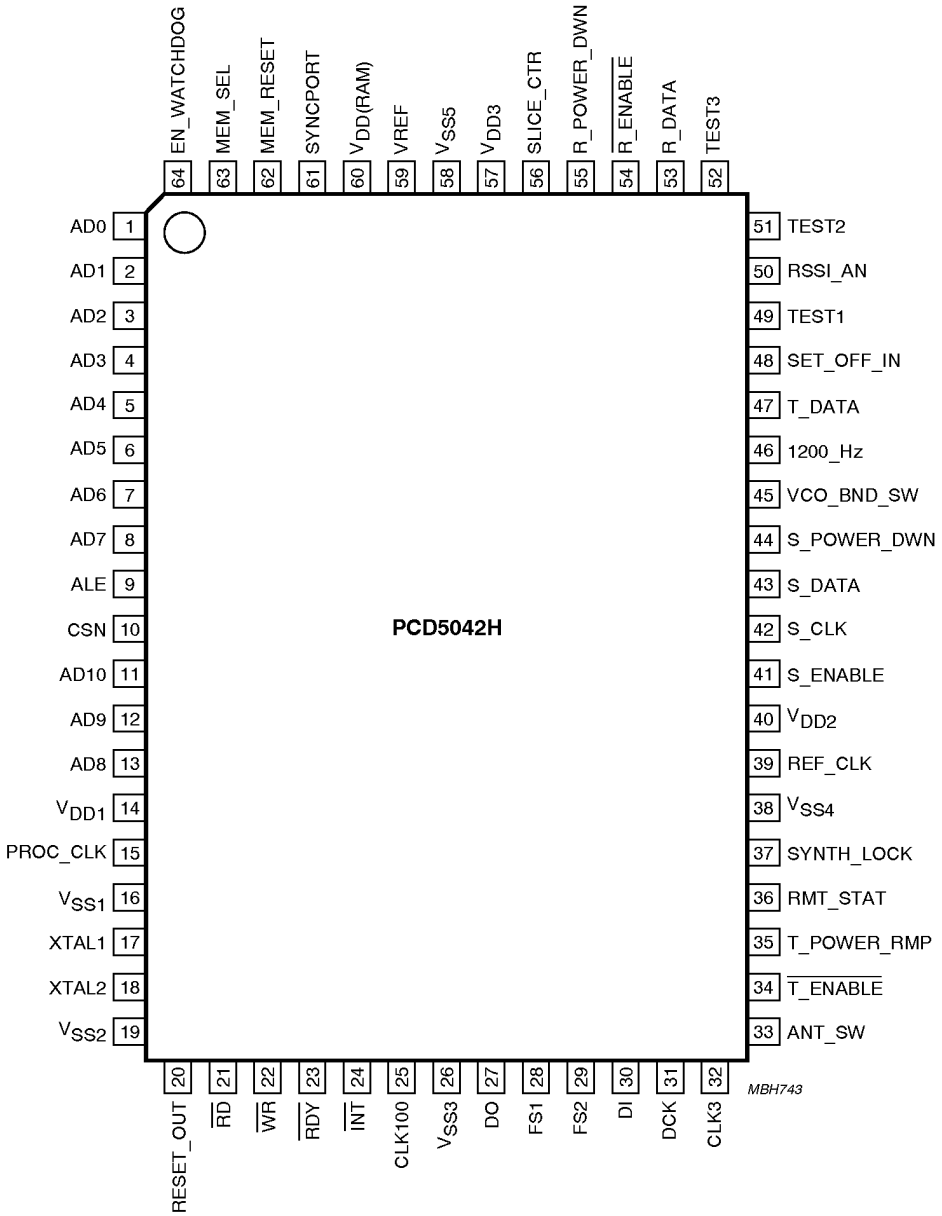

Fig.2 Pin configuration, PCD5042H (QFP64 package).

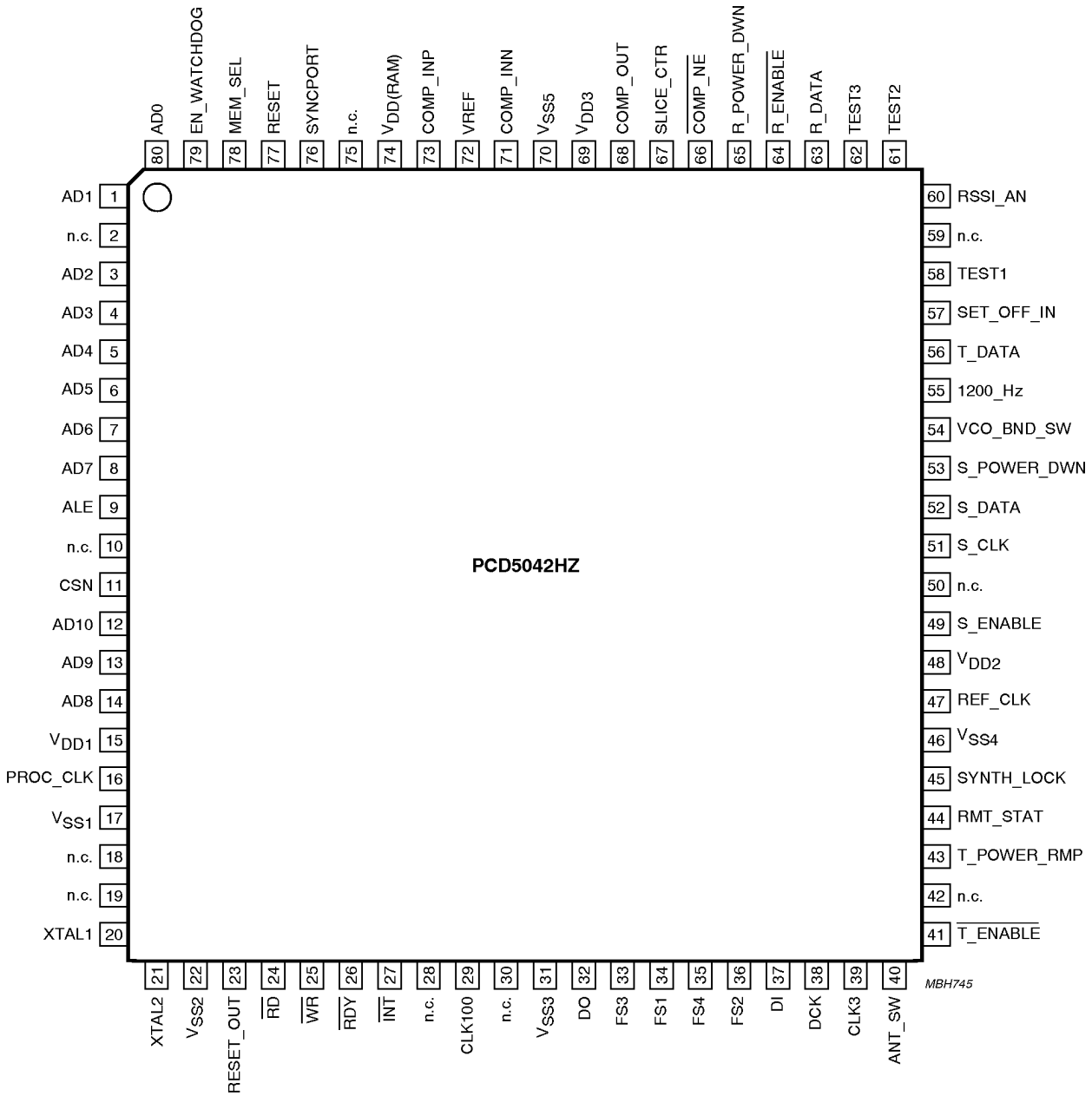

Fig.3 Pin configuration, PCD5042HZ (LQFP80 package).

6 FUNCTIONAL DESCRIPTION (see Fig.1)

The PCD5042 has dedicated hardware blocks containing logic for time-critical functions requiring bit or byte-time accuracy. Other functions requiring only slot-time accuracy are performed by software in the Preprogrammed Communication Controller (PCC). This approach offers maximum flexibility during prototyping.

6.1 Internal bus and data memory

6.1.1 INTERNAL BUS

The function of the internal bus is:

- To provide access for all functional blocks to the common data memory
- To provide access for the microcontroller-interface and the PCC to all other functional blocks.

All functional blocks (speech-interface, RF-interface, microcontroller-interface and PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

6.1.2 DATA MEMORY

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface. The data memory also acts as the main communication interface between the external microprocessor and the PCC.

6.2 Clock generation and correction (see Fig.4)

The device has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz for the synthesizer reference (pin REF_CLK). This output is only provided if the synthesizer power-down control (output on pin S_POWER_DWN) is not selected.
- 0.144 to 13.824 MHz for the microcontroller clock (pin PROC_CLK)
- 3.456 MHz for the ADPCM CODEC (pin CLK3)
- 1200 Hz (pin 1200_HZ) for dual synthesizer switching
- 100 Hz (pin CLK100) indicates start of frame.

Nominally, the frequency on pin CLK3 is 3.456 MHz. This frequency is obtained by dividing the crystal frequency by 4. Sometimes, the crystal frequency will be divided by 3 or by 5, to synchronize the combination of the ADPCM CODEC and the device to an external source. External synchronization for base station applications is achieved as follows:

- **Master base station**. The master base station provides a 100 Hz signal to slave base stations on pin SYNCPORT. If the PCD5042 is connected to a digital interface (32-slot mode speech interface), the external synchronization will be done on the incoming 8 kHz signal. If it is connected to an analog line (12-slot mode speech interface), it will use its own crystal oscillator as reference.
- **Slave base station**. The slave base station will use the incoming SYNCPORT signal as synchronization reference.

6.3 Programmable communication controller and program memory

6.3.1 PCC

The PCC is a RISC-type controller and is used to control functions which are slot-time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (equivalent to 3.4 Mips). After finishing a task, it switches to a power saving state, from which it returns after a pre-programmed time.

6.3.2 PCC FUNCTIONS

The most important functions of the PCC are to:

- Perform the appropriate actions on received messages: PMID and FMID checking, RFPI checking, TBC handling
- Prepare A-field messages for transmission
- Prepare the RF-interface for the coming slot
- Perform the procedures for RSSI and set-up scan, maintain scan counters and timers, assemble the RSSI field in the common data memory
- Filter events and indicate them to the microcontroller by interrupt.

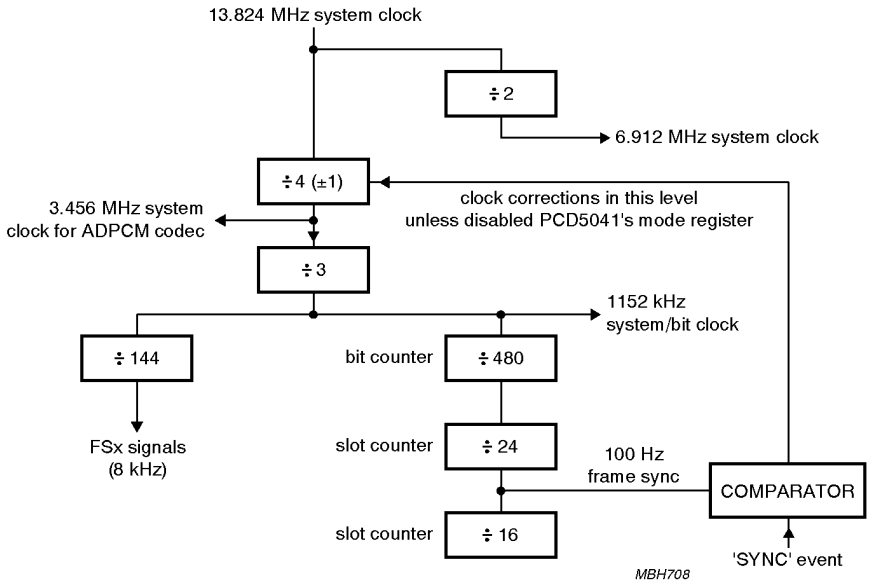

Fig.4 Internal clocking scheme of the PCD5042.

6.4 Speech interface

The speech interface block performs the following functions:

- Connection to a 1152 kbits/s interface in a handset and a simple base station in the so called '12 slot mode'
- Connection to a n x 64 kbits/s interface in base stations in the so called '32 slot mode'
- Autonomous storing/fetching of ADPCM speech data in/from the PCD5042's common data memory, using internal addressing logic
- Muting of speech data
- Local call.

6.4.1 12-SLOT MODE

The 12-slot mode is selected if up to 4 ADPCM CODECs are connected to the PCD5042, where the PCD5042 is the master of these CODECs. In a handset, or in a simple base stations which is connected with up to 4 analog lines to the public network, the PCD5042 is master of the CODECs. Each CODEC is connected with a separate framing reference signal (FS1 to FS4) to the PCD5042. In the QFP64 package, 2 framing signals FS1 and FS2 are available, whereas in the LQFP80 package 4 framing signals can be used (FS1 to FS4). When more CODECs are to be connected, the FS5 to FS12 signals have to be generated externally. When using the framing signals FS1 to FS4, no interface logic is required when using the PCD5032 ADPCM CODEC.

A speech-slot control table is used to determine where to store/fetch speech data for transmission and reception. The hardware speech-interface is capable of addressing the right speech buffer for the relevant speech slot, and will maintain a counter carrying the offset to the correct stored/fetched address.

6.4.2 32-SLOT MODE

The 32-slot mode is used to connect the PCD5042 to a digital interface with a data rate of n × 64 kbits/s; where n = 1 to 32 is the number of speech slots. This equates to data rates from 64 kbits/s to 2048 kbits/s.
Up to 12 of the 32 speech slots can be used simultaneously. The same kind of speech-slot control table used in the 12-slot mode is used for the 32-slot mode.

6.4.3 MUTING

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech

data, these disturbances are not audible (or are less audible) to the user. The PCD5042 performs two types of muting:

- Fast muting
- Slow muting.

Fast muting, which is performed by the PCD5042 automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM CODEC. It is issued if no Sync word was detected. Slow muting is issued by the microcontroller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM CODEC, until slow mute is released.

6.4.4 LOCAL CALL

A local call option is implemented, in order to loopback data from one CODEC to another CODEC, and vice versa, see Fig.5.

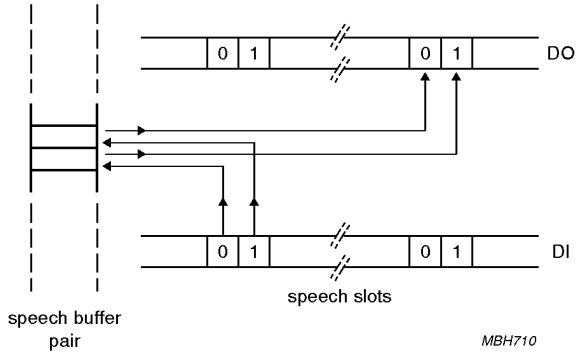

Fig.5 Local call switching on speech interface.

6.5 RF interface

Most of the functions performed by the RF interface are under control of the PCC. Specifically, the processing of non-speech data and the programming of functions and registers is done via the PCC.

6.5.1 SERIAL RECEIVER

The serial receiver processes the data, which comes from the RF section, and which is already filtered by the synchronization part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In Fig.6 the data flow in the serial receiver is shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a ciphered message is being received or transmitted, which requires the ciphering to be switched on in the A-field also.

6.5.2 SERIAL TRANSMITTER

The serial transmitter performs the reverse of the receiver functions. Several blocks used in the receiver are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 7 shows the serial transmitter structure.

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronization sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory and will be fetched by the transmitter, just before transmission.

Two additional functions are not shown in Fig.7:

- In the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the RF section
- The transmitted data can be inverted (using a switch in the PCD5042 mode register), in order to connect the PCD5042 to VCOs requiring negative modulation.

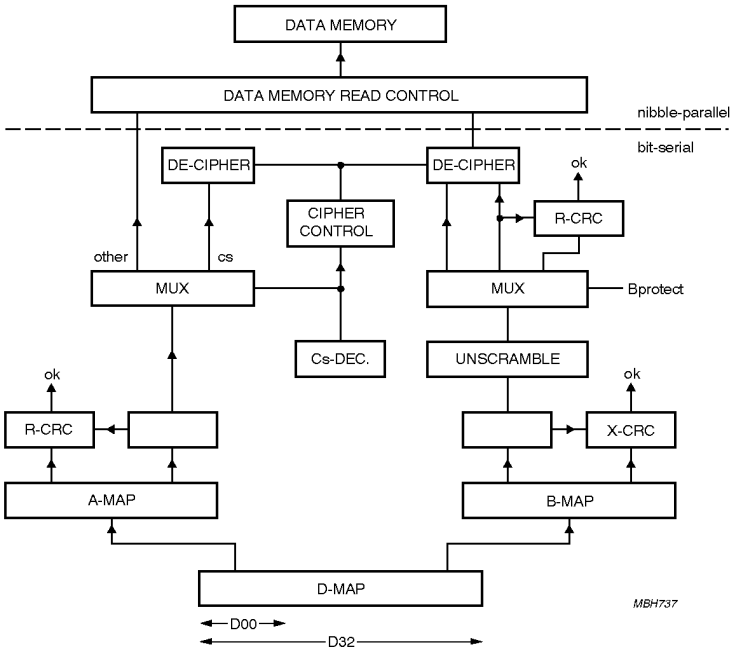

Fig.6 Serial receiver structure.

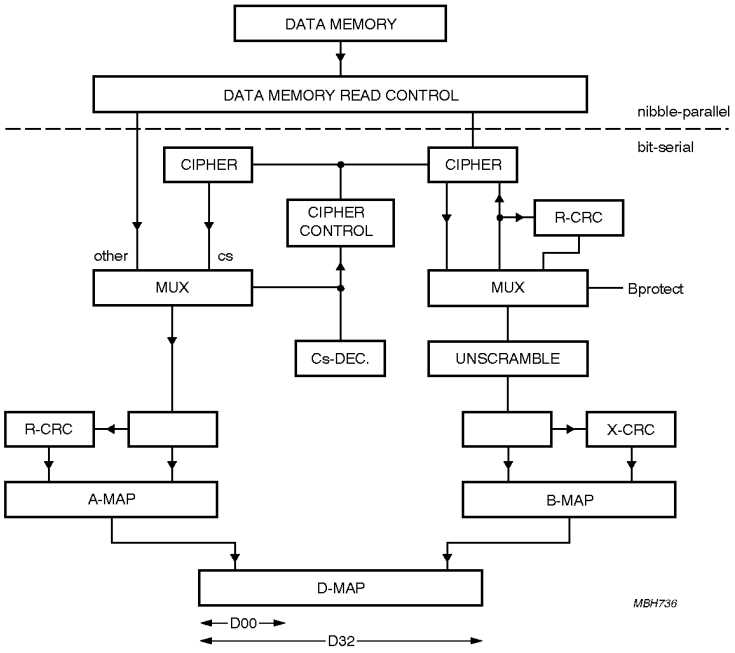

Fig.7 Serial transmitter structure.

6.5.3 SEAMLESS HANDOVER

Seamless handover guarantees that when speech information is switched from one slot to another, no speech samples are lost, added or displaced. Seamless handover is achieved in the RF interface by:

- Using a look-up table containing the correct start addresses of the B-fields in the data memory
- The RF receive and transmit blocks move data to/from the data memory block in 4-bit nibbles.

6.5.4 RF CONTROL SIGNALS

The timing of the control signals to the RF section is fixed, but such that an RF delay between 1.5 and 7 μs can be tolerated. Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

6.5.5 SYNTHESIZER PROGRAMMING

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data).

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8, 16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

6.5.6 RSSI MEASUREMENT (see Fig.8)

The RSSI measurement in the PCD5042 RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control unit, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

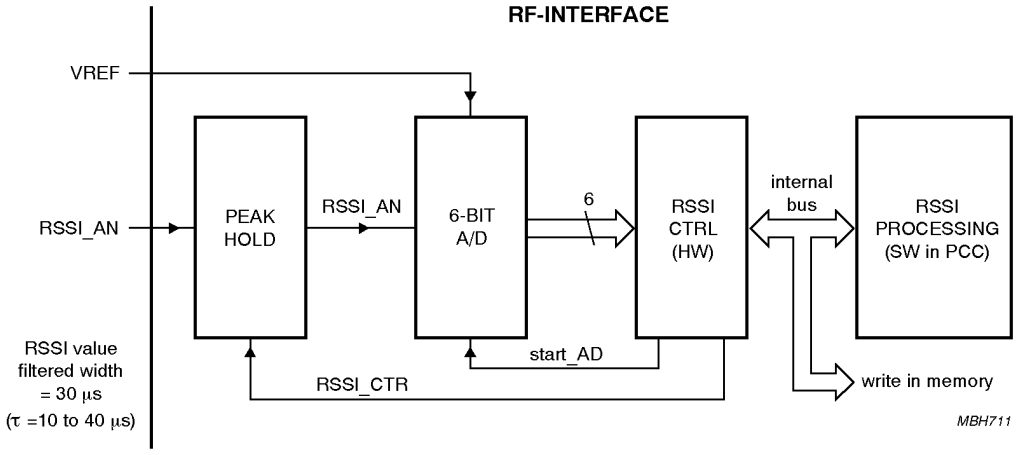

Fig.8 RSSI measurement path.

6.5.7 LOCAL CALL SWITCHING (see Fig.9)

The PCD5042 provides a local call switching function in the base station. It will store incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it passes the start pointer of the same data memory area to the transmit block. Thus, the speech data is echoed to the other user. To handle quality degradation for local calls, a mute can be performed at the RF side of the speech buffer.

6.5.8 DATA SYNCHRONIZATION (see Fig.10)

The data synchronization is done in 2 phases:

- Bit synchronization
- Sync word detection.

Bit synchronization is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running at 12 times the data rate. The output from the DPLL is a receive clock signal (RxC), which acts as the enable for a 20-bit shift register.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronization field pattern, using a correlator.
The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means that 'SlotSync', which indicates the slot synchronization event, can be detected only during a certain period (the time window).

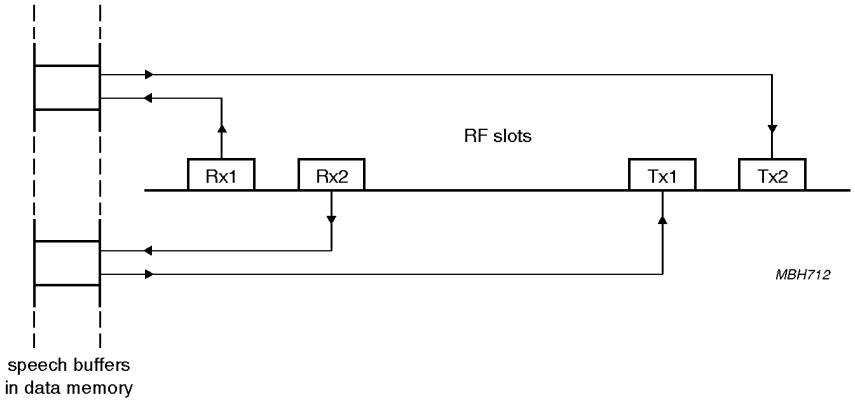

Fig.9 Local call switching on the RF-side.

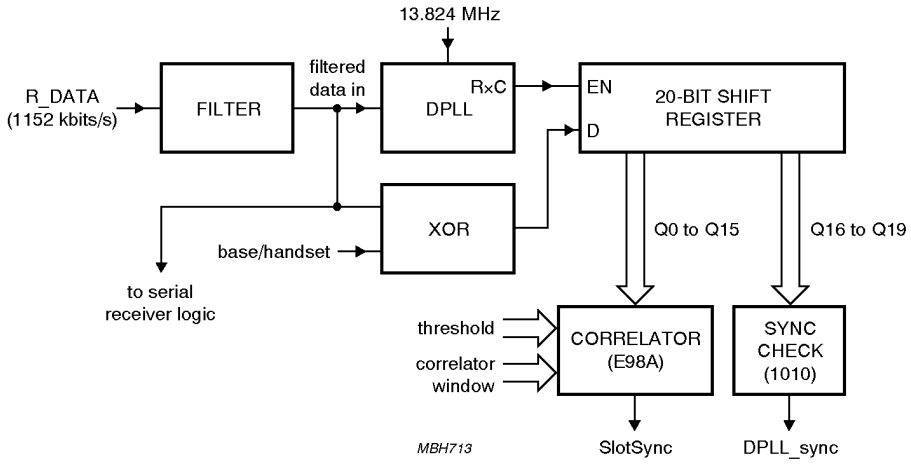

Fig.10 Schematic of the receiver synchronization part.

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the pre-amble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronized) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a 'fast mute' because speech data received in the previous frame is not destroyed.

6.5.9 CIPHERING MACHINE

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI under the terms of a Non-Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:

- A_cipher (40 bits) for A-field messages (ciphers tail only)
- B_cipher (320 bits) for speech in B-field.

The transmitted ciphered bits are then:

- A_ciphered: = A XOR A_cipher
- B_ciphered: = B XOR B_cipher.

On reception by the peer end point, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

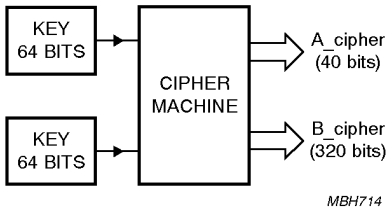

Fig.11 Cipher machine and its sources.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external microprocessor.

6.5.10 COMPARATOR/DATA SLICER ON PCD5042HZ

The PCD5042HZ contains a comparator/data slicer. The comparator is a stand-alone circuit. No connections other than power supply are made internally.
The comparator can be used as a data slicer for the receiver input. The delay requirements listed in Chapter 8 were derived from this application. Another use of the comparator is in a successive approximation A/D converter to indicate battery low-voltage condition, or in a power-on-reset circuit.

When the signal $\overline{\text{COMP\_NE}}$ is LOW the comparator is enabled. When $\overline{\text{COMP\_NE}}$ is HIGH the comparator is disabled, and the circuit consumes no power. If the comparator is used as a data slicer for the receiver input, the R_DATA is connected to COMP_OUT, the $\overline{\text{COMP\_NE}}$ is connected to $\overline{\text{R\_ENABLE}}$, both connection are done externally. The pin COMP_INP is connected to the RF mixer. A proper bias voltage (from the slicer time constant control circuit) is connected to COMP_INM. Another use of the comparator is in a successive approximation A/D converter for battery voltage detection.

The pins are protected against ESD damaging, with a protection diode to the positive and negative supply rail. The input pin $\overline{\text{COMP\_NE}}$ has a pull-up resistor which keeps the comparator in power-down mode by default.

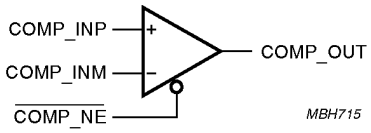

Fig.12 Circuit schematic of the comparator/data slicer.

6.6 Microcontroller Interface

6.6.1 Function of the microcontroller interface

The microcontroller Interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface
- General interface to processors that can handle 'wait states' e.g. 68000-family; in this case glue logic is required
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load
- A programmable interrupt register
- A watchdog timer with time-out periods of 1.25 or 82 seconds, depending on the programming.

The microcontroller can address the PCD5042 as any other RAM memory connected to the microcontroller bus. By writing the 'Interface-Mode Register', the microcontroller can select the interface mode and its own clock frequency.

6.6.2 Microcontroller interrupts

The function of microcontroller Interrupts is to make optimal use of the microcontroller's processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register.

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the corresponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

6.6.3 Watchdog

The PCD5042 is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a μC) after time-out. Two (fixed) time-out periods can be programmed; 1.25 s and 82 s. The watchdog function can be disabled by using the EN_WATCHDOG input pin.

6.6.4 Power-down

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power-down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, microcontroller interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power-down the external microcontroller has still access to the common data area.

6.7 Survey of registers

For a survey of all addresses occupied refer to Tables 1 and 2. Some of the address locations are used differently for read and write. The addresses 000 to 7DF are occupied by RAM memory, while the upper 32 bytes are assigned to the hardware registers. A part of the RAM memory is allocated for use by the RF block, cipher block, and the speech interface.

Table 1 Hardware register addresses

ADDRESS	WRITE	READ
7E0	–	–
7E1	S-DATA1	–
7E2	S-DATA2	–
7E3	S-DATA3	RMT-STAT
7E4	–	RF-STATUS
7E5	B-field-shift	–
7E6	B-field-loc.	–
7E7	A-field-loc.	–
7E8	window-wide-off	–
7E9	window-wide-on	–
7EA	window-narrow-off	–
7EB	window-narrow-on	–
7EC	T-power-rmp-on	–
7ED	synth-off	–
7EE	RF-control-port	sync-status
7EF	slot-cnt-off	slot-counter-copy
7F0	frame-cnt-ref	RSSI
7F1	sync-ref-preset	bit-counter-copy1
7F2	bit-counter-preset	bit-counter-copy2
7F3	frame-counter	frame-counter
7F4	slot-counter	slot-counter
7F5	sync-control	sync-control
7F6	BMC-mode	BMC-mode
7F7	correlator-threshold	measure
7F8	watchdog-1	–
7F9	watchdog-2	–
7FA	–	–
7FB	–	–
7FC	interrupt-event	interrupt-event
7FD	interrupt-enable	interrupt-enable
7FE	interrupt-reset	–
7FF	controller mode	controller mode

Table 2 Fixed RAM locations

ADDRESS	ENTRY
740 to 747	cipher key vector #0
748 to 74F	cipher key vector #1
750 to 757	cipher key vector #2
758 to 75F	cipher key vector #3
760 to 767	cipher key vector #4
768 to 76F	cipher key vector #5
770 to 777	cipher key vector #6
778 to 77F	cipher key vector #7
780 to 787	cipher key vector #8
788 to 78F	cipher key vector #9
790 to 797	cipher key vector #10
798 to 79F	cipher key vector #11
7A0 to 7A7	cipher init vector
7A8 to 7AA	not used
7AB	XZ field buffer
7AC to 7AF	S-field buffer
7B0 to 7BB	cipher-slot-control-table
7BC to 7BF	not used
7C0 to 7DF	speech-slot-control-table

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_i	all input voltages	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	–	+500	mW
P_O	power dissipation per output	–	30	mW
I_{DD}	supply current	–100	+130	mA
I_{SS}	ground current	–100	+130	mA
T_{stg}	storage temperature range	–55	+100	°C
T_j	operating junction temperature	–	90	°C

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
T_{amb}	operating ambient temperature		–25	–	+70	°C
V_{DD}	supply voltage		2.7	–	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	–	V_{DD}	V
I_{DD}	operating supply current	note 1	–	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	–	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	–	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current				1.0	μA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤V_O ≤ V_{DD} – 0.4 V	2.0	5.0	–	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤V_O ≤ V_{DD} – 0.4 V	2.0	5.0	–	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	–	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	–	6.0	–	mA
f_{DCK}	DCK input frequency	n = 1 to 32	–	n × 64	–	kHz
f_{FS1}	FS1 input frequency		–	8	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	–	–	mS
		V_{DD} = 3.6 V	–	1.6	–	mS
R_F	feedback resistance		200	500		kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	–	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	–	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	–	50	–	kΩ
t_{conv}	conversion time		18.4	–	–	μs
	integral non-linearity		–	–	4	LSB
	differential non-linearity	note 3	–	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		–	1	–	MΩ
PCD5042HZ comparator characteristics						
$I_{DD(stb)(comp)}$	supply current (standby)	note 4	–	10	–	μA
$I_{DD(idle)(comp)}$	supply current (idle)	V_{DD} = 3.0 V; note 4	–	135	–	μA
$I_{DD(1MHz)}$	supply current (1 MHz)	V_{DD} = 3.0 V; note 4	–	350	–	μA
$I_{LI(comp)}$	input leakage current	note 5	–	–	1	μA
C_i	input capacitance	note 5	–	10	–	pF
R_{pu}	pullup resistance	note 6	–	200	–	kΩ
V_{cm}	input common mode range	note 7	1.0	–	V_{DD} – 0.5	V
V_{os}	max. input offset voltage	note 8	–	5	–	mV
t_{pd}	propagation delay	note 9	–	100	200	ns
Δt_{pd}	delay difference	note 8 and 9	–	10	–	ns
$V_{OL(comp)}$	output level LOW	I_O = 2 mA	–	–	0.4	V
$V_{OH(comp)}$	output level HIGH	I_O = 2 mA	V_{DD} – 0.4	–	–	V
t_r	output rise time	C_L = 50 pF	–	15	–	ns
t_f	output fall time	C_L = 50 pF	–	15	–	ns
t_{en}	enable time		–	–	8	μs

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.
4. Supply current $I_{DD(stb)(comp)}$ flows when $\overline{COMP\_NE}$ is HIGH.
   Supply current $I_{DD(idle)(comp)}$ flows when the comparator is in active mode ($\overline{COMP\_NE}$ is LOW). It is the DC current of the comparator when it is not switching, and V(COMP_INP) < V(COMP_INM).
   The active mode supply current $I_{DD(1MHz)}$ includes the output pulse rate of 1 MHz.
5. For input pins COMP_INP, COMP_INM, $\overline{COMP\_NE}$.
6. For input pin $\overline{COMP\_NE}$.
7. The minimum input common mode voltage will be measured at DC levels with, COMP_INM at 1 V DC ±30 mV. The same goes for the maximum input common mode voltage at (V_{DD} – 0.5V).
8. These values are not tested in production, and are based upon theoretical estimates and laboratory tests.
9. The propagation delay t_{pd} is measured from the time the differential input voltage equals the offset voltage, to the 50% point of the output transition. The initial differential input voltage is 100 mV and the propagation delay is specified for an input overdrive of 30 mV, and a load capacitance of 50 pF. t_{pd} is valid for both the positive and negative going output transition. The maximum value is valid for the total ranges of temperature, supply voltage and common mode input voltage. The worst case operation conditions are at the minimum supply voltage, the lowest operating temperature and the minimum input common mode voltage. The delay difference Δt_{pd} gives the difference between t_{pd} for the rising output transition and t_{pd} for the falling output transition and is valid for all operating conditions. The test method to check the maximum delay difference is by measuring the RMS voltage of the output signal.