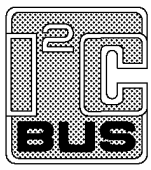
DECT baseband controllers PCD5091; PCD5092

FEATURES

- The PCD509x is designed for GAP-compliant handsets and base stations
- Embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).
- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. External program memory is addressable up to 128 kbytes (PCD509x/xxx).
- +5 V port (P0 to P3) interface
- Portable Part (PP) and Fixed Part (FP) modes
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot.
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for frequency adjustment of 13.824 MHz on-chip crystal oscillator
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface



- IOM interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable timing of radio-control signals
- Programmable polarity of radio-control signals
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- GMSK pulse shaper
- On-chip comparator for use as bit-slicer
- Power-on reset
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

DSP software features

- ADPCM encoding and decoding complying with G.721
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Dial tone detection
- Echo cancellation
- Automatic gain control
- Telephone Answering Machine (TAM) switch
- Hands-free operation (PCD5091 and PCD5093)
- Conference call (PCD5094).

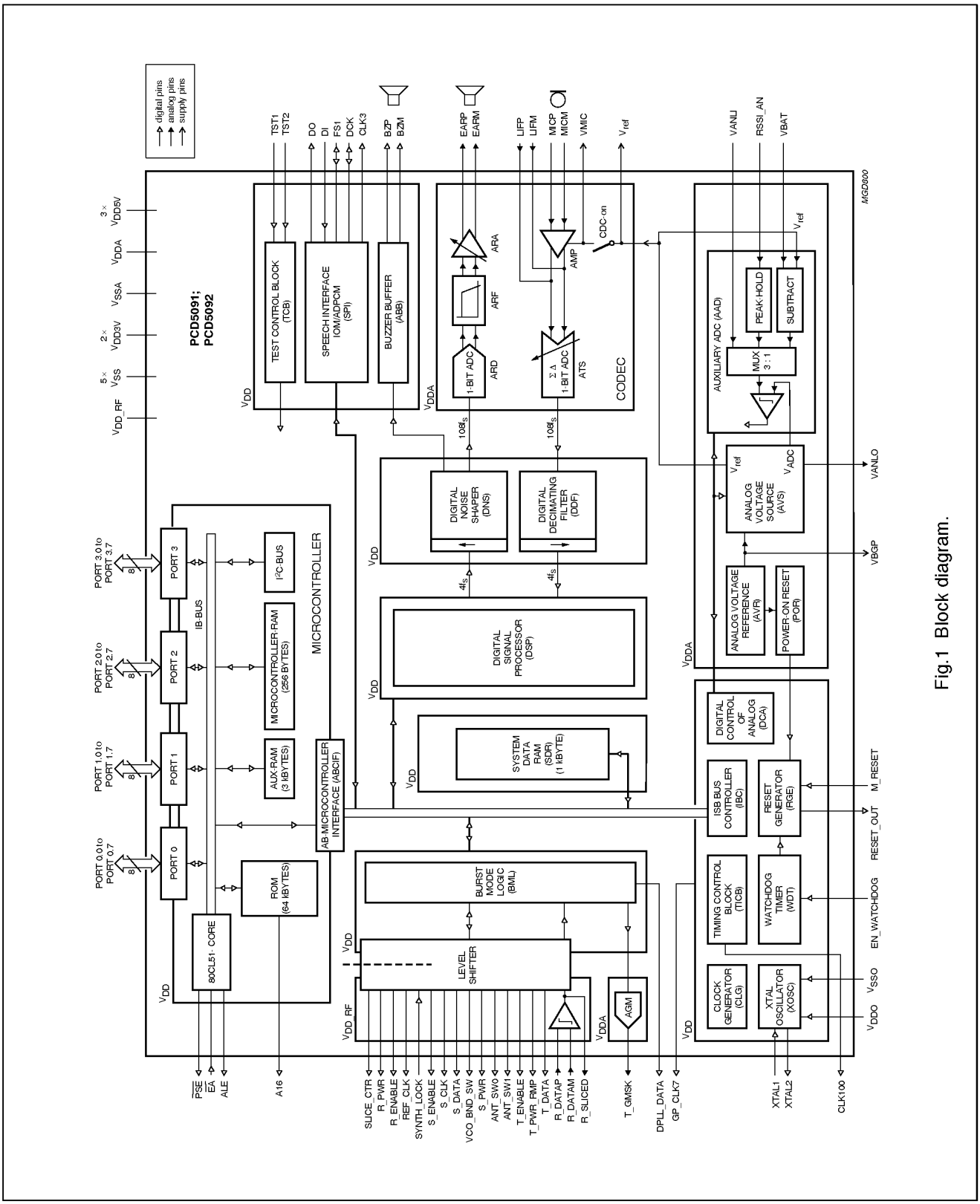
For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set.

For further information please contact Philips Semiconductors.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5091HZ	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
PCD5091H PCD5092H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

BLOCK DIAGRAM



PINNING

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
ANT_SW1	1	99	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	100	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	1	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	2	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	3	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	4	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	5	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	6	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	7	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	8	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	9	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	10	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	11	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	12	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	13	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	14	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	15	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	16	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	17	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	18	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	19	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	20	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	21	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	22	I	–	ANAIOD1	analog input to ADC
VBAT	25	23	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	24	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	25	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	26	I	–	DIPP0PES	ADPCM or IOM data input

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
FS1	29	27	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	28	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	29	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	30	I	–	ANAIOD1	crystal oscillator input
VANLO	33	31	O	1.0 V	ANAIOD1	analog output from D/A converter
V_{SSO}	34	32	I	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	33	I	–	supply	positive supply voltage for the oscillator
LIFM	36	34	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	35	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	36	–	–	supply	negative supply voltage for analog circuits
MICM	39	37	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	38	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	39	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	40	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	41	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	42	–	–	supply	positive supply voltage for analog circuits
EARM	45	43	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	44	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	45	I	–	DIUP0PES	watchdog enable input
P1.0	48	46	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	47	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	49	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	50	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	51	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	52	I	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	53	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	54	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
P1.6	58	56	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	57	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	58	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	59	O	L	ANAIOD2	negative buzzer output
BZP	62	60	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	61	–	–	supply	negative supply voltage 2
V_{SS3}	64	62	–	–	supply	negative supply voltage 3
P3.0	65	63	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	64	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	74	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	75	I	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	76	I	–	supply	negative supply voltage 4
TST1	79	77	I	–	DIDP0PES	test input 1
TST2	80	78	I	–	DIDP0PES	test input 2
P2.3	81	79	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	80	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	84	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	85	O	H	ISQ4CPES	address latch enable (80C51)

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
$\overline{EA}$	88	86	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	87	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	88	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	89	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	90	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	97	I	–	DIDP0PES	master reset input (Schmitt-trigger)
RESET_OUT	100	98	O	H	ISF2DPES	reset output

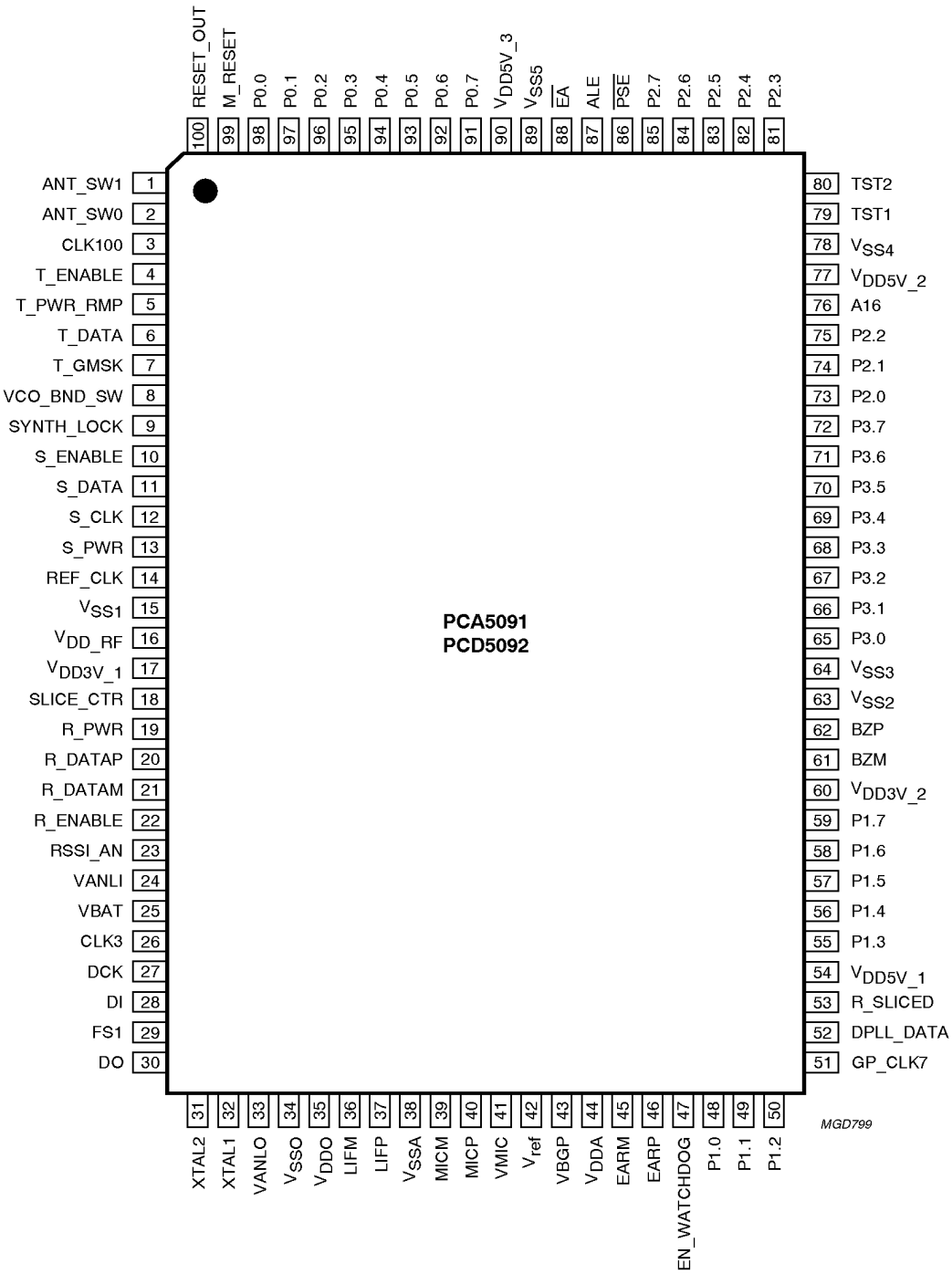


Fig.2 Pin configuration (QFP100).

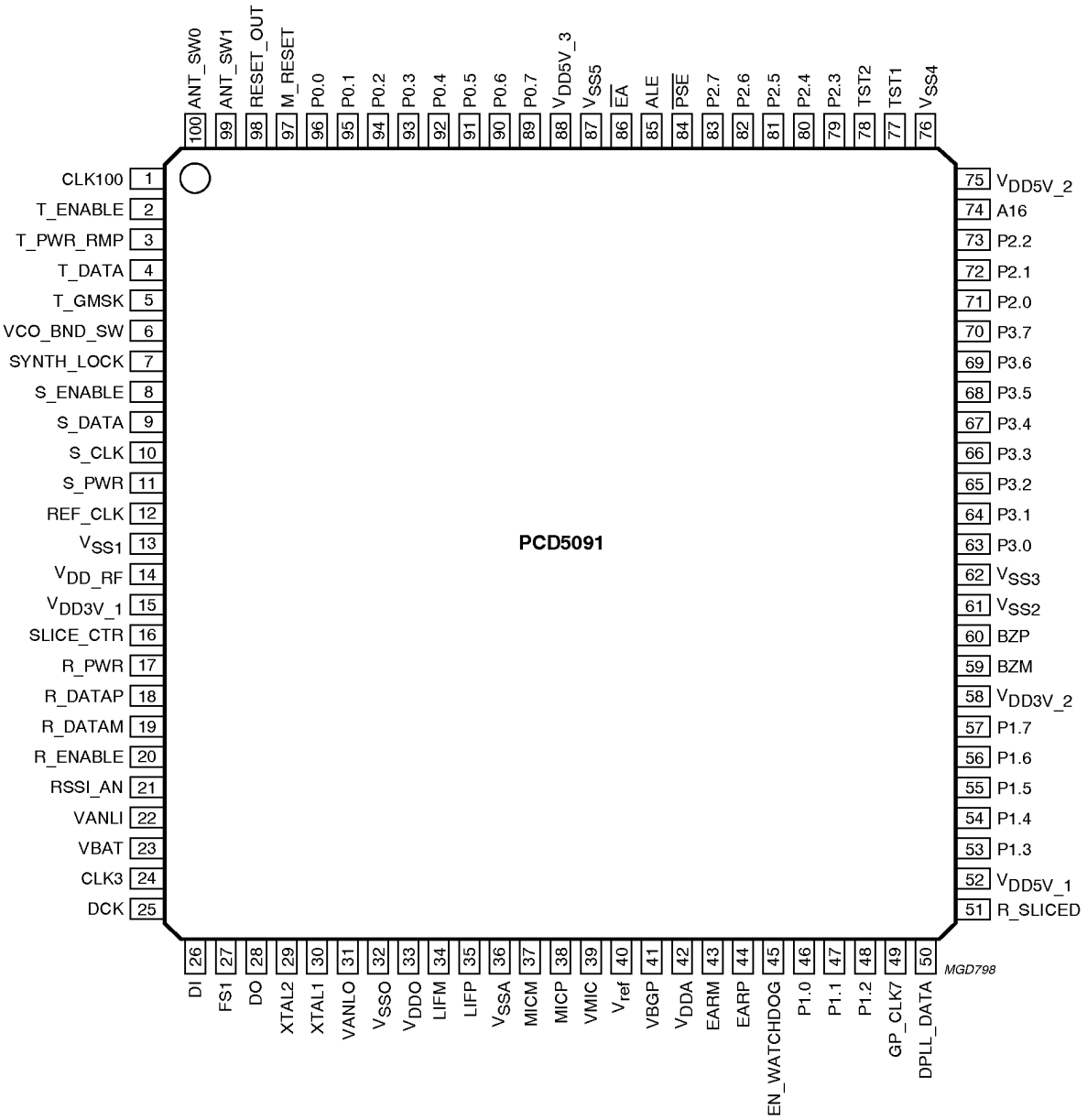
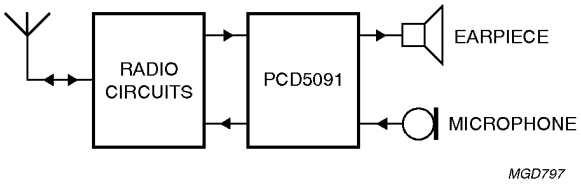


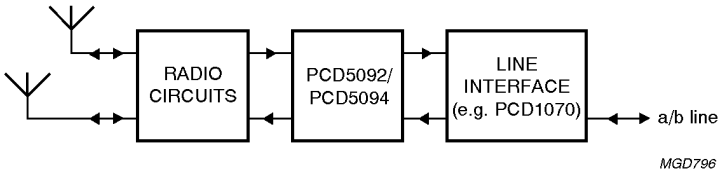
Fig.3 Pin configuration (LQFP100).

FUNCTIONAL DESCRIPTION

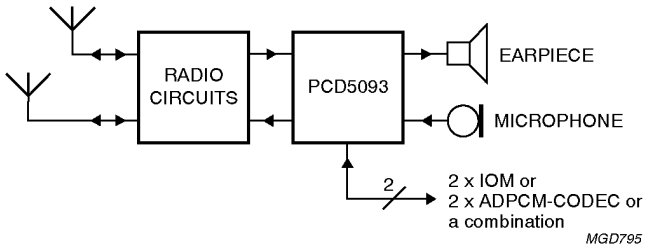
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I^2C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Base with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.4 Block diagrams of DECT systems with PCX509x.