

Threshold detector and reset generator

PCF1252-X family

FEATURES

- Very low current consumption, typically 10 μ A
- 10 factory programmed threshold voltages available covering trip voltages from 4.75 to 2.55 V
- ± 50 mV trip point accuracy over full temperature range
- Variable RESET delay
- RESET pulse polarity selection
- Defined outputs at 0.6 V (typ.)
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power fail
- Operating temperature range -40 to $+85$ °C.

GENERAL DESCRIPTION

The PCF1252-Xs are low-power CMOS voltage threshold detectors designed especially for supervision of microcontroller/microprocessor systems for detection of power-on/off conditions and generation of a system reset pulse. The PCF1252-X also provides a $\overline{\text{POWF}}$ (power fail) output which is activated at a precise factory-programmed trip point. A system RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}).

A second comparator (comparator 2) has been included to enable the possibility of a second monitoring point in the system.

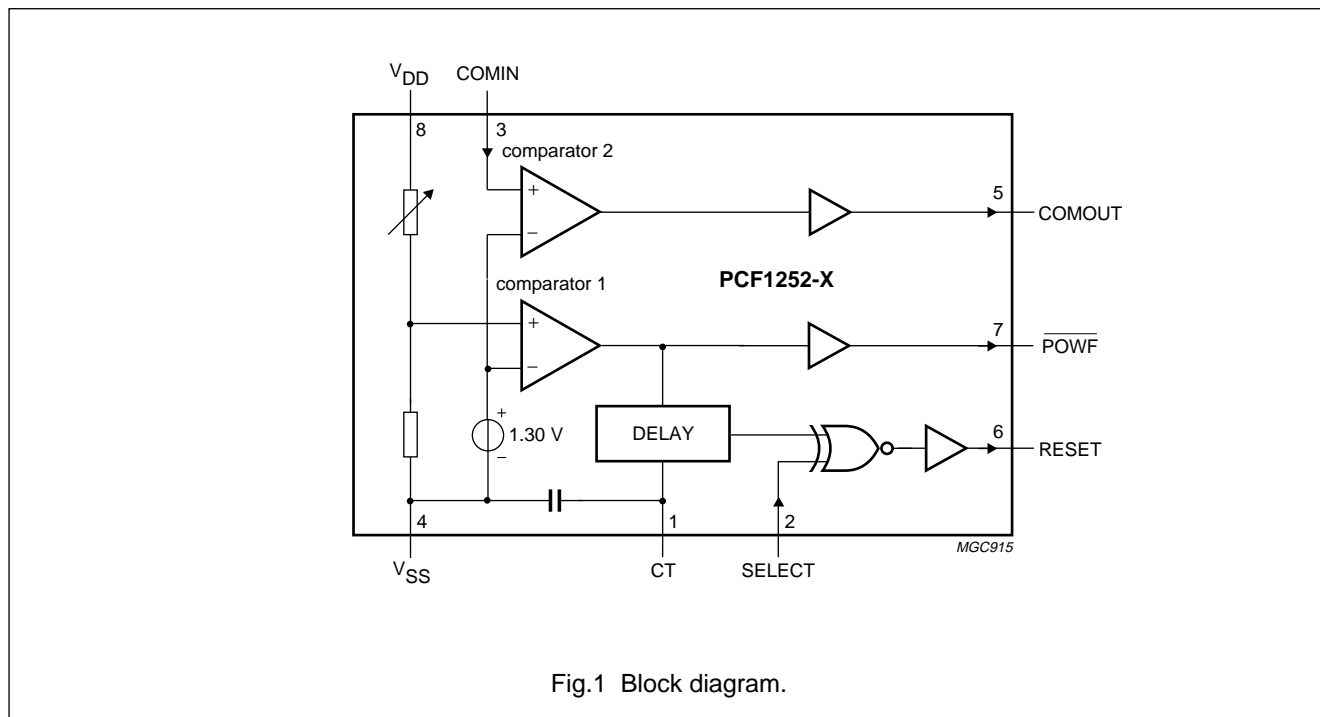
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1252-XP ⁽¹⁾	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF1252-XT ⁽¹⁾	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Note

1. X = 0 to 9; depending on threshold voltage.

BLOCK DIAGRAM

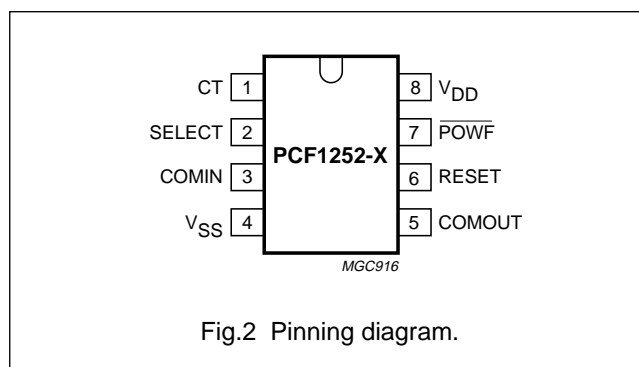


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PINNING

SYMBOL	PIN	DESCRIPTION
CT	1	connection for the external capacitor
SELECT	2	select polarity or external reset input
COMIN	3	comparator input
V _{SS}	4	ground (0 V)
COMOUT	5	comparator output
RESET	6	reset output
$\overline{\text{POWF}}$	7	power failure signal output
V _{DD}	8	supply voltage



FUNCTIONAL DESCRIPTION (see Fig.1)

The PCF1252-X contains:

- A precise factory-programmed voltage reference
- Two comparators
- A delay circuit.

The PCF1252-X family is comprised of 10 versions with different factory-programmed voltage trip-points (V_{TRIP}), see Chapter “Characteristics”.

Supply

The supply voltage (V_{DD}) is internally divided before being compared, via comparator 1, with the internal reference voltage.

 $\overline{\text{POWF}}$ (see Fig.3)

The $\overline{\text{POWF}}$ output is:

- LOW, if V_{DD} is below V_{TRIP}
- HIGH, if V_{DD} is above V_{TRIP} .

Power-on reset (SELECT = LOW)

As V_{DD} rises past V_{TRIP} , a positive reset pulse is generated at RESET. The duration of the reset pulse (t_{R}) is determined by the value of the external capacitor (C_{CT} ; maximum 1 μF , see Fig.8) connected to CT. With no external capacitor connected, C_{CT} assumes a minimum value of 100 pF. If SELECT is HIGH, the reset pulse is inverted.

Power failure

During a power-off condition ($V_{\text{DD}} < V_{\text{TRIP}}$), $\overline{\text{POWF}}$ goes LOW. After a time delay (t_{S}), also determined by C_{CT} , RESET goes HIGH. Any $\overline{\text{POWF}}$ assertion ($V_{\text{DD}} < V_{\text{TRIP}}$) will result in a subsequent RESET pulse.

Voltage trip-point

By selecting the voltage trip-point slightly higher than the minimum operating voltage of the microcontroller/microprocessor, there is sufficient time for data storage before the power actually fails.

In order to prevent oscillations around the voltage trip-point, a small hysteresis has been included, resulting in a power-on switching point that is higher than the voltage trip-point (minimum of 15 mV). The voltage trip-point refers to the value at which power-off is signalled.

COMIN

Input to the second comparator (comparator 2). When used in conjunction with an external voltage divider, this allows a second point in the system to be monitored. This input has no built-in hysteresis. When not in use connect to V_{DD} . COMOUT will be LOW or HIGH depending on the voltage at COMIN:

- COMOUT = HIGH, if voltage at COMIN is above the switch point V_{SP} (typically 1.30 V).
- COMOUT = LOW, if voltage at COMIN is below the switch point V_{SP} (typically 1.30 V).

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_I	DC clamp-diode current	all pins: $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	20	mA
I_O	output current		-	20	mA
P_{tot}	total power dissipation		-	150	mW
T_{stg}	storage temperature		-65	+100	°C
T_{amb}	operating ambient temperature		-40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD} = 2.4$ to 6.0 V; $V_{SS} = 0$ V; $T_{amb} = -40$ to $+85$ °C; (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.4	-	6.0	V
V_{TRIP}	Voltage trip-point: PCF1252-0 PCF1252-1 PCF1252-2 PCF1252-3 PCF1252-4 PCF1252-5 PCF1252-6 PCF1252-7 PCF1252-8 PCF1252-9	$T_{amb} = 25$ °C	4.70 4.50 4.20 4.00 3.70 3.50 3.20 3.00 2.70 2.50	4.75 4.55 4.25 4.05 3.75 3.55 3.25 3.05 2.75 2.55	4.80 4.60 4.30 4.10 3.80 3.60 3.30 3.10 2.80 2.60	V V V V V V V V V V
I_{DD}	supply current	$T_{amb} = 25$ °C; $V_{DD} = V_{TRIP} + 0.5$ V; $COMIN = V_{DD}$; see Figs. 4 and 5	-	10	15	μA
ΔV_{TRIP}	voltage trip-point temperature coefficient	note 1	-	$\pm 100 \times 10^{-6}$	$\pm 400 \times 10^{-6}$	mV/K
V_{hys}	voltage trip-point hysteresis		15	30	50	mV

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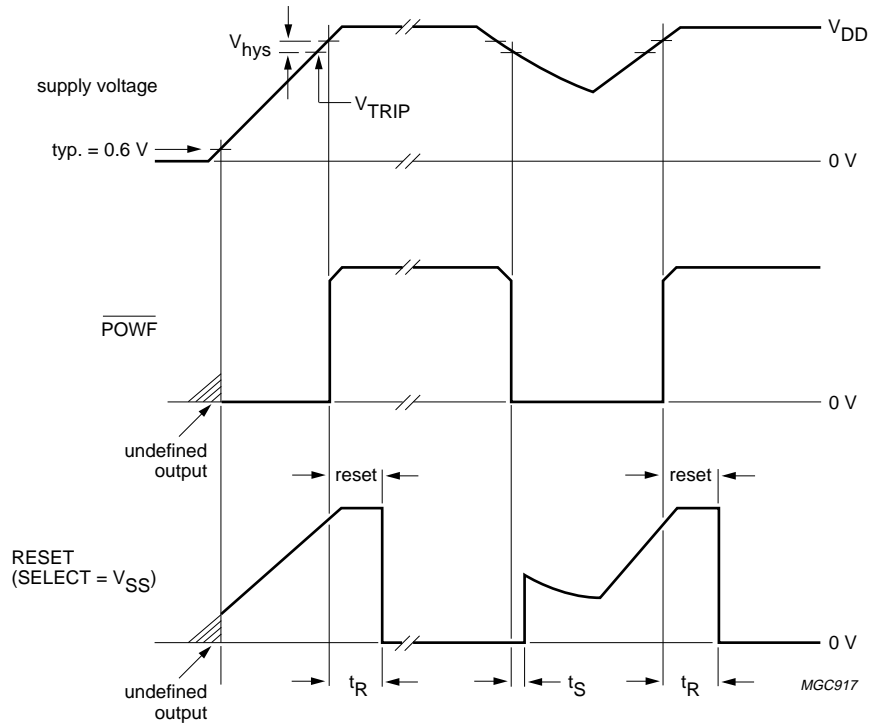
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
COMIN						
V_{SP}	COMIN switch point	$T_{amb} = 25\text{ °C}$	1.28	1.30	1.32	V
ΔV_{SP}	COMIN switch point temperature coefficient	note 1	–	± 0.1	± 0.5	mV/K
SELECT						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
SELECT and COMIN						
I_{LI}	LOW level leakage input current		–	–	–1.0	μA
I_{LI}	HIGH level leakage input current		–	–	1.0	μA
POWF, RESET and COMOUT						
I_O	output sink current	$V_O = 0.4\text{ V};$ $V_{DD} = 2.4\text{ V};$ see Fig.6	1	3	–	mA
I_O	output source current	$V_O = 2.0\text{ V};$ $V_{DD} = 2.4\text{ V};$ see Fig.7	–0.75	–2	–	mA
t_R	reset time	$C_{CT} = 1\text{ nF};$ note 2	400	1000	2000	μs
t_S	save time	$C_{CT} = 1\text{ nF};$ note 2	40	100	200	μs
t_R/t_S	reset to save time ratio		–	10	–	
C_{int}	CT internal capacitance		–	100	–	pF

Notes

1. Values given per degree Kelvin; tested on a sample basis.
2. Conformance to these specifications is only guaranteed if the slew rate of V_{DD} is less than 25 V/ms.

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t_R = reset time (duration of reset pulse).

t_S = save time (time between assertion of \overline{POWF} and assertion of the reset output). This time can be used for storing of critical data and orderly system shut-down.

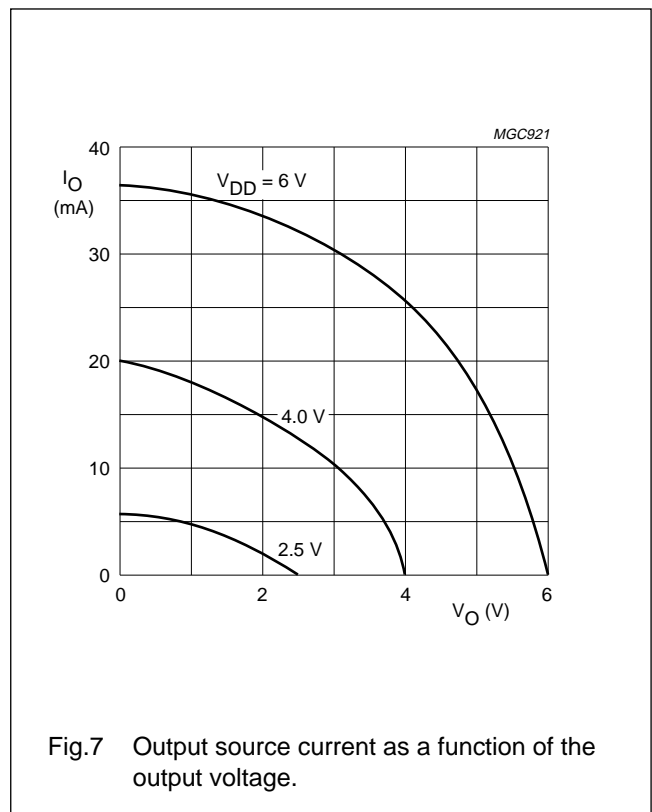
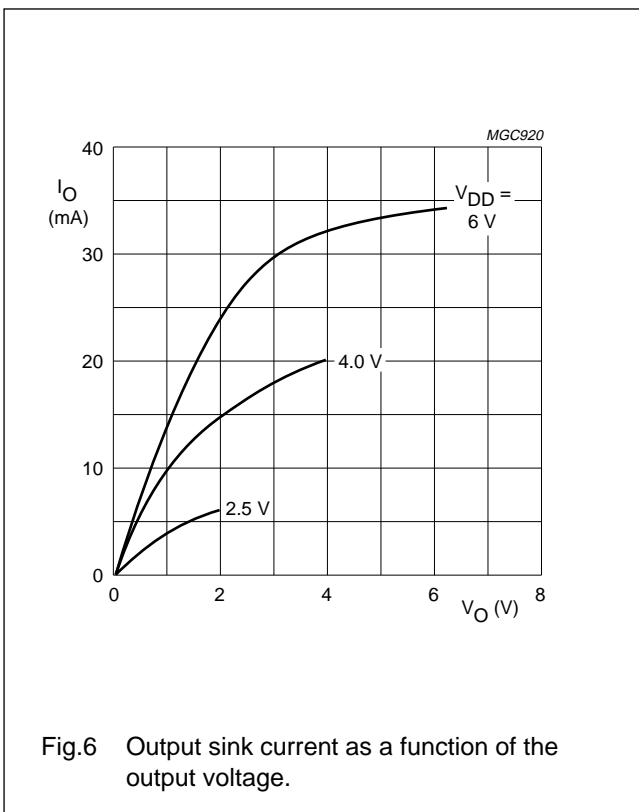
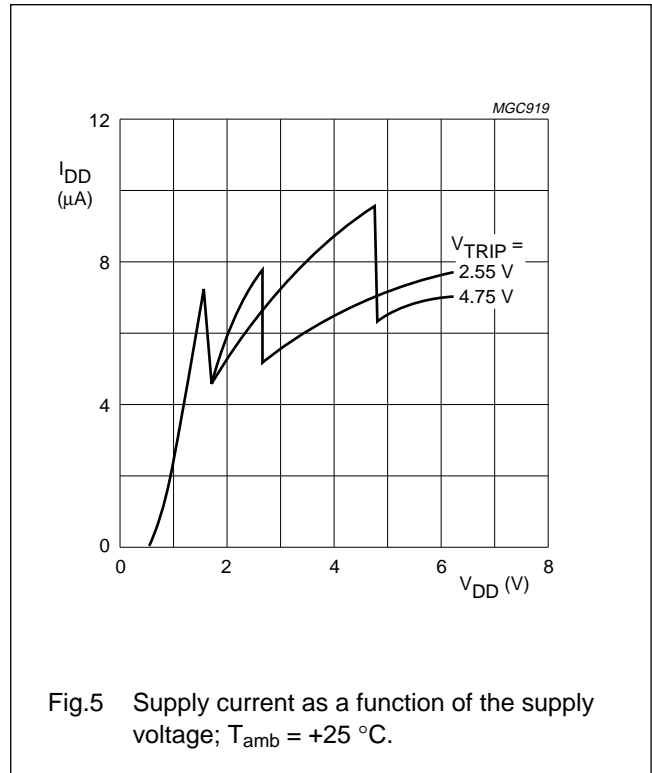
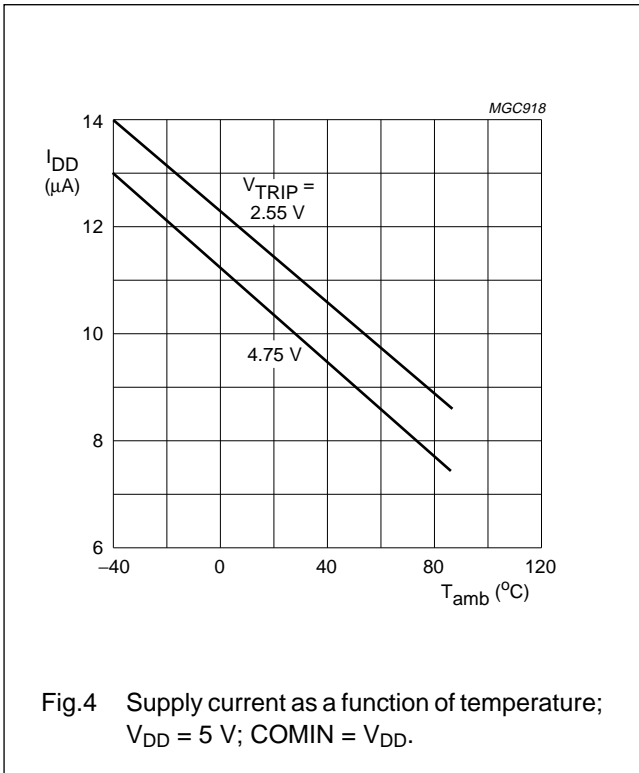
V_{hys} = hysteresis voltage (prevents oscillation around V_{TRIP}).

Fig.3 Timing diagram.

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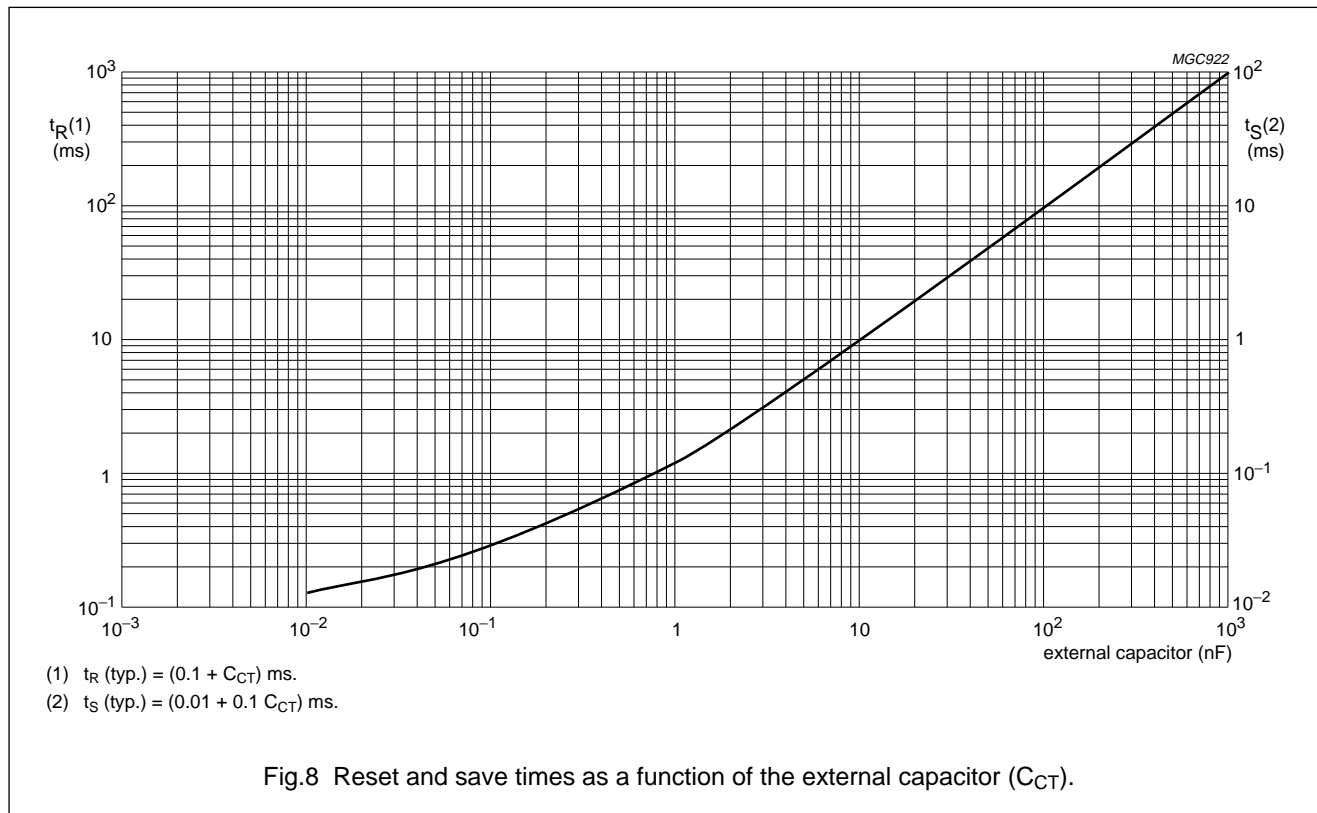
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Typical performance characteristics

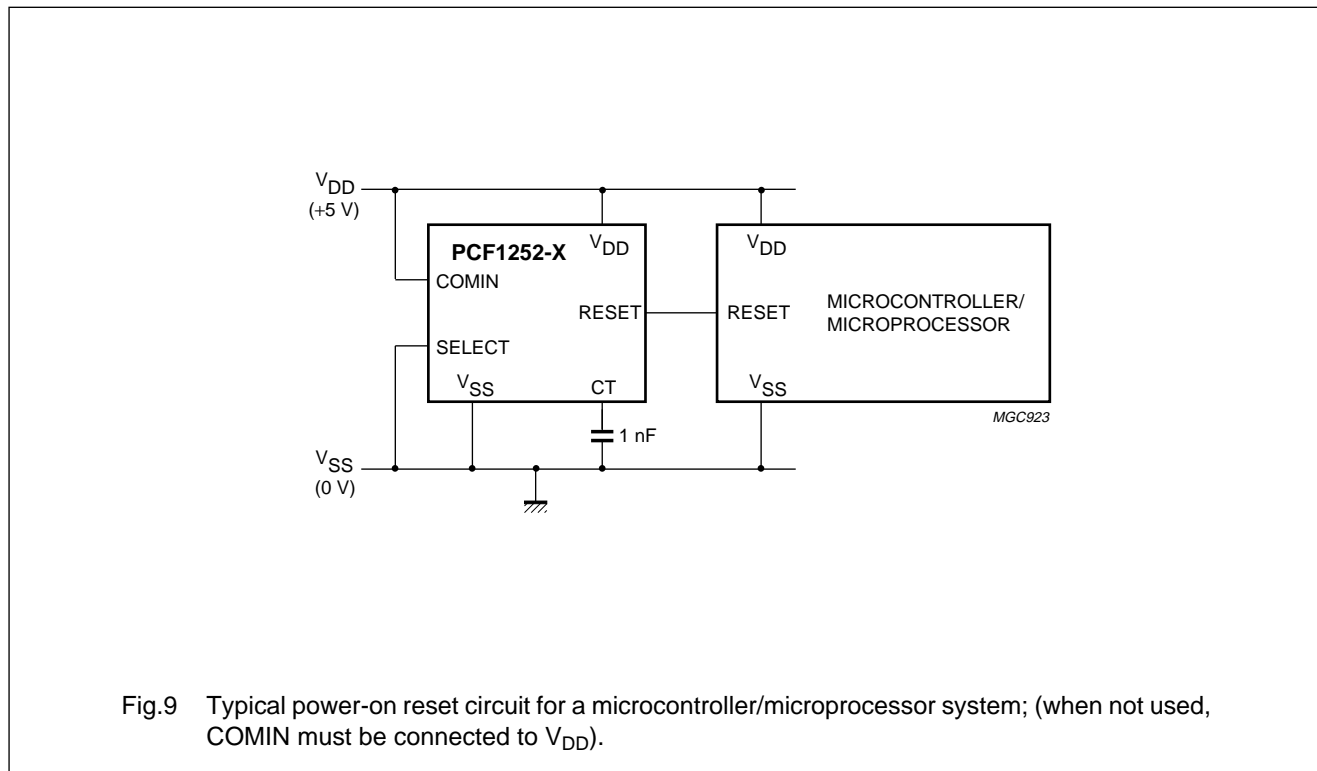


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APPLICATION INFORMATION



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