LCD controller/driver PCF2104 family

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2104 integrated circuit is similar to the PCF2114 but does not contain the high voltage generator. It is optimized for chip-on-glass applications. The letter X in PCF2104X specifies the character set in the Character Generator ROM (CGROM). The different character sets currently available are specified by the letters C and L. Other character sets are available on request.

The PCF2104 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104 interfaces to most microcontrollers via a 4 or 8-bit bus or, via the 2-wire I²C-bus.

Packages

- PCF2104XU/12; chip with bumps on Flexible Film Carrier (FFC)
- Pin grid array PGA144 (samples only).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

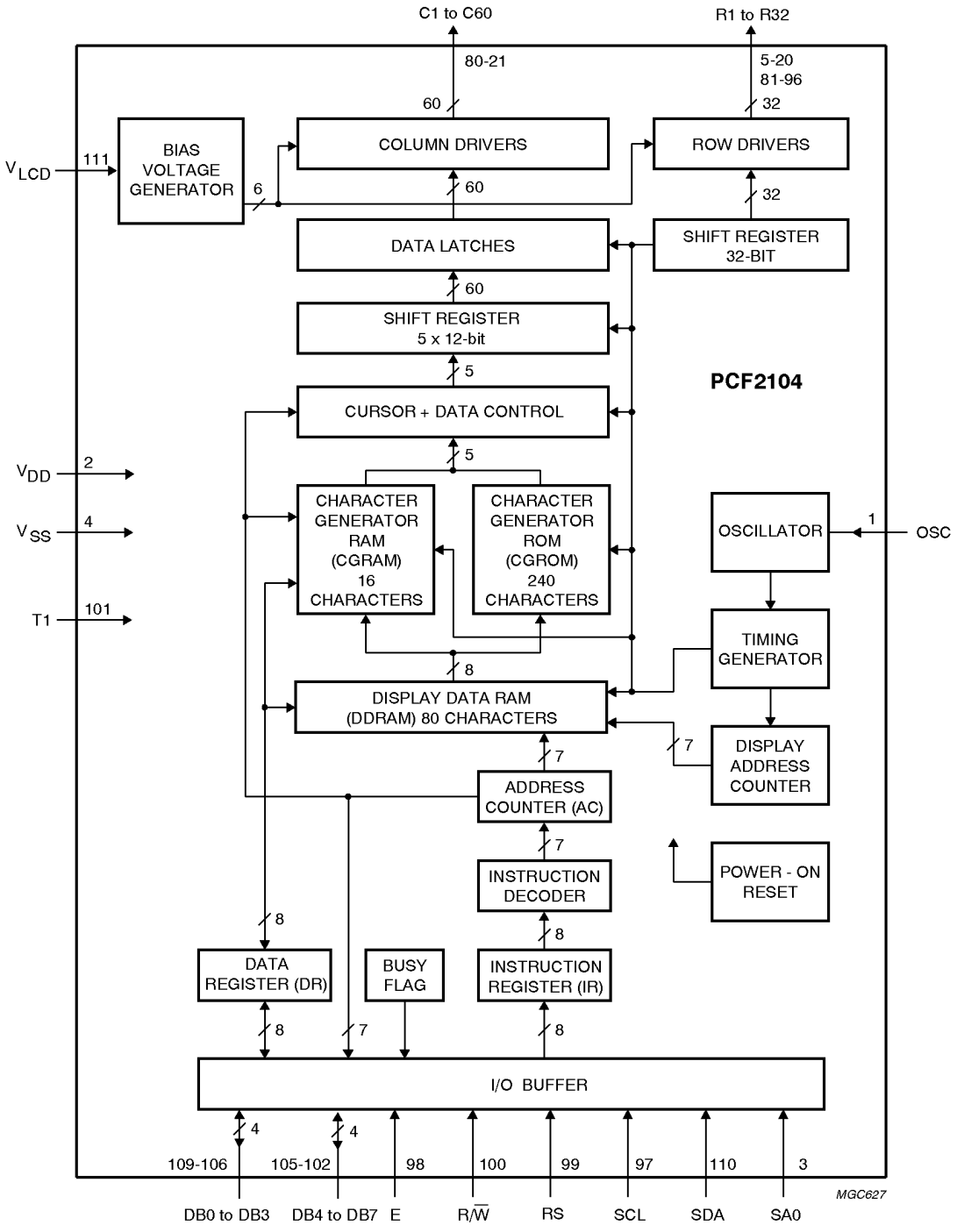

Fig.1 Block diagram.

PINNING

SYMBOL	FFC PAD	DESCRIPTION
OSC	1	oscillator/external clock input
V_{DD}	2	logic supply voltage
SA0	3	I^2C-bus address pin input
V_{SS}	4	ground
R8 to R5	5 to 8	LCD row driver outputs
R32 to R29	9 to12	LCD row driver outputs
R24 to R17	13 to 20	LCD row driver outputs
C60 to C1	21 to 80	LCD column driver outputs
R9 to R16	81 to 88	LCD row driver outputs
R25 to R28	89 to 92	LCD row driver outputs
R1 to R4	93 to 96	LCD row driver outputs
SCL	97	I^2C-bus serial clock input
E	98	data bus clock input
RS	99	register select input
R/$\overline{W}$	100	read/write input
T1	101	test pad input
DB7 to DB0	102 to 109	bidirectional data bus input/output
SDA	110	I^2C-bus serial data input/output
V_{LCD}	111	LCD supply voltage input