Low voltage GSM front-end transceiver SA1620

DESCRIPTION

The SA1620 is a combined receive (Rx) and transmit (Tx) front-end for GSM cellular telephones. The receive path contains two low noise amplifiers (LNA1 and LNA2) with four switchable attenuation steps. A Gilbert Cell mixer in the receive path down-converts the RF signal to a first IF of 70MHz to 500MHz. A second Gilbert Cell in the transmit path transposes a GMSK or phase modulated IF to RF by image reject mixing. A buffered LO signal is fed to Rx and Tx mixers. Rx or Tx path or the entire circuit may be powered-down.

FEATURES

- Excellent noise figure: <2dB for the LNAs at 950MHz
- LNAs matched to 50Ω with external matching components
- LNAs with gain control, 59dB dynamic range in four discrete steps
- LNA gain stability ±0.5dB within -40 to 85°C
- Feedthrough attenuation LNA1 to Rx mixer ≥ 35dB
- Tx power adjustable from -3 to +12dBm by external resistor
- Direct supply: 2.7V to 5.5V
- Battery supply voltage V_{BATT} = 3.3V to 7.5V or direct supply
- Two DC regulators programmable for 3.0V, 3.4V, 3.7V or 5.1V
- Low current consumption: 25mA for Rx or 65mA for Tx
- Fully compatible with SA1638 GSM IF Digital I/Q circuit

APPLICATIONS

- 900MHz front end for GSM hand-held units
- Portable radio, TDMA systems

PIN CONFIGURATION

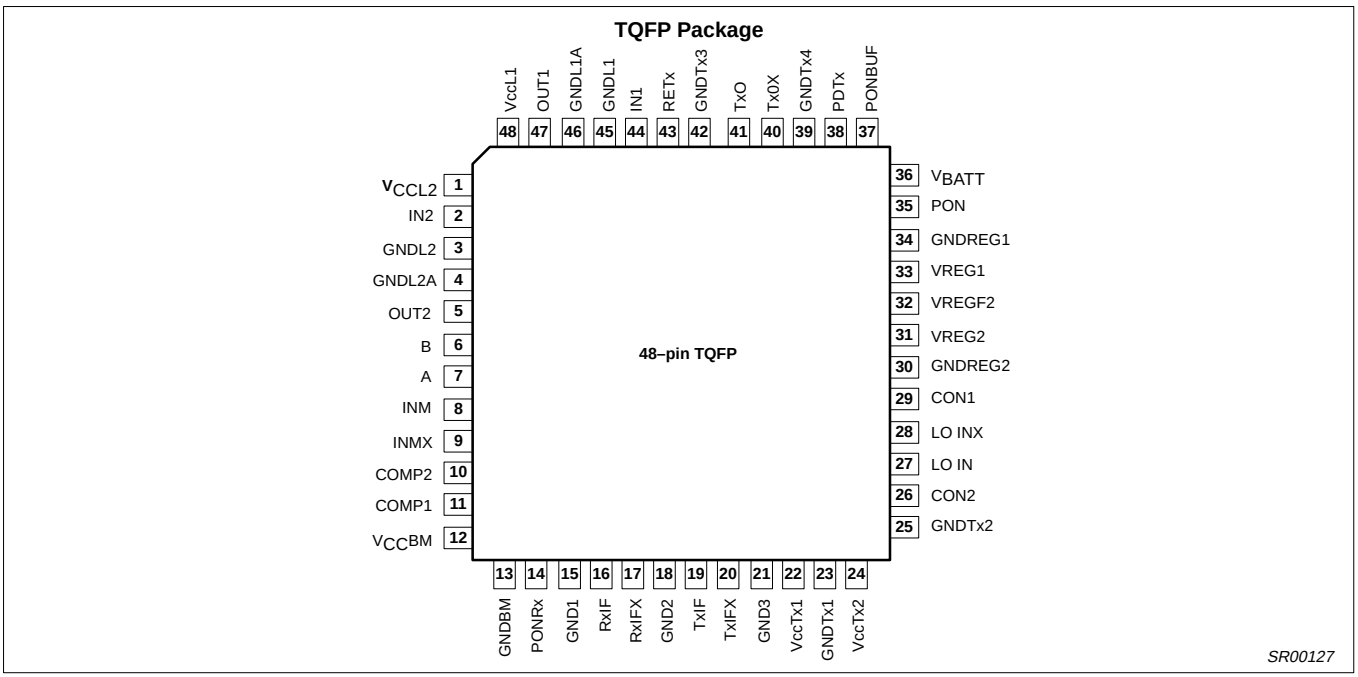

Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1620BE	SOT313-2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	2.7 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM

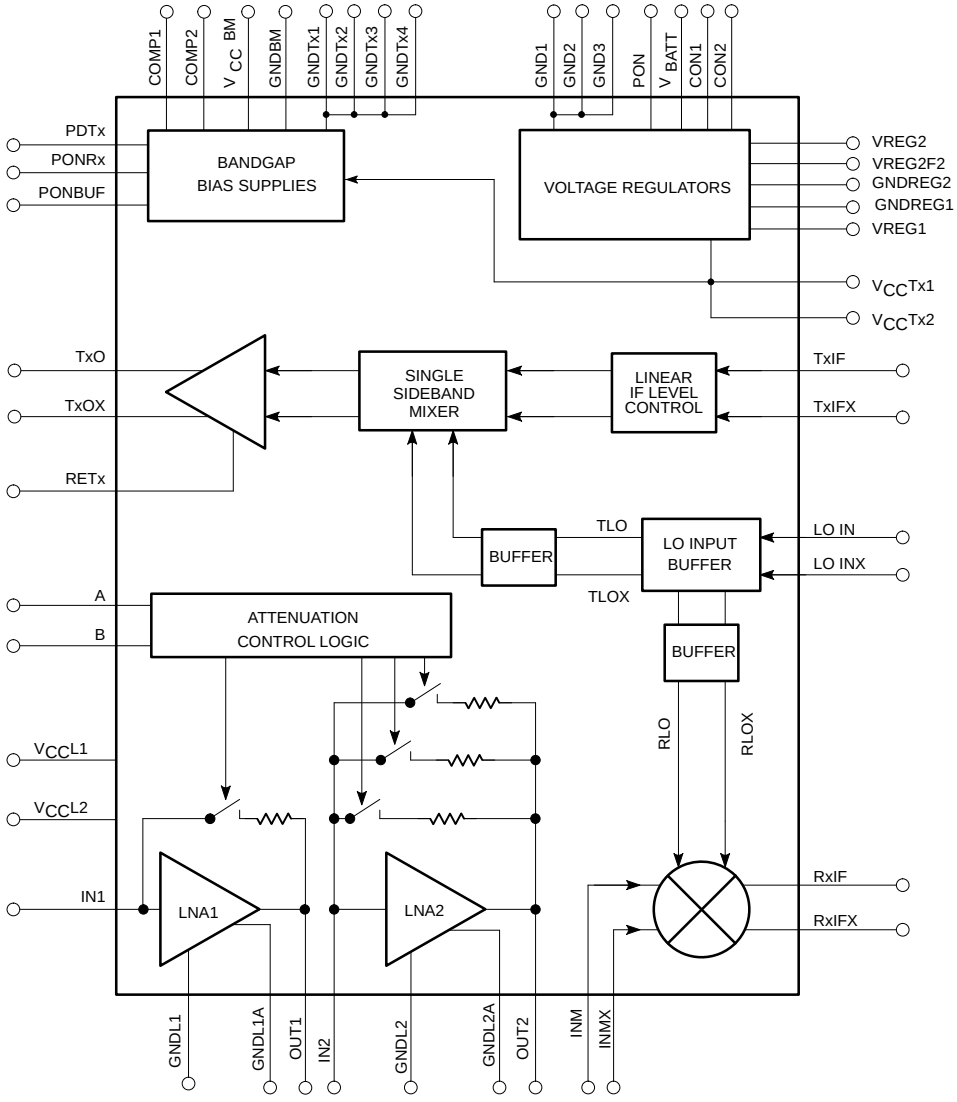

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Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
DC Regulators		
15	GND1	Ground of regulator supply
18	GND2	Ground of regulator supply
21	GND3	Ground of regulator supply
26	CON2	Control 2, voltage select for regulator 1 and 2
29	CON1	Control 1, voltage select for regulator 1 and 2
30	GNDREG2	Ground of regulator 2
31	VREG2	Output of regulator 2
32	VREG2F2	Feedback of regulator 2
33	VREG1	Output of regulator 1
34	GNDREG1	Ground of regulator 1
35	PON	Power-on input of regulators
36	V_{BATT}	Input of regulator 1 and 2
Rx Path		
1	V_{CC}L2	Positive supply for LNA2
2	IN2	Input LNA2
3	GNDL2	Ground L2 for LNA2
4	GNDL2A	Ground L2A for LNA2
5	OUT2	Output LNA2
6	B	Attenuation select B for LNA1 and LNA2
7	A	Attenuation select A for LNA1 and LNA2
8	INM	RF input for Rx mixer, open emitter
9	INMX	Inverse RF input for Rx mixer, open emitter
10	COMP2	Capacitor for bias stabilization
11	COMP1	Capacitor for bias stabilization
12	V_{CC}BM	V_{CC} for Rx Bias and Rx mixer
13	GNDBM	Ground for Rx Bias and Rx mixer
14	PONRx	Power on input for Rx bias supply
16	RxIF	IF output, open collector
17	RxIFX	Inverse IF output, open collector
44	IN1	Input to LNA1
45	GNDL1	Ground L1 for LNA1
46	GNDL1A	Ground L1A for LNA1
47	OUT1	Output LNA1
48	V_{CC}L1	Positive supply for LNA1
Tx Path		
19	TxIF	IF input for Tx
20	TxIFX	Inverse IF input for Tx
22	V_{CC}Tx1	Positive supply for Tx input
23	GNDTx1	Ground for Tx input
24	V_{CC}Tx2	Positive supply for LO and Tx input
25	GNDTx2	Ground for LO and Tx input
38	PDTx	Power down Tx input
39	GNDTx4	Ground for Tx output
40	TxOX	Inverse Tx output, open collector
41	TxO	Tx output, open collector
42	GNDTx3	Ground 1 for Tx output side
43	RETx	Reference resistor for Tx output current
Elements for Tx and Rx Path		
27	LO IN	Input for Local Oscillator signal
28	LO INX	Inverse input for LO or AC ground
37	PONBUF	Power on first stage LO input buffer and bias

NOTES:
1. Device is ESD sensitive. There are no ESD protection diodes at Pins 16, 17, 40 and 41. Thus, open-collector outputs may have increased DC voltage or higher AC peak voltage.
2. Pins 15, 18 and 21 are connected to each other and to a separate ground in REG1 and REG2.
3. Pins 23, 25, 42 and 39 are connected to each other and to the Tx path, LO buffer and associated bias supplies.
4. Pins 22 and 24 are connected to each other providing a sense input. They are also connected to the Tx path, LO buffer and associated bias supplies.
5. Pins 30 and 34 are not internally connected. They must be connected to external grounds.
6. Pins 48, 1, and 12 are not internally connected and have no ESD protection diodes between them. Power may be saved by connecting V_{CC}L1 and IN1 or V_{CC}L2 and IN2 to ground if LNA1 or LNA2 is not needed.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔV	V_{CC}Tx1,2 pins to V_{CC}BM	-0.3 to +1	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	800	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C
V_{TXO}, V_{TXOX}	Positive RF peak voltage at Tx outputs	6	V
V_{RXIF}, V_{RXIFX}	Positive IF peak voltage at Rx mixer outputs	6	V

NOTES:
1. Maximum junction temperature is determined by the power dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: θ_{JA} = 67°C/W.

DC REGULATORS

Two low drop regulators (REG1 and REG2) are included on the chip and may be used to deliver the supply voltage of the main circuitry (e.g., 3V) out of the battery (at V_{BATT} = 3.3 to 7.5V) as shown in Figure 4 and in Table 1.

REG1 is intended to supply, at least, the internal functions of the SA1620. Both regulators may also be used for external circuitry. For this application, different voltages may be programmed as shown in Table 1.

The transmitter supply pins (V_{CC}Tx1,2) also operate as a sensor connection in the feedback loop of REG1 and must be externally connected to pin VREG1. For REG2, the sensor pin VREGF2 must be connected to VREG2.

All ground pins are internally bonded to the header except for pins GNDL1, GNDREG1 and GNDREG2.

When both regulators are not used, connect pins V_{BATT}, PON, CON1, CON2, VREG1, VREG2 and VREG2F2 to ground.

Table 1. DC Reg Output Voltage Control Pins

CON1	CON2	VREG1	VREG2	UNITS
L	L	3 ±5%	3 ±5%	V
L	H	3.4 ±5%	3.4 ±5%	V
H	L	3.7 ±5%	3.7 ±5%	V
H	H	5.1 ±5%	5.1 ±5%	V

NOTES:
1. Logic levels at CON1 and CON2:
   H – Open circuit. Pin must not be connected externally. Logic high level supplied on chip.
   L – Connected to ground.
2. Currents at CON1 and CON2:
   H – 0µA
   L (PON = H) – 50µA
   L (PON = L) – <1µA

Table 2. DC Regulators

SYMBOL	PARAMETER		RATING	UNITS
V_{BATT}	Common positive input voltage at both regulators		3.3 to 7.5	V
VREG1, VREG2	Output voltages of regulators 1 and 2		See Table 1	V
I_{INT1}	Internal current of REG1 in power-on mode		4 + I_{VREG1}/10	mA
I_{INT2}	Internal current of REG2 in power-on mode		2.5 + I_{VREG2}/10	mA
I_{INT01}, I_{INT02}	Internal current in power-down mode		<15	µA
$I_{VREG1MAX}$[5]	Max output current at VREG1		100	mA
$I_{VREG2MAX}$[5]	Max output current at VREG2		30	mA
C13[4]	Capacitor at pin VREG1		0.1 to 1000	µF
C14[4]	Capacitor at pin VREG2		0.1 to 500	µF
BW[6]	V_{BATT} = 3.3V, I_{REG1} = 0.1mA		0.03	kHz
	V_{BATT} = 3.3V, I_{REG1} = 100mA		60	
	V_{BATT} = 7.5V, I_{REG1} = 100mA		80	
F_{REG}[7]	f	≤100kHz	≤–61	dB
		10MHz	≤–32	
		100MHz	≤–37	
		400MHz	≤–48	

NOTES:
1. Power-on pin of Regulator 1 and 2: PON
2. Input currents at PON: <1µA. There are no pull-up or pull-down resistors.
3. Feedthrough attenuation from the logic input PON to the outputs VREG1 and VREG2: ≥40dB.
4. Recommended load capacitors: In every case C529 = C530 = 1µF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω.
5. At T_j ≥ 150°C a thermal switch reduces the output current.
6. Typical open loop bandwidths of regulator 1 at V_{REG1} = 3V and C529 = 1µF.
7. Feedthrough attenuation (at the indicated frequency f) from the input V_{BATT} to the outputs V_{REG1} and V_{REG2} at V_{BATT} = 3.3V, (CON1=CON2=L): F_{REG} (f) = V_{REG} (f) / V_{BATT} (f).

DC ELECTRICAL CHARACTERISTICS

V_{CCxxx} = +2.7V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmitter						
I_{VCC}	Current at pins V_{CC}Tx1,2, V_{CC}BM, $I_{RX\ IF}$, $I_{RX\ IFX}$	Transmit mode R_{546} = 240Ω	46	59	72	mA
R1	External resistor[1]			240		Ω
V_{R1}	Internal supply at pin RETx	V_{CC}Tx1,2 = 2.7V		0.43		V
		V_{CC}Tx1,2 = 5.5V		0.45		
I_{R1}	Current at pin RETx	R546 = 240Ω, V_{CC}Tx1,2 = 2.7V		1.7		mA
		R546 = 240Ω, V_{CC}Tx1,2 = 5.5V		1.8		
Low noise amplifiers						
I_{VCC}L1	Current at pin V_{CC}L1	G1hi mode	2.5	3.5		mA
I_{VCC}L2	Current at pin V_{CC}L2	G2hi mode	2.5	3.5		mA
Receiver						
I_{VCC}	Current at pins V_{CC}Tx1,2, V_{CC}BM, $I_{RX\ IF}$, $I_{RX\ IFX}$	Receive mode R_{546} = 240Ω	13	18	23	mA
Logic levels[2]						
V_{IH}	Logic 1 level	P_{ON}BUF, PDTx, P_{ON}Rx, A, B	2.0		V_{CCBM}[3]	V
V_{IH}	Logic 1 level	P_{ON}	2.0		V_{BAT}	V
V_{IL}	Logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_{Ia}	Input logic capacitance			1.7		pF

NOTES:

1. The output current I_{TXO} + I_{TXOX} is adjustable by the external resistor R546. I_{TXO} + I_{TXOX} = 10 * I_{R546}, I_{R546} = V_{R1}/R546,
2. Thresholds are independent of supply voltages. Thus the SA1620 is compatible with SA1638 and with the power down inputs of usual external voltage regulators.
3. P_{ON} logic 1 max is V_{BAT}.

AC ELECTRICAL CHARACTERISTICS

V_{CCXX} = +2.7V, T_A = 25°C; RF = 925-960MHz; IF=400MHz, f_{LO}=RF + IF; LO = -18dBm; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[1]					UNITS
			MIN[1]	-3σ	TYP	3σ	MAX[1]	
Low Noise Amplifier LNA1[2]								
S_{21}	Gain	G1hi mode	7	9.4	10	10.6	13	dB
		G1hi mode, RF = 1800MHz			-2.5			
		G1lo mode	-15	-13	-12	-11	-9	
	IP3	G1lo mode			28			
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G1hi mode			0.003			dB/°C
		G1lo mode			0.0140			
$\Delta S_{21}/\Delta V_{CCL1}$	Gain/voltage sensitivity				0.1			dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation				0.01			dB/MHz
S_{12}	Reverse isolation	G1hi mode			-19			dB
S_{11}	Input match[3]	50Ω			-11			dB
S_{22}	Output match[3]	50Ω			-14			dB
P_{-1dB}	Input 1dB gain compression	G1hi mode		-15.5	-14	-12.5		dBm
IIP3	Input third order intercept			-5.5	-4	-2.5		dBm
IIP3/Δt	Input third order intercept				.011			dB/°C
NF	Noise figure				1.7			dB
t_{ON}	Turn-on time				7			µs
t_{OFF}	Turn-off time				0.5			µs
Low Noise Amplifier LNA2[2]								
S_{21}	Gain	G2hi mode	7	9	10	11	13	dB
		G2hi mode, RF = 1800MHz			-1.5			dB
		G2lo1 mode	-10.5	-8.5	-7.5	-6.5	-4.5	dB
		G2lo2 mode	-24.5	-22.5	-21.5	-20.5	-18.5	
		G2lo3 mode	-31.5	-30	-28.5	-27	-25.5	
	IP3	G2lo1 mode			18			
		G2lo2 mode			20			
		G2lo3 mode			25			
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G2hi mode			0.003			dB/°C
		G2lo1,2,3 modes			0.014			
$\Delta S_{21}/\Delta V_{CCL2}$	Gain/voltage sensitivity				0.1			dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation				0.01			dB/MHz
S_{12}	Reverse isolation	G2hi mode			-24			dB
S_{11}	Input match[3]	50Ω			-13			dB
S_{22}	Output match[3]	50Ω			-15			dB
P_{-1dB}	Input 1dB gain compression	G2hi mode		-18	-16	-14		dBm
IIP3	Input third order intercept			-8	-6	-4		dBm
IIP3/Δt	Input third order intercept				.019			dB/°C
NF	Noise figure				2.0			dB
t_{ON}	Turn-on time				-6			µs
t_{OFF}	Turn-off time				0.5			µs

AC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[1]					UNITS
			MIN[1]	-3σ	TYP	3σ	MAX[1]	
Rx Mixer								
PG_C	Power conversion gain[5]		5	7.5	+8.5	9.5	12	dB
		RF = 1800MHz			-4			
$PG_C/\Delta T$	Gain temperature sensitivity							dB/°C
$PG_C/\Delta f$	Gain frequency variation							dB/MHz
S_{11}	Mixer input match at ports INM and INMX[4]				-13			dB
NF_M	SSB combined noise figure				10			dB
P_{-1dB}	Input 1dB compression				-7.3			dBm
IIP3	Input third order intercept			-2	0	2		dBm
IIP3/Δt	Input third order intercept				.005			dB/°C
IIP2	Input second order intercept				19			dBm
G_{RFM-IF}	RF feedthrough	400MHz			-26			dB
$G_{LOfloor}$	LO floor feedthrough	400MHz			-30			dB
G_{LO-IF}	LO feedthrough to IF	1.3GHz			-16			dB
G_{LO-RFM}	LO to mixer input feedthrough	1.3GHz			-53			dBm
G_{LO-RF1}	LO to RF LNA1 input feedthrough	1.3GHz			-85			dBm
G_{LNA1-2}	LNA1 output to LNA2 input feedthrough	400MHz 1290-1760MHz			-41 -26			dB
G_{LNA2-M}	LNA2 output to mixer input feedthrough	1290-1760MHz			-23			dB
G_{LNA1-M}	LNA1 output to mixer input feedthrough	400MHz 1290-1760MHz			-50 -35			dB
LO input								
Z_{IN}	Input impedance (each single-ended input)	1.3GHz			35-j97			Ω
P_{IN}	Input power				-18			dBm
A_{SAT}	Transistor saturation limit, max input amplitude				500			mV
Tx IF input								
$\|Z_{IN}\|$	Input impedance	400MHz			2			kΩ
P_{IN}	Input power				-25			dBm
Tx RF output								
P_{OUT}	R546 = 240Ω, V_{CC}Tx1,2 = 2.7V		5	7.5	8.5	9.5		dBm
	R546 = 240Ω, V_{CC}Tx1,2 = 5.5V			8.2	9.2	10.2		dBm

NOTES:
1. Due to our automatic test equipment accuracy and repeatability test limits may not reflect the ultimate device performance. Standard deviations are calculated from characterization data.
2. If the LNA1 is not needed, connect pin V_{CC}L1 and IN1 to GND. If the LNA2 is not needed, connect pin V_{CC}L2 and IN2 to GND.
3. Simple L/C elements are needed to achieve specified return loss.
4. The mixer RF inputs (emitters of a Gilbert Cell) may be driven by a symmetrical matching network.
5. Input symmetry suppression is such that the product 6*RF–4*LO is to be suppressed by at least 66dB relative to the wanted IF output when the input to the mixer is at –32dBm.

Table 3. Power-Down and Tx/Rx Control Logic

No.	PONBUF	PDTX	PONRX	MODE	RESULT
1	H	H	L	Standby	LO buffer active, Tx and Rx path inactive
2	H	L	L	Transmit	LO buffer active, Tx path active, Rx path inactive (LNAs + mixer)
3	H	H	H	Receive	Tx path inactive, LO buffer and Rx path active (LNAs + mixer)
4	H	L	H	Calibrate	Tx path and Rx LNAs inactive, LO buffer and Rx mixer active
5	L	x	x	Power-Down	Tx- and Rx-path, LO buffers and Bias inactive

NOTES:
1. Logic levels of PONBUF, PDTx and PONRx: TTL, see DC Electrical Characteristics.
2. Logic levels / polarities are compatible with Philips Semiconductors Power Amp Controller PCA5075 and synthesizers UMA1019 or SA8025.
3. First stage of LO buffer and parts of bias supply are powered on by PONBUF.
4. Tx- or Rx-paths may be activated for special timeslots. Lines 1 and 4 show options to support DC offset calibrations at baseband mixers, following in the receiver chain (SA1638).

Table 4. Gain Control Logic for LNA1 and LNA2

INPUT		ATTENUATION STEP	GAIN		POWER CONSUMPTION	
a	b		LNA1	LNA2	LNA1	LNA2
H	H	0	G1hi	G2hi	on	on
H	L	1	G1hi	G2lo1	on	off
L	H	2	G1hi	G2lo2	on	off
L	L	3	G1lo	G2lo3	off	off

NOTES:
1. Logic levels of a and b: TTL
2. For values of G1hi and G1lo, G2hi, G2lo1, G2lo2 and G2lo3 see LNA1 and LNA2 AC Electrical Characteristics.

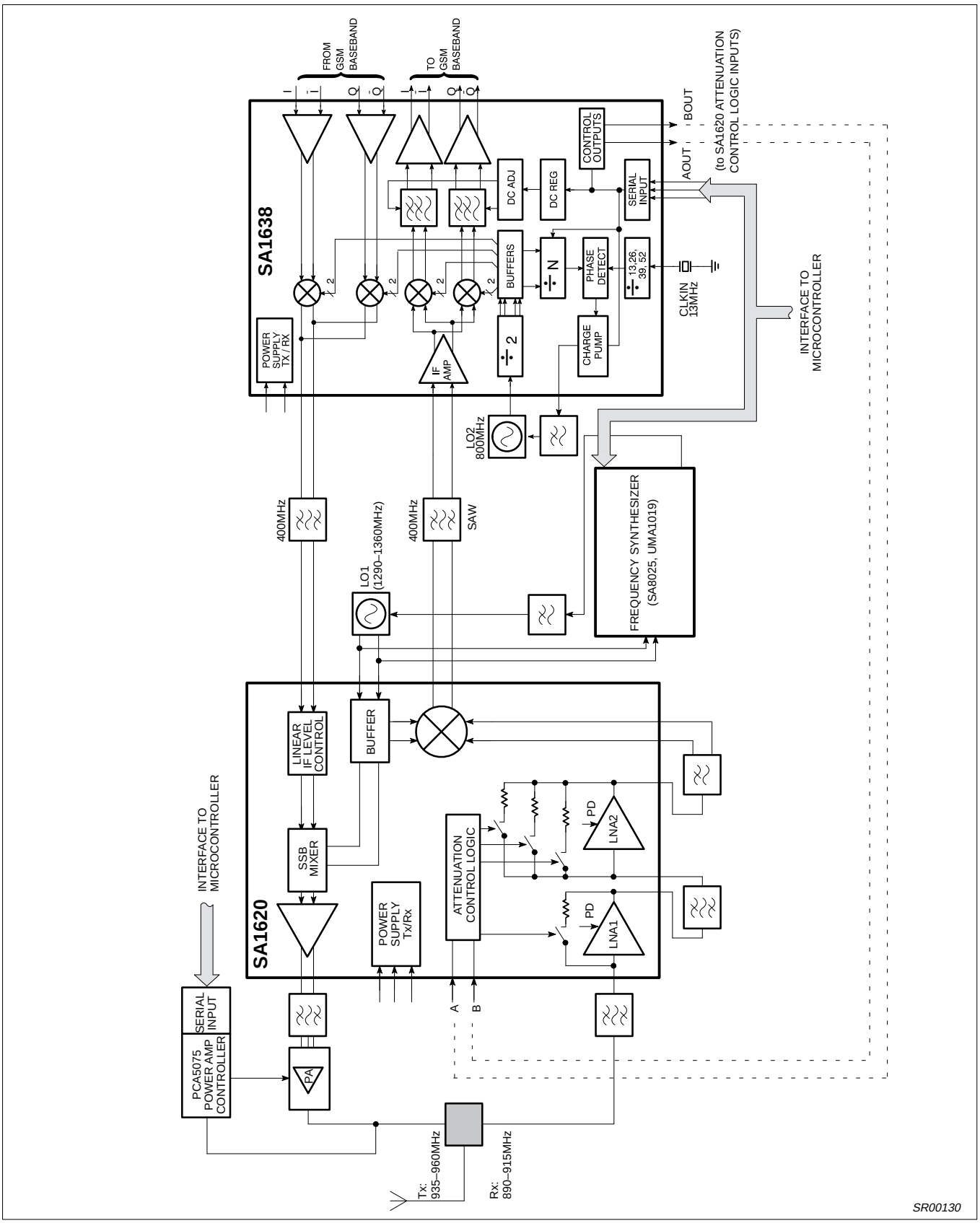

FROM GSM BASEBAND
TO GSM BASEBAND
I
Ī
Q
Q̄
SA1638
POWER SUPPLY TX / RX
IF AMP
÷ 2
BUFFERS
÷ N
PHASE DETECT
÷ 13, 26, 39, 52
CHARGE PUMP
DC ADJ
DC REG
CONTROL OUTPUTS
SERIAL INPUT
BOUT
AOUT
(to SA1620 ATTENUATION CONTROL LOGIC INPUTS)
CLKIN 13MHz
INTERFACE TO MICROCONTROLLER
LO2 800MHz
400MHz
SAW
LO1 (1290–1360MHz)
FREQUENCY SYNTHESIZER (SA8025, UMA1019)
SA1620
LINEAR IF LEVEL CONTROL
BUFFER
SSB MIXER
POWER SUPPLY Tx/Rx
ATTENUATION CONTROL LOGIC
PD
LNA2
LNA1
A
B
INTERFACE TO MICROCONTROLLER
SERIAL INPUT
PCA5075 POWER AMP CONTROLLER
PA
Tx: 935–960MHz
Rx: 890–915MHz
SR00130

Figure 3.

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–500MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. The placing of the AGC gains switches at the front means that for most of the time some attenuation will be inserted, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +8.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption the output power can be reduced, if not required, by appropriate choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filters to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

Receive Path

Multiple LNAs allow the flexibility to exploit the best choice of currently available filters (on performance, size, or cost grounds). This approach is preferable to a single high-gain stage as the stray cross-coupling effects between pins remain manageable. In a single stage amplifier this would limit the amount of rejection of out-of-band signals that could be achieved, and would also limit the amount of AGC attenuation that could be practically implemented.

The LNAs are powered up only when PONBUF, PDTx and PONRx are high, to allow a high degree of battery economy. If greater sensitivity is required for an application, an external preamplifier circuit can be used instead of LNA1, and LNA1 left unconnected.

A special mode is provided with just the IF output related circuitry active in order to allow calibration of the DC offset at the SA1638 baseband receive outputs. This offset contains a contribution due to coupling effects between the second local oscillator and the IF circuitry, and therefore the receiver is set up in the receive state (but with incoming signals excluded) to allow accurate offset calibration.

Gain Control

Gain control is implemented in the SA1620 RF front-end. This avoids the disruption of the DC offset at the baseband IQ outputs that is typically caused by changes in the AGC. The SA1620 and SA1638 are designed so that the GSM dynamic range requirements can be met with the AGC remaining on the maximum gain setting.

These gain steps scale the dynamic range of the received signal (e.g., 90dB for GSM) into the dynamic range of the baseband processing device.

The absolute gain tolerances may be measured together with the attenuation tolerances of external filters during production of the receiver equipment. After software calibration switching from one dynamic range to another will cause only minor errors.

Tx Path

TXIF and TXIFX are differential IF inputs for phase modulated signals (e.g., GMSK). There is an IF level control loop which provides a constant amplitude to an image reject up mixer. Thus, this mixer operates linearly in the IF path, independent of IF level tolerances.

The single sideband up mixer is sufficient in quadrature to achieve the typical performance indicated in Table 6 over an IF range of 250 to 500MHz. The mixer is operating in switching mode by well matched 0° and 90° LO signals, optimized for 1.1 to 1.5GHz.

The Tx output stage operates in switching mode. Thus, parasitic AM at the IF is not transferred. The outputs TXO and TXOX may be used symmetrically or single-ended. Some spurious emissions will be very low when a symmetrical output signal is used.

$$P_{OUT} = R_e \left[6.25V \cdot (Z_{Pin\ 40} + Z_{Pin\ 41}) \cdot (I_{R546})^2\right]$$

according to Figure 4 and $I_{R546} = \frac{V_{R546}}{R_{546}}$ according to DC Electrical Characteristics. P_{OUT} is adjustable with R546 and is accurate to within ±1dB over the full voltage range 2.7 to 5.5V, and ±0.5dB from a given supply voltage. The absolute limit of the negative peak voltage swing at pins TxO and TxOX is $V_{SAT} = V_{CC}Tx1,2 – 1V$. The absolute limit of the positive peak voltage is +6V.

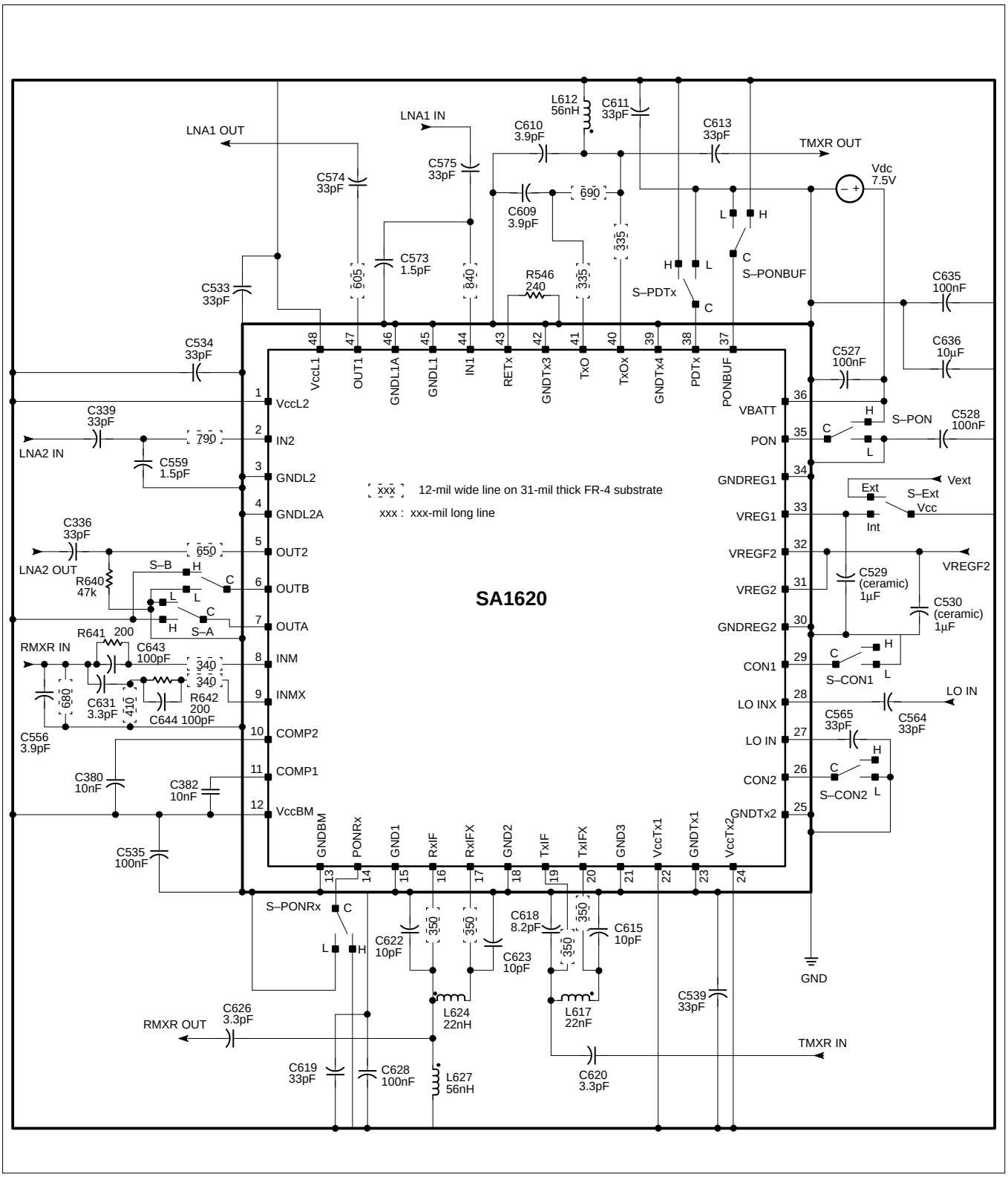


Figure 4. Application Circuit

APPLICATION CIRCUIT

LNA

Impedance Match: Intrinsic return losses at the input and output ports are 7dB and 11dB, respectively. However, since long and narrow traces are always needed to fan out the pins, the user can adjust the traces' dimensions so that only one shunt capacitor at the input is required to achieve excellent impedance match for both ports. If the user wants to skip the input matching network for simplicity, then roughly 0.7dB gain would be lost, although it benefits the system IP3.

Noise Match: The LNA1 and LNA2 can achieve 1.7dB and 2.0dB noise figure, respectively, when S11 = –11dB. Further improvement in S_{11} will slightly decrease NF and increase S_{21}.

Gain Control: The LNA1 can be switched to the attenuation mode, while LNA2 has three attenuation modes to choose from. When gain and loss modes from two LNAs are combined, there will be a total dynamic range of 59dB in the RF block; 3.0V operation is preferred to achieve better IP3 for both LNA1 and LNA2. A shunt resistor of 47kΩ is connected between the LNA2 OUT (pin5) and ground to ensure 5 uS switching time providing the coupling capacitor is limited to 33 pF.

Temperature Compensation: Both LNAs have a built–in temperature compensation scheme to reduce the gain drift rate to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 2.7V to 5.5V.

Mixer

Mixer Input Match: The mixer is configured for best gain, noise figure and spurious response. The user must supply an external, patented resonant balun to provide the differential drive as well as the impedance match (embedded in). Because the mixer consists of two single–balance mixers, whose inputs are connected in parallel instead of in series, the differential and common–mode impedances are equal.

Output Match: The mixer output circuit also features an external resonant balun to optimize the conversion gain and noise figure. The principal IF operating frequency is 400 MHz.

LO Drive: The internal buffer only requires –18dBm from an external source. Furthermore, the transmitter incorporates an integrated SSB upconverter that consists of narrowband phase shifters at 1300MHz (LO side) and 400MHz (IF side), so the LO frequency is recommended to be the receiver band plus 400MHz. Additionally, the LO leakage at the input of LNA1 is extremely low, which can greatly alleviate the LO re–radiation problem.

Outband Blocking: For optimum performance, passive R/C network is added at each input of the mixer. The resistors degenerate the noise conversion gain, while the capacitors preserve the gain and noise figure at RF frequencies.

Noise Figure and IP3: The resonant balun is superior to the conventional balun in terms of insertion loss, size and cost. As a result, the user can expect excellent SSB noise figure and gain which is 10dB and 8.5dB, respectively, at 400MHz IF. And the associated input IP3 is 0dBm typically. In the meantime, due to the internal LO buffer, the noise figure and IP3 are not sensitive to the LO levels. As discussed in the LNA Impedance Match session, a better system IP3 can be achieved (if necessary) through LNAs' gain reduction.

Transmitter

The resonant balun is applied again to maximize the gain and output power, for a given bias current. Typical output power is 8.5dBm when the input level exceeds –25dBm.

LO Input

The LO input is used in Tx- and in Rx-mode.

Only one synthesizer PLL is necessary to supply the LO input with different frequencies in Tx and Rx timeslots.

The LO input buffer should only be set in power-down mode together with the PLL. As further buffering is included on chip there will be no influence on the PLL in active mode when the SA1620 Rx- or Tx-path is power On or Off. Current consumption can thus be saved by powering on the Rx- and Tx-circuitry just before it is required, without disruption of the LO circuitry. LO input pins LO IN and LO INX may be used single-ended or symmetrically.

Table 5. GSM/DSC1800 Frequency Specification

(GSM 05.05, Version 4.2.0, April 1992) Mobile Stations Frequency Bands

	GSM	EGSM	DCS1800	Unit
Tx	890 to 915	880.2 to 915	1710 to 1785	MHz
Rx	935 to 960	925.2 to 960	1805 to 1880	MHz

Table 6. Measured Tx Output Frequency and Tx Mixer Products

IF=400MHz, symmetrical load at pins TxO, TxOX.

No.	SPECTRAL LINE f=n*IF+m*LO MHz					RELATIVE POWER OF SPECTRAL LINE			REMARKS
	LO = 1280MHz	LO = 1300MHz	LO = 1315MHz	Order					
				n	m	min dBc	typ dBc	max dBc	
1	80	100	115	–3	1		–70		
2	160	200	230	–6	2		–76		
3	320	300	285	4	–1		–60		
4	400	400	400	1	0		–46		IF
5	480	500	515	–2	1		–31		
6	560	600	630	–5	2		–62		
7	720	700	685	5	–1		–56		
8	800	800	800	2	0		–37		2)
9	880	900	915	–1	1		0		1)
10	960	1000	1030	–4	2		–46		3)
11	1020	1100	1185	6	–1		–63		
12	1200	1200	1200	3	0		–60		
13	1280	1300	1315	0	1		–32		LO
14	1360	1400	1430	–3	2		–46		
15	1440	1500	1545	–6	3		–64		
16	1600	1600	1600	4	0		–75		
17	1680	1700	1715	1	1		–50		4) 5)
18	1760	1800	1830	–2	2		–34		3)
19	1840	1900	1945	–5	3		–68		3)
20	2000	2000	2000	5	0		–77		
21	2080	2100	2115	2	1		–74		
22	2160	2200	2230	–1	2		–67		
23	2240	2300	2345	–4	3		–59		
24	2400	2400	2400	6	0		–75		
25	2480	2500	2515	3	1		–76		
26	2560	2600	2630	0	2		–70		2LO

NOTE:
1. Desired Tx output frequency LO–IF corresponding to EGSM Tx band in Table 5.
2. (LO+IF)–(LO–IF) = 2 * IF
3. See Rx bands in Table 5
4. LO+IF = mixer image frequency
5. See Tx bands in Table 5

Table 7. Measured Tx Output Noise Floor

Frequency MHz		dBc/Hz			REMARKS
		MIN	TYP	MAX	
< 860			–135		
860 to 880			–134		
880.2 to 890			–133		EGSM TX extension
890 to 915			–133		GSM TX
915 to 925			–133		
925.2 to 935			–134		EGSM RX extension
935 to 960			–135		GSM RX
960 to 1000			–135		
1000 to 1710			–135		
1710 to 1785			–146		DCS1800 TX
1785 to 1805			–145		
1805 to 1880			–144		DCS1800 RX
1880 to 12750			–147		
>12750			tbd		
Adjacent Channel			–130		

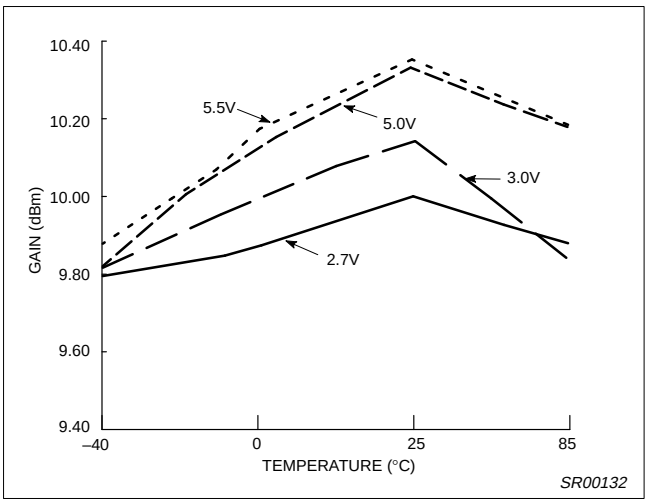


Figure 5. Receive LNA1 Gain

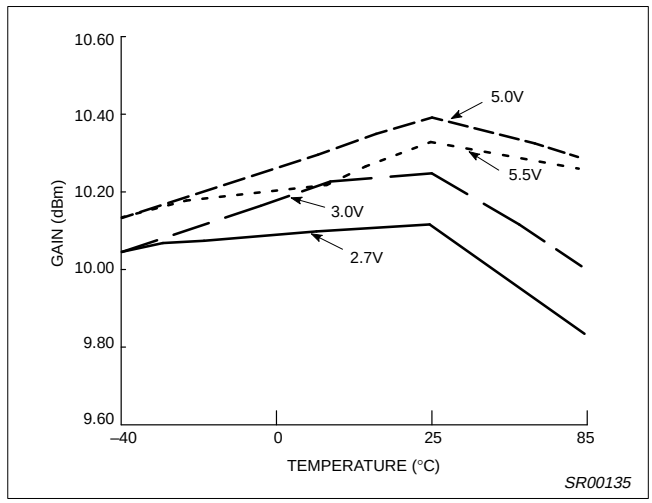


Figure 8. Receive LNA2 Gain

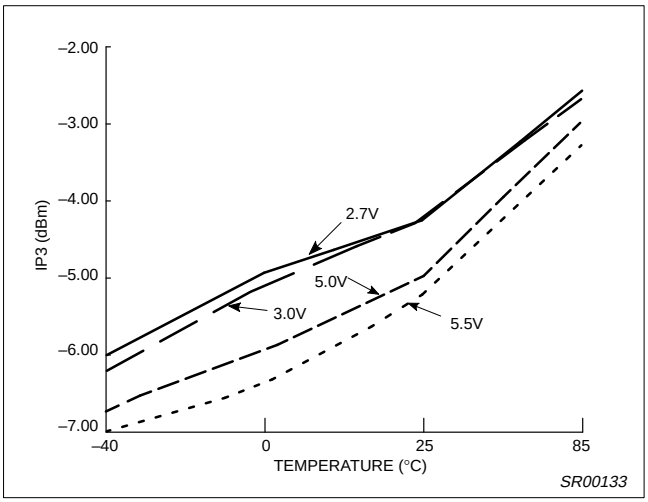


Figure 6. Receive LNA1 IIP3

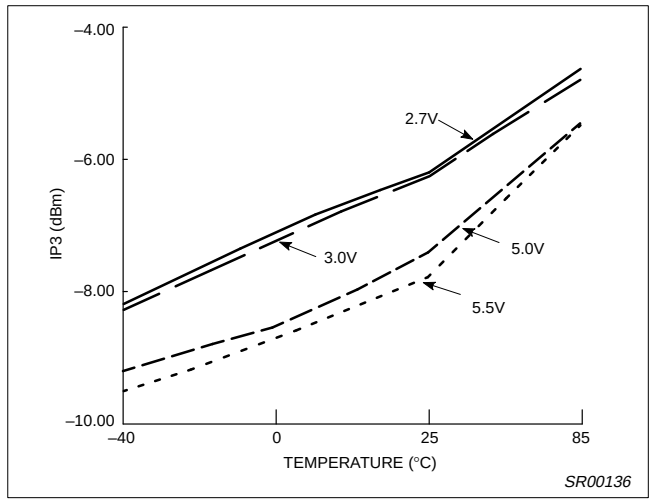


Figure 9. Receive LNA2 IIP3

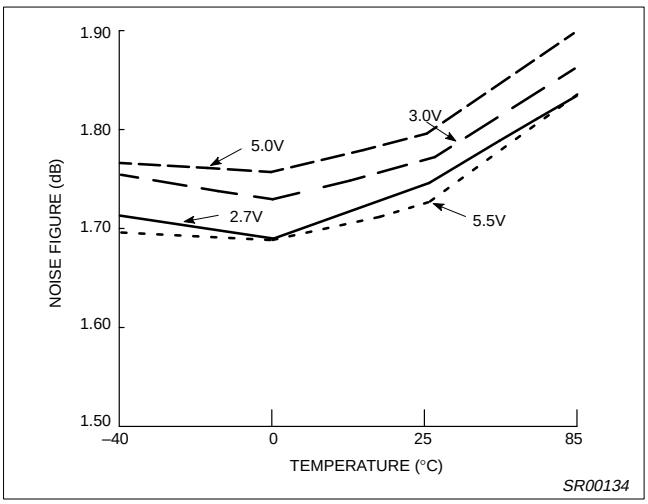


Figure 7. Receive LNA1 Noise Figure

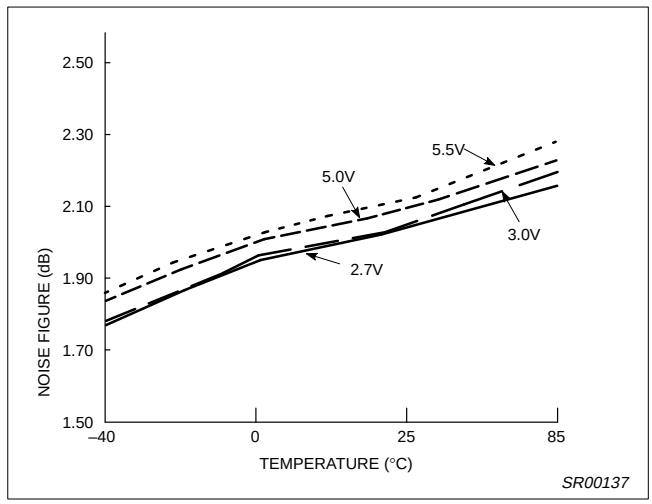


Figure 10. Receive LNA2 Noise Figure

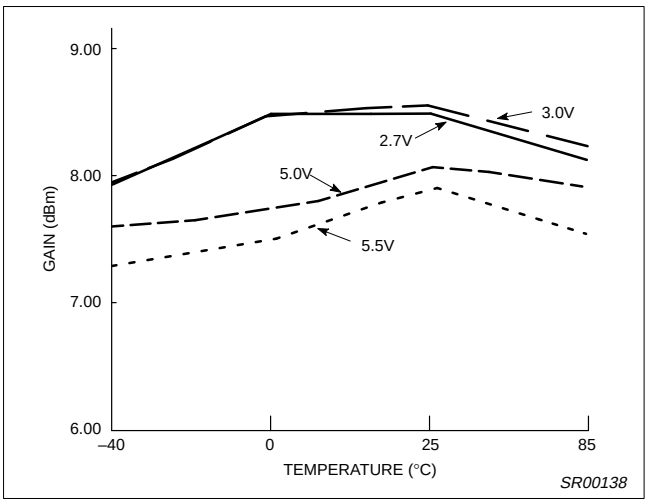


Figure 11. Receive Mixer Gain

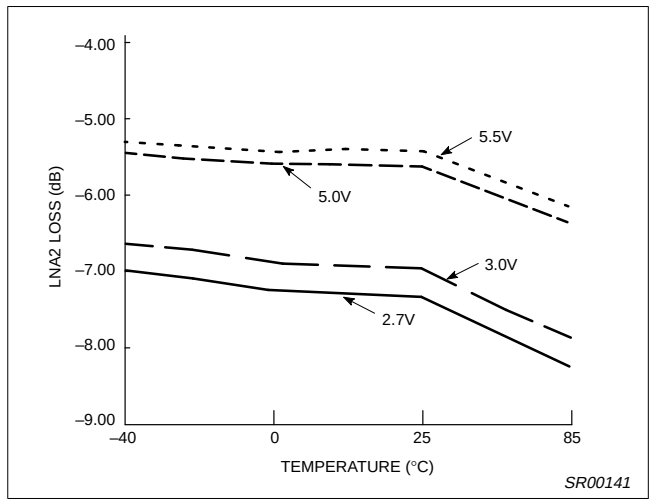


Figure 14. Receive LNA2 Loss Mode 1

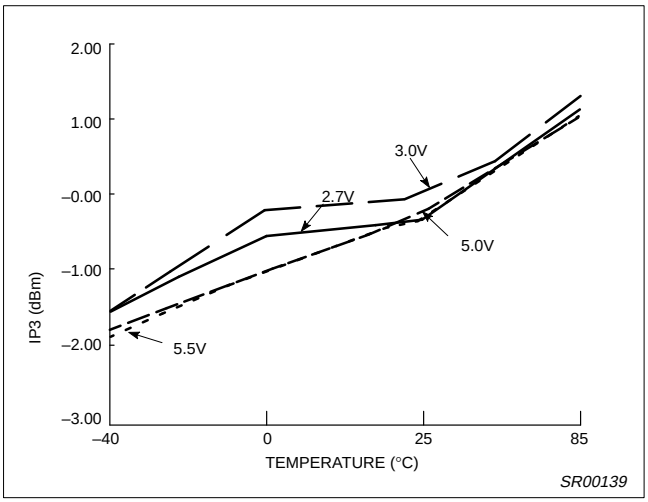


Figure 12. Receive Mixer IIP3

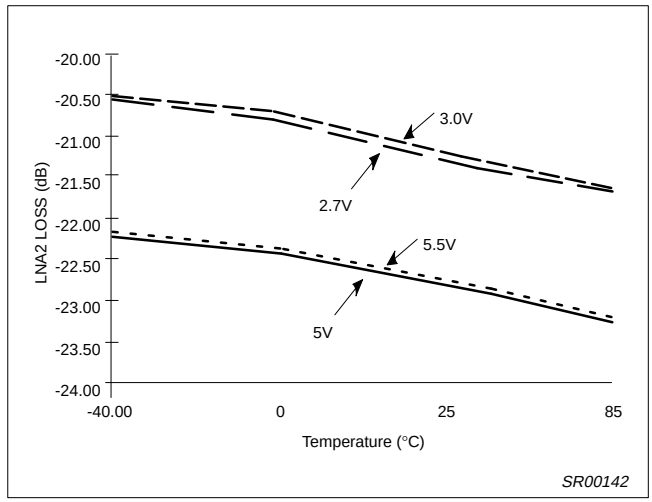


Figure 15. Receive LNA2 Loss Mode 2

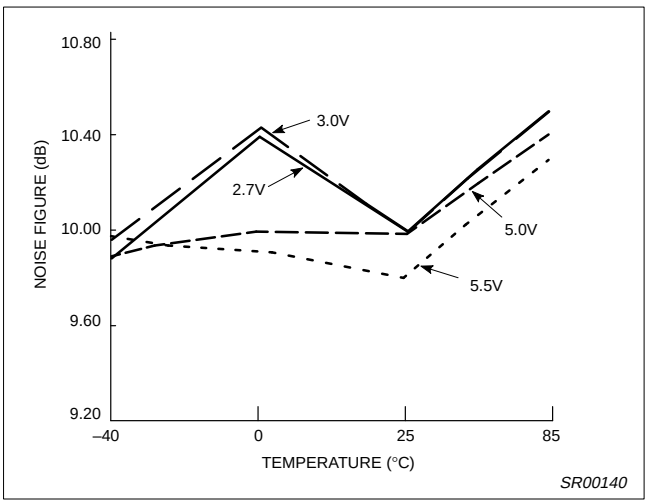


Figure 13. Receive Mixer Noise Figure

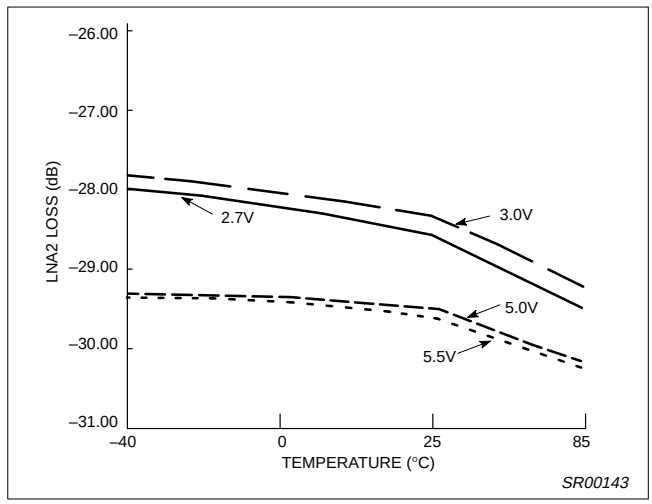


Figure 16. Receive LNA2 Loss Mode 3

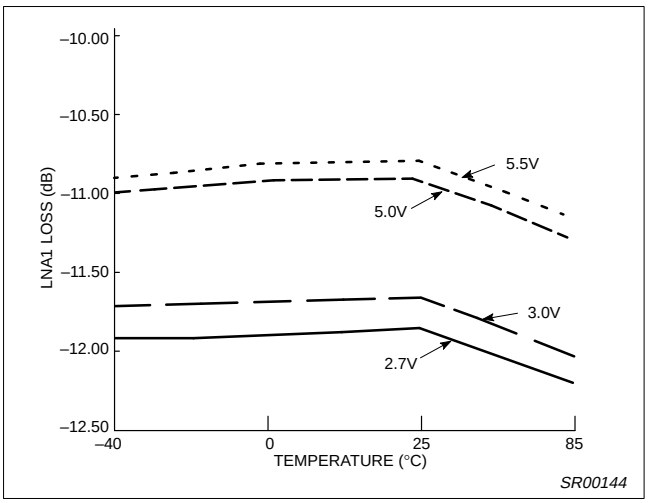


Figure 17. Receive LNA1 Loss

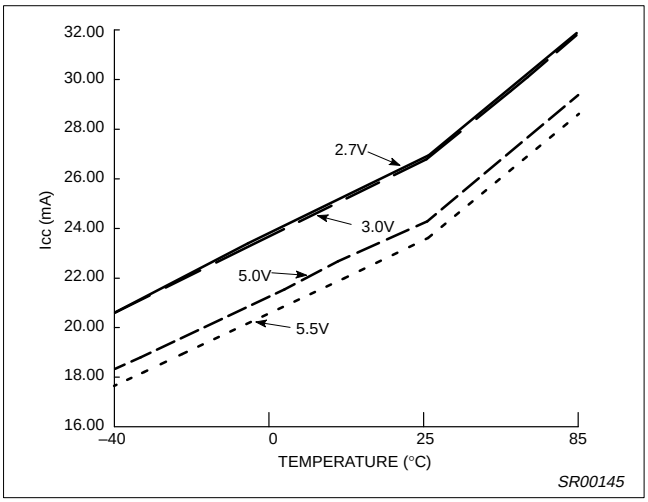


Figure 18. Receive Mode Current

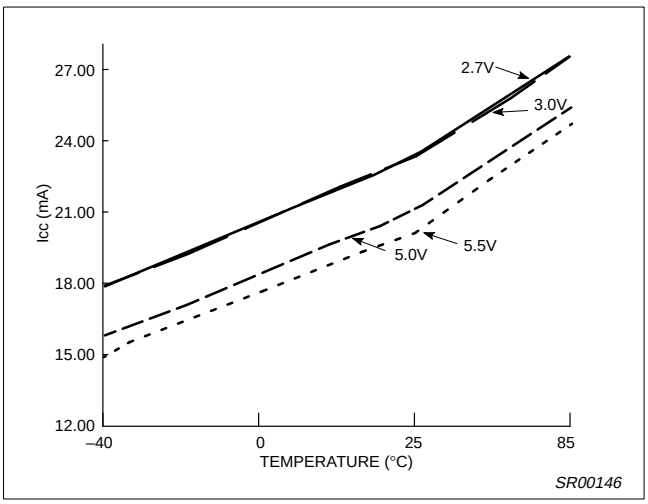


Figure 19. Receive Mode (LNA2 OFF) Current

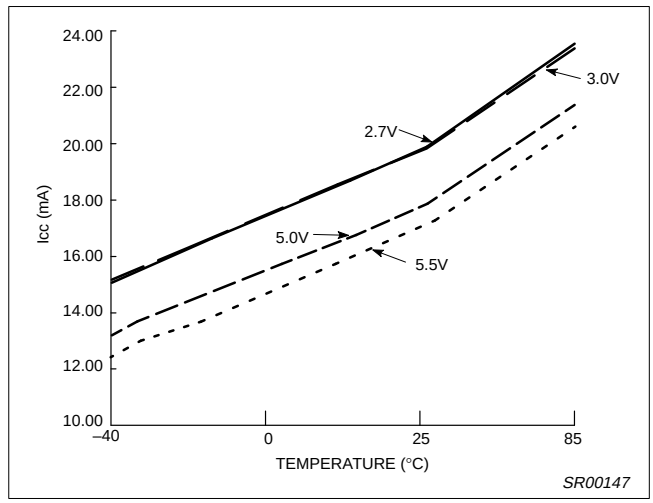


Figure 20. Calibrate Mode Current

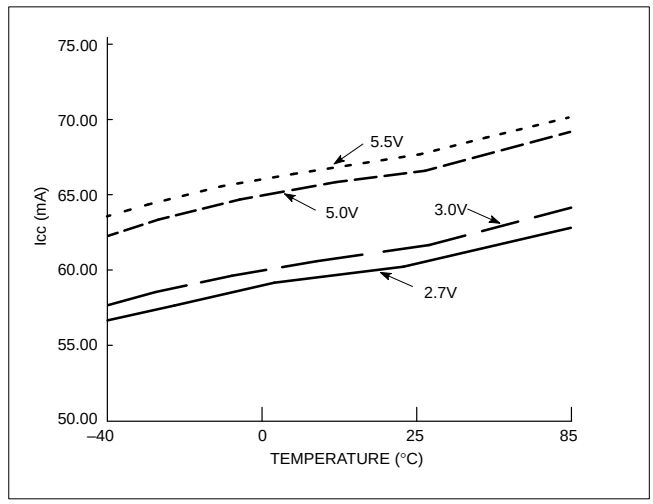


Figure 21. Transmit Mode Current

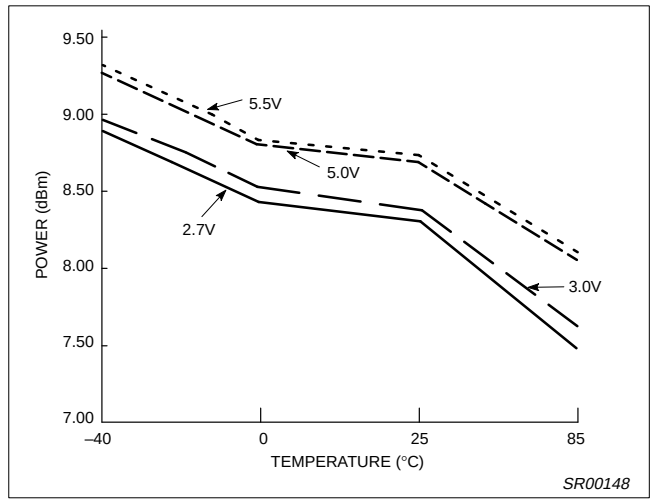


Figure 22. Transmit Power @ -20dBm

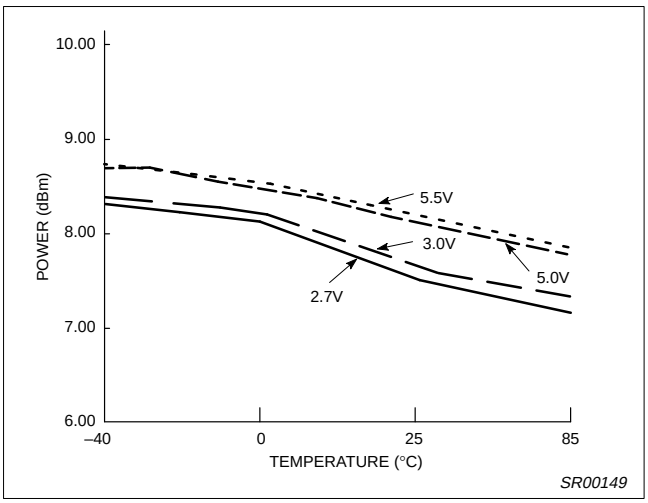


Figure 23. Transmit Power @ -25dBm

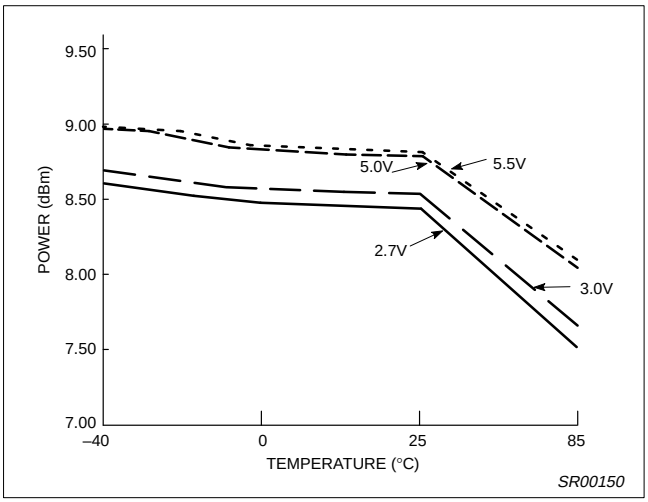


Figure 24. Transmit Power @ -15dBm

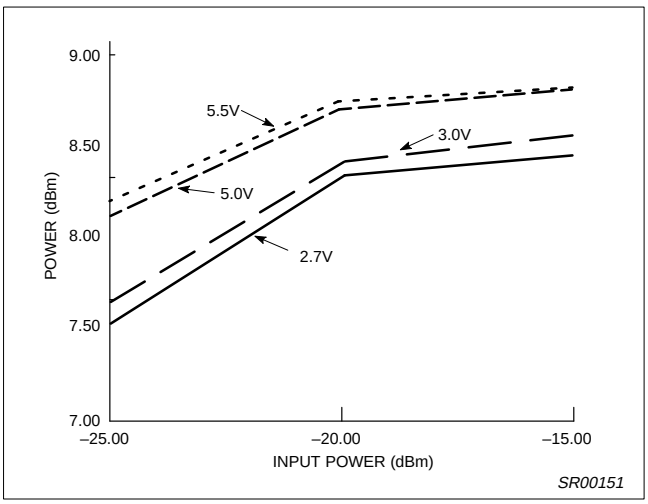


Figure 25. Transmit Power @ 25°C

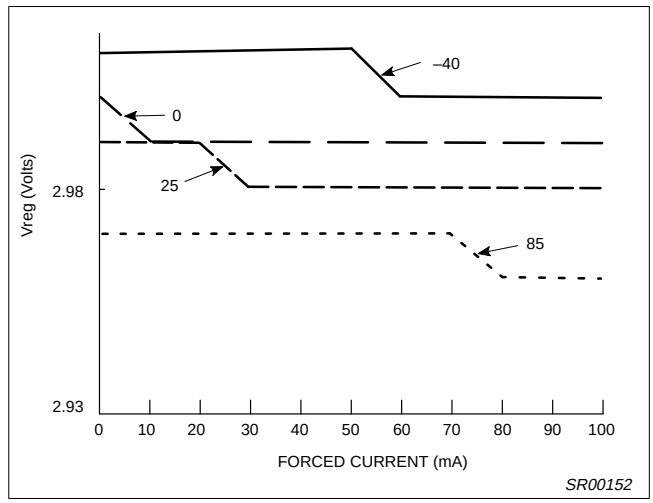


Figure 26. Regulator 1 Load Regulation (V_{BAT} = 3.5V)

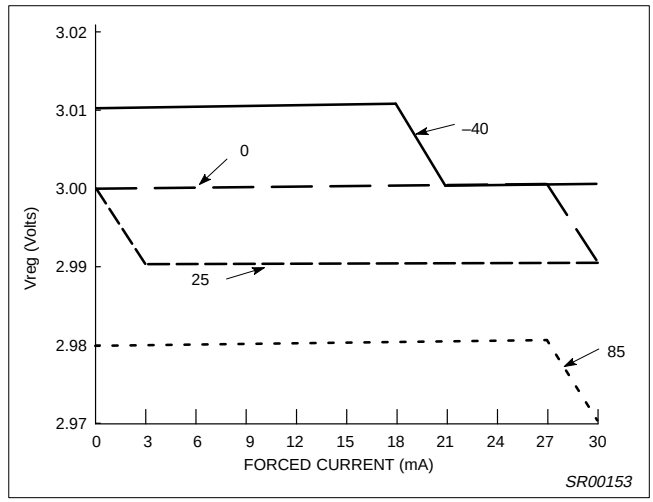


Figure 27. Regulator 2 Load Regulation (V_{BAT} = 3.5V)

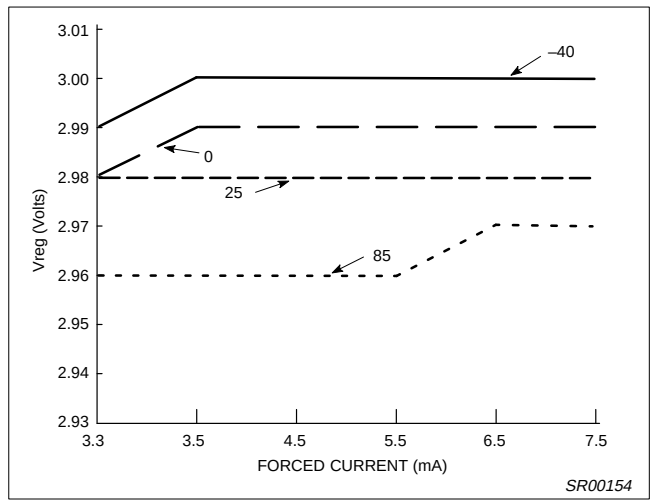


Figure 28. Regulator 1 Line Regulation @ 100mA Load

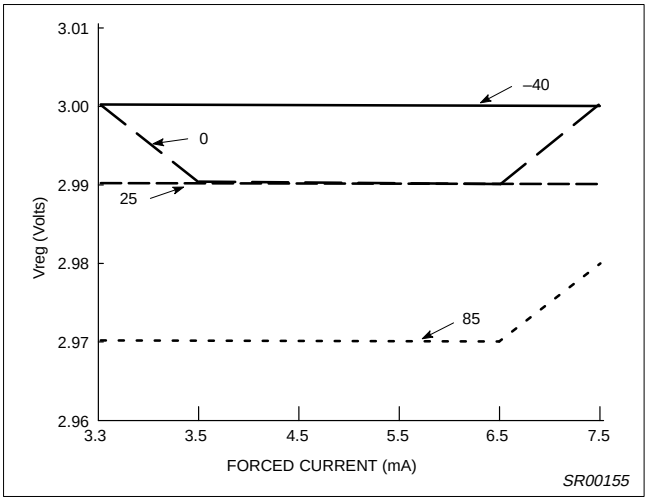


Figure 29. Regulator 2 Line Regulation @ 30mA Load

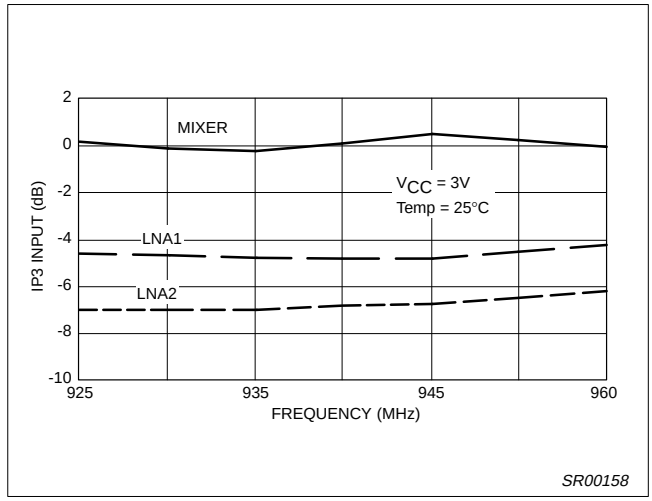


Figure 32. Input IP3 vs Frequency

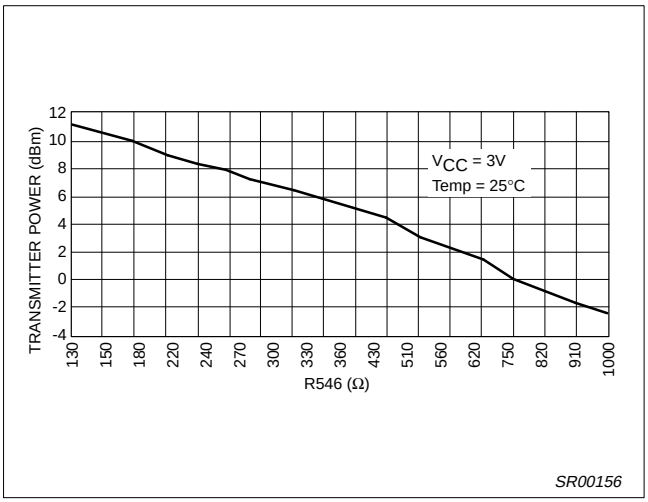


Figure 30. Transmit Output Power vs R(546) @ V_{CC} = 3V

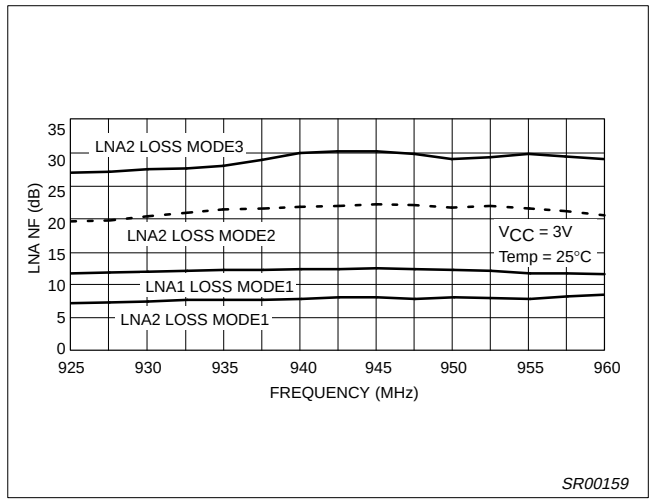


Figure 33. LNA NF vs Frequency

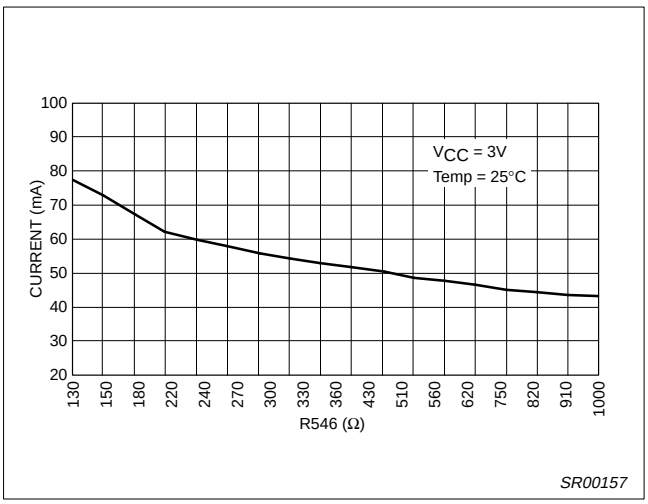


Figure 31. Transmit Mode Current vs R(546) @ V_{CC} = 3V

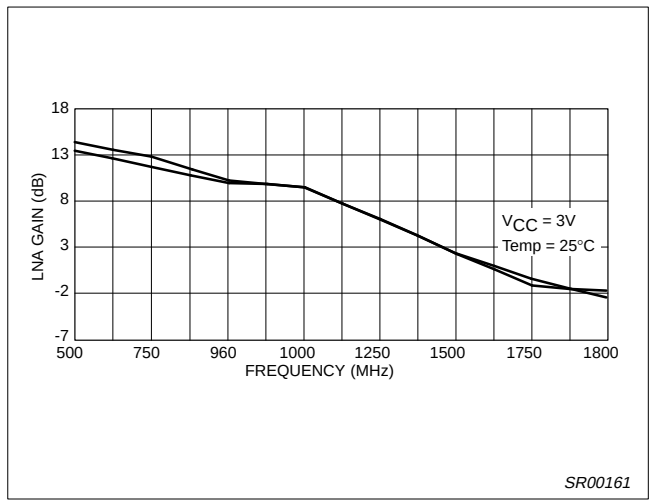
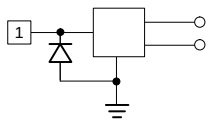
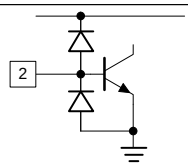
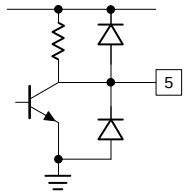
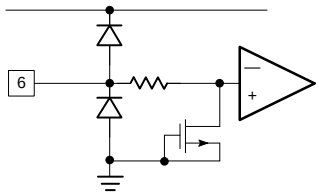
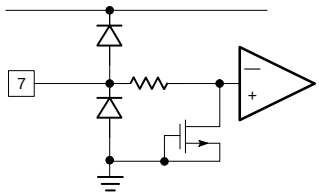
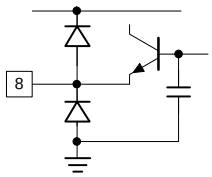
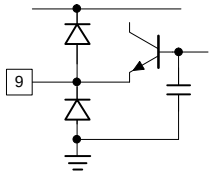
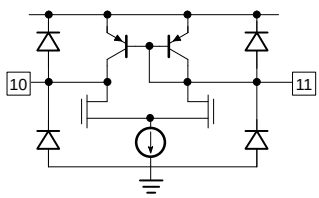


Figure 34. LNA Gain vs Frequency

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	V_{CC}	3.0	
2	IN2	0.8	
3	GNDL2	0.0	
4	GNDL2a	0.0	
5	OUT2	2.2	
6	B CMOS INPUT		
7	A CMOS INPUT		
8	INM	0.4	
9	INMX	0.4	
10	COMP2	2.2	
11	COMP1	2.2	

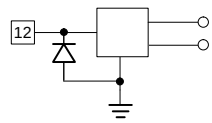
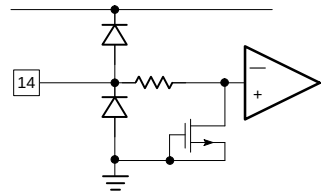
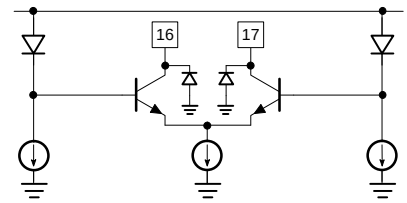
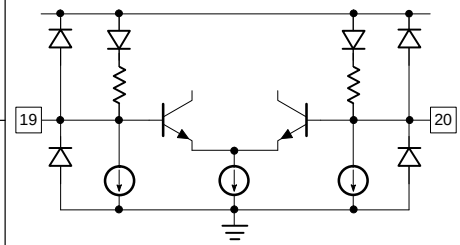
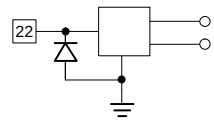
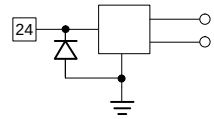
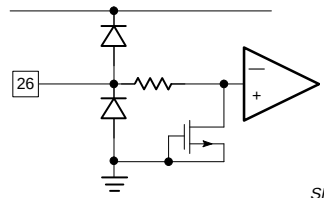
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
12	V_{CC}BM	3.0	
13	GND	0.0	
14	POnRx CMOS INPUT		
15	GND	0.0	
16	Rxif	3.0	
17	RxifX	3.0	
18	GND	0.0	
19	Txif	2.2	
20	TxifX	2.2	
21	GND	0.0	
22	V_{CC}Tx	3.0	
23	GND	0.0	
24	V_{CC}Tx	3.0	
25	GND	0.0	
26	CON2 CMOS INPUT		

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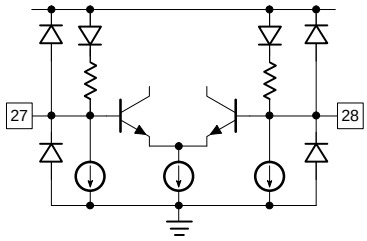
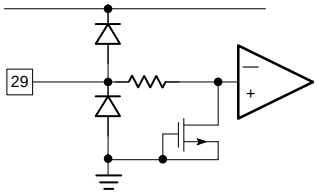
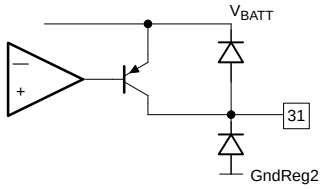
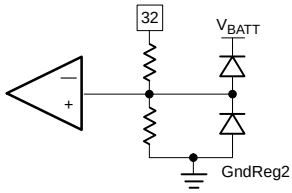
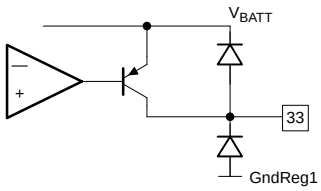
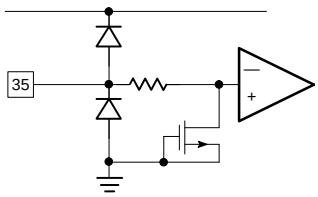
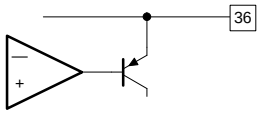
Figure 35. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
27	LOin	2.2	
28	LOinX	2.2	
29	CON1 CMOS INPUT		
30	GndReg1	0.0	
31	VReg2	3.0	
32	VRegF2	3.0	
33	VReg1	3.0	
34	GndReg1	0.0	
35	POn CMOS INPUT		
36	V_{BATT}	3.0	

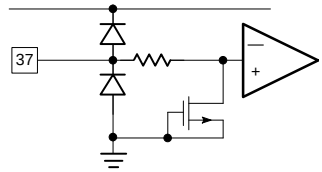
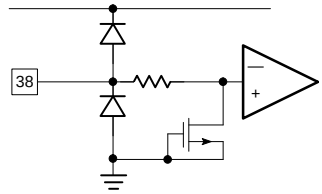
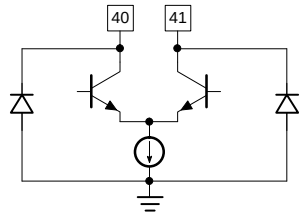
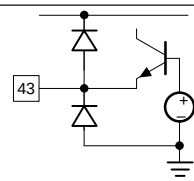
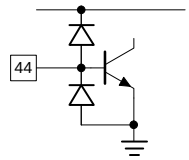
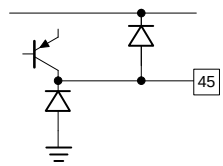
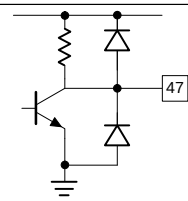
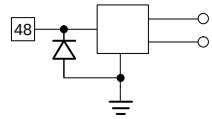
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
37	POnBuf CMOS INPUT		
38	PDTx CMOS INPUT		
39	GndTx	0.0	
40	TxOx	3.0	
41	TxO	3.0	
42	GndTx	0.0	
43	RETx	0.4	
44	IN1	0.8	
45	GndL1	0.0	
46	GndTx	0.0	
47	OUT1	2.2	
48	$V_{CC}L1$	3.0	

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Figure 36. Pin Functions (cont.)