IF quadrature transceiver SA1630

DESCRIPTION

The SA1630 is a 70–400 MHz I/Q transceiver for wireless LAN using direct controlled IF amplifier, a pair of quadrature down conversion mixers and a pair of baseband amplifiers. The transmit path contains a pair of quadrature up conversion mixers that transposes a quadrature baseband input signal up to IF frequency. An external VCO signal is divided internally and provides quadrature local oscillator signals for the mixers. Another divider chain, reference divider and phase detector are provided to avoid the need for an external synthesizer. To keep power consumption to a minimum the transmit, receive and local oscillator functions can be powered down under digital control.

FEATURES

- Low supply voltage operation of 2.7V for main chip and 2.9V for charge pump.
- Low current consumption: 33.5 mA in RX, 26.5 mA in TX, typical at 3V.
- Flexible power up/down options.
- Optional 2.5V regulated reference voltage available during transmit.
- Input/output IF frequency from 70–400 MHz.
- Internal IF PLL for synthesizing the local IF oscillator signal.
- Bandwidth of baseband Tx inputs is 20 MHz and that of baseband Rx outputs is 10 MHz.
- Designed for IEEE 802.11 wireless LAN using Direct Sequence Spread Spectrum modulation.
- Control registers power up in a default state.
- Optional quadrature phase trim capability.
- Only standard reference input frequency required, choice of 8, 11, 22 or 44 MHz.
- Digital IF gain control of 74 dB in steps of 2 dB.
- Package: LQFP–48

APPLICATIONS

- IF circuitry for IEEE 802.11 DSSS wireless LAN.
- Applications for high speed wireless data.

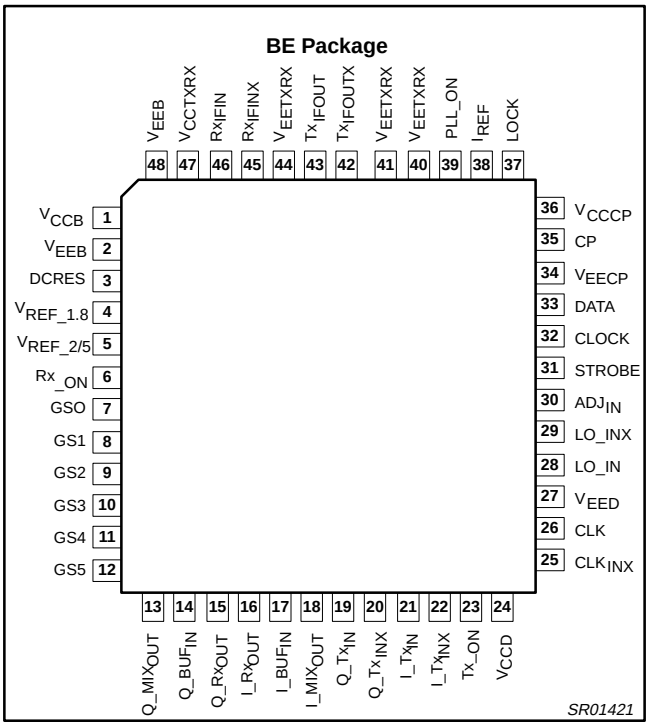

Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48–Pin Plastic Low Profile Quad Flat package	–40 to +85°C	SA1630BE	SOT313–2

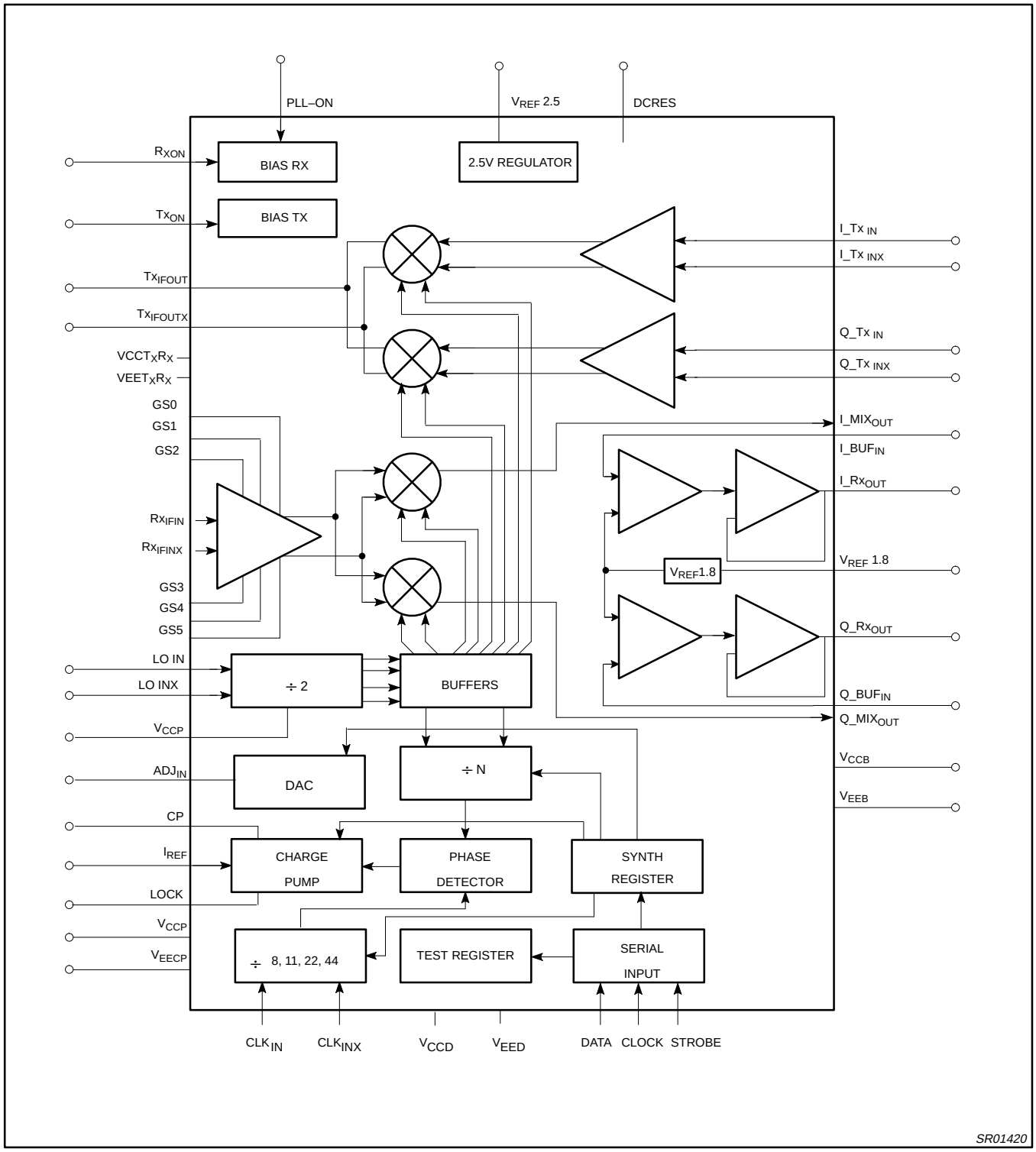

Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VCCB	Supply Pin for Baseband and Bias circuits of R_x, bypassed suitably externally
2, 48	VEEB	Ground pIns for Baseband and Bias Circuits of R_x. Needs low inductance separate path to system ground.
3	DCRES	Not used currently.
4	Vref_1.8	Reference Voltage Output (used for test only, do not connect)
5	Vref_2.5	Reference Voltage output in Tx mode for external use.
6	RX_ON	Rx enable CMOS signal input.
7	GS0	Control bit 0 for IF VGA Gain control, CMOS input
8	GS1	Control bit 1 for IF VGA Gain control, CMOS input
9	GS2	Control bit 2 for IF VGA Gain control, CMOS input
10	GS3	Control bit 3 for IF VGA Gain control, CMOS input
11	GS4	Control bit 4 for IF VGA Gain control, CMOS input
12	GS5	Control bit 5 for IF VGA Gain control, CMOS input
13	Q_MIXOUT	RX Q Mixer current output for external filtering
14	Q_BUFIN	Rx Q Buffer current input after external filtering
15	Q_RXOUT	Quadrature baseband voltage output, single–ended
16	I_RXOUT	In–phase baseband voltage output, single–ended
17	I_BUFIN	Rx I Buffer current input after external filtering
18	I_MIXOUT	Rx I Mixer current output for external filtering
19	Q_TXIN	Quadrature differential Tx baseband input
20	Q_TXINX	Quadrature differential Tx baseband input
21	I_TX IN	In–phase differential Tx baseband input
22	I_TX INX	In–phase differential Tx baseband input
23	TX_ON	Tx Enable CMOS input.
24	$V_{CC}D$	Digital circuit supply, bypassed suitably, externally.
25	CLKINX	Differential reference input for synthesizer
26	CLKIN	Differential reference input for synthesizer
27	VEED	Digital Ground, needs separate low inductance connection to system ground.
28	LO_IN	Differential LO input
29	LO_INX	Differential LO input
30	ADJIN	Used for test only. Do not connect
31	STROBE	Serial bus strobe input
32	CLOCK	Serial bus clock input
33	DATA	Serial bus data input
34	VEECP	Charge pump ground, needs separate low inductance connection to system ground.
35	CP	Charge pump output, connected to PLL loop filter.
36	VCCCP	
37	LOCK	Test control output and synthesizer lock indicator
38	IREF	Reference current for charge pump
39	PLL_ON	Power–on input (CMOS) for synthesizer circuits (active high). When LOW the entire chip goes into SLEEP mode.
40, 41, 44	VEETXRX	Ground pins for Tx and Rx. Needs separate low inductance connection to system ground.
42	TXIFOUTX	Differential transmitter IF output (open collector)
43	TXIFOUT	Differential transmitter IF output (open collector)
45	RXIFINX	Differential receiver IF input
46	RXIFIN	Differential receiver IF input
47	VCCTXRX	Supply for Tx and Rx. Bypass suitably externally

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{CCXX}	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXXXX}	Supply voltages:	2.7 to 3.6	V
V_{CC}CP	Charge pump supply voltage	2.9 to 3.6	V
T_A	Operating ambient temperature range	-40 to +85	°C

POWER CONTROL

NO:	PLL_ON	RX_ON	TX_ON	STATE DESCRIPTION	MODE
1	0			SLEEP mode	SLEEP
2	1	0	0	Synthesizer ON, Rx STDBY, Tx OFF	WAIT
3	1	0	1	Synthesizer ON, Rx STDBY, Tx ON	TRANSMIT
4	1	1	0	Synthesizer ON, Rx ON, Tx OFF	RECEIVE
5	1	1	1	Synthesizer ON, Rx OFF, Tx ON	TRANSMIT

1. Sleep mode (PLL OFF, Rx OFF, Tx OFF)

In this mode everything is switched off except the 3–wire digital bus. As long as the digital supply is still on, the programmed values are active and the 3–wire bus will continue to be programmable.

2. Wait Mode (Tx Off, Rx Standby)

PLL is on. Receiver is in the reduced current standby mode and the transmitter is completely switched off. This mode maybe useful if the PLL is to be kept on and is waiting for a quick turn–on to either transmit or receive modes.

3. Transmit mode (Rx standby)

The PLL and transmitter are on. The receive section is in a reduced current mode wherein most of the Rx circuitry is powered down except for the bias and baseband circuits needed to hold the baseband output voltages in the active state. This mode is useful if the Rx baseband outputs are AC coupled via a large capacitor and the application demands quick turn–on for the Rx.

4. Receive Mode (Tx Off)

The Transmitter is completely shut–off. The PLL and receiver sections are operating.

5. Transmit Mode (Rx OFF)

PLL and Transmit sections are on. However, the Receiver is completely shut–down. This mode is useful if the Rx baseband outputs are DC coupled to the external world.

DC ELECTRICAL CHARACTERISTICS

V_{CC}XXX +3V; V_{EE}XXX = 0V; TA=25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
I_{CC}	Supply Current, Receive mode			33.5	tbd	mA
I_{CC}	Supply Current, Wait mode	Wait mode (2)		17	tbd	mA
I_{CC}	Supply Current, Transmit mode	PLL_ON=TX_ON=Hi RX_ON=L0		26.5	tbd	mA
I_{CC}	Supply Current	PLL_ON=Lo RX_ON=dc TX_ON=dc		.068	tbd	mA
CMOS LOGIC INPUTS (DATA, CLOCK, STROBE)						
V_{IH}	Input logic 1 level		2.0		V_{CCD}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_I	Input logic capacitance				4	pF
CMOS Logic output (LOCK)						
V_{OH}	Output logic 1 level		V_{CC}–0.4			V
V_{OL}	Output logic 0 level				0.4	V
Regulator PON logic input						
V_{IH}	Input logic 1 level		2.0			V
V_{IL}	Input logic 0 level				0.8	V
I_I	Input logic current				1	µA

AC ELECTRICAL CHARACTERISTICS IF TRANSMIT MODULATOR

V_{CC}XXX=RX_ON=PLL_ON= +3V; V_{EE}XXX = GND1=GND2=GND3= 0V; LO in=100 mV peak at 704 MHz, CLKin=100mV peak, 22 MHz, Ta=25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
BW[4]	Input modulation bandwidth	500 ohms source impedance	22			MHz
V_{IN}	Input signal amplitude, Differential[1]	Vcm range		1		Vpp
THD	Total harmonic distortion[1]	Input signal amplitude[1= 1 Vpp, 11 MHz]		–50		dBc
R_{INTx}	Input resistance	Between pins ITxIn and ITxInX		98		kΩ
C_{INTx}	Input Capacitance	Between pins ITxIn and ITxinX			2	pF
	Mean output voltage	ITxIn=ITxinX= QTxin=QTxinX= V_{cc}/2	V_{CC}–0.3			V
	Mean output current	Per collector		2		mA
	Output current DC offset				20	µA
	Output Current[2]			0.475		mA rms
	Output differential voltaage[1.2]	400 Ω tuned load[2]		190		mV rms
$f_{LO–IF}$	LO feedthrough[1.3]	Differential output		–43	–30	dBc
	SSB Suppression [1.3]	f_{OUT}=352 MHz	35	50		dBc
	Spot Noise[4] (Output Spectrum)	offset F1 (tbd) offset (tbd)		tbd tbd		dBc/Hz
G[4]	Gain stability				2.0	dB
t_{ON}[4]	Turn–on time	Tx signal to 90%		3		µs
T_{OFF}[4]	Turn–off time	Tx signal to 10%		2		µs

NOTES:
1. I_TXIN=0.25 Sin wmt, I_TXINX=0.25 Sin wmt, Q_TXIN=0.25 Sin (wmt–90), Q_TXINX=0.25 Sin (wmt–90). The output spectrum will be a SSB one. The tone is at a frequency of 11 MHz.
2. The output current in each arm is the same but 180 degrees out of phase with each other. Also the tuned load of 400 ohms differential, is assumed. The power delivered to 400 ohms will be –10.4 dBm (typ.). The output current measurement is indirect based on output powert measurement.
3. This is measured with respect to the SSB output.
4. Guaranteed by design and or characterization but not final tested.
5. The input bandwidth will be tested by measuring the output THD and signal level using a DSB spectrum where I=Q and the signal is a tone at 22 MHz.

AC ELECTRICAL CHARACTERISTICS IF RECEIVER AND DEMODULATOR

V_{CC}XXX=RX_ON=TX_ON=PLL_ON= +3V TO +5V, V_{EE}XXX = GND1=GND2=GND3= 0V; LO in=100 mV peak at 704 MHz, CLKin=100mV peak, 22 MHz, Ta=25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
RInRx	Differential input impedance	f_{IN}=400 MHz		tbd		kΩ
VG	Voltage gain	AGC at maximum gain	tbd	83		dB
NF[1]	Input noise figure[1]	VGA at maximum gain		7.5		dB
	AGC range			70		dB
	AGC step size			2		dB
	AAGC differential error					dB
	AGC settling time	any AGC step				nS
	Channel matching gain phase	This will be on a best effort basis as mentioned before		0.2 1.0		dB deg
	Output voltage swing	V_{CC}=3V, into Load[3]	1			Vpp
THD[4]	Third Harmonic Distortion	Max. Gain, rated output at 1 MHz		3		%
t_{ON}	Turn–on time	90%		1		µs
t_{OFF}	Turn–on time	90%		1		µs

NOTES:

1. The Receive input is to be differential (using a balun or a differential source such as a differential SAW filter) and matched to external generator's impedance (ex: 50 ohms). The balun may or may not provide any impedance transformation depending on availability. an external L–C matching circuit can provide the rest of the impedance transformation as well absorb the input capacitance of the receiver input. Such a differential input scheme is mandatory to avoid pickup, and keep the noise figure low. A shunt resistor across the input (value TBD) will be used to set the input impedance as a compromise between the matching ease in production versus the noise figure of the receiver.
2. The system board layout has to keep the isolation between the receive inputs and the LO signal as high as possible. Otherwise the LO leakage will overload the receiver.
3. The load is 1000 ohms in parallel with 15pF of capacitor.
4. THD is total harmonic distortion. Since 3rd harmonic will dominate we will just measure this one.

AC ELECTRICAL CHARACTERISTICS IF RECEIVER AND DEMODULATOR

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SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX.	
f_{LO}	Local oscillator input frequency range		140		800	MHz
Z_{LOIN}	Differential input impedance	Between LOin and $LO_{\_INX}$		276 0.6		Ω pF
	LO input sensitivity	Single ended Referred to 50Ω	tbd		tbd	mVpp
	Programmable divider division range step size		64	1	511	
f_{CLK}	Reference clock frequency			8, 11, 22 or 44		MHz
Z_{CLKIN}	Differential input impedance	Between Clk_{IN} and Clk_{INX}		10 1.0		KΩ pF
	CcLK input sensitivity	Referred to 50Ω	50	200	400	mVpk
f_C	Phase detector comparison frequency			1		MHz
I_{REF}	Charge pump reference current			31.2		µA
I_{CP}[1]	Charge pump output current: C0...C2=000 C0...C2=111 step size	I_{REF}=31.25 µA $V_{CP}=V_{CC}$CP/2		0.200 0.400 0.029		mA mA mA
$\frac{I_{CP}}{I_{CP}}$	Relative output current variation	I_{REF}=31.25 µA		1.3	±10	%
I_{CP_M}	Output current matching	I_{REF}=31.25 µA $V_{CP}=V_{CC}$CP/2			±12%	µA
	Output current tolerance with programmed step with temperature with output voltage	CP between 0.8 V and V_{CC} CP=0.8V		±10 ±10 ±5		%

APPLICATION DESCRIPTION

General

The 1630 performs the dIF modulator and demodulator functionality for high–speed wireless data transceivers. The design is optimized for IEEE 802.11 wireless LAN using 11 chips/symbol direct Sequence Spread Spectrum.

Transmitter

The IF quadrature transmitter baseband modulator input is driven from single–ended D/A converters in the DSP chip *using a minimum number of external components.* The baseband signals are DC coupled for fast turn–on and turn–off and for constant carrier testing. A constant output carrier is generated if ITXIN is high and QTXIN is low or vice versa, while this does not offset the ITXINX and QTXINX lines. This requires a good common–mode rejection of the baseband inputs (>20 dB). The typical common–mode input voltage is VCC/2.

The open collector outputs of the mixers are biased by two choke coils, which are part of an LC tank. The LC tank matches the output impedance of the mixers to the input impedance of the upconverter chip (or any filter in between) and suppresses IF harmonics.

Receiver

The receiver part of the SA1638 consists of an IF AGC amplifier, a quadrature demodulator and a pair of baseband amplifiers. The IF AAGC amplifier has its gain controlled by the DSP chip. This ensures linear operation of the receiver chain over a wide dynamic range of input signals. Linear operation is essential for resolving echo's due to multipath reception.

The digital controlled AGC is meant for fast level training for the receiver. During message reception the digital AGC should not change state.

The high gain receiver, which is distributed between the IF and baseband part facilitates interfacing with the RF front–end chip, which normally have moderate gains (up to 20 dB), and SAW IF filters, which mostly have considerable loss (up to 8 dB) without external amplifiers.

The baseband amplifiers have a high drive capability (1 Vpp into 1kΩ, 15 pF for VCC=3V) that facilitates direct interfacing to the A/D converter without active external elements.

Power control

The DSP chip contains power management logic that support at least three modes of operation: SLEEP (all off), Transmit (PLL on, Tx on, Rx standby) and Receive (PLL on, Rx on, Tx off) and supplies the corresponding logic control lines to the IF chip. The data transmission protocol requires fast transmit/receive turnaround times (2µs). The maximum power–up time from standby mode is 0.25 ms, which is determined by the PLL and VCO characteristics.

Local oscillator

The SA1630 has an integrated synthesizer that uses an external VCO operating on twice the IF frequency. It is internally divided by 2 for obtaining quadrature signals. The divided VCO signal is not externally available. This minimizes the LO feedthrough to the IF input port and hence minimizes output dc glitches when the IF gain is switched.

The PLL reference clock is derived from the 22 MHz DSP clock. The available divider ratios facilitate both 1 and 2 MHz phase comparison frequency from a 22 MHz and an optional 44 MHz clock respectively. In essence the reference divider will have programmable dividers ratios of 8, 11, 22 and 44.

The VCO is fed from a stabilized supply. Such a stabilized supply is necessary in order to prevent oscillator jitters due to Rx/Tx switching. The effect of oscillator jitters is further minimized when using a high PLL loop bandwidth, which on its turn requires a high phase comparison frequency (1 MHz, preferably 2 MHz).