SEI-1618PG Fractional Phase Lock Loop Specification

The SEI-1618PG is a Phase Lock Loop (PLL) chip designed to provide frequency control in a PLL at fractional multiples of the reference frequency. Its fractional design provides improved phase noise in phase lock systems within the loop bandwidth and gives a greater flexibility than any other fractional chip on the market. The device fractionality can be programmed to be any value from $^1/_1$ to $^1/_{64}$. To form a complete PLL only a VCO, an external loop filter and dual modulus prescaler are required. The use of an external prescaler allows the designer the flexibility of choosing one with the most appropriate divide ratios.

The device runs on a 2.5 to 5.5 V power supply, accepting standard 2.5 to 5.5 V CMOS logic level as input and delivering 2.5 to 5.5 V CMOS levels at its outputs. The divided VCO input may vary in frequency from DC to 100 MHz, giving a maximum frequency into an external ÷16/17 dual modulus of 1600 MHz, for example.

The device features selectable polarities on the phase detector and the modulus control line to provide easy configuration into a given system. The on chip phase detector supplies both a differential voltage and a tri-state current source output. An on chip-inverting amplifier is provided for use with an external crystal to generate a frequency reference.

- 20 pin plastic SOL package
- Supply voltage 2.5 V to 5.5 V
- 10 mA typical I_{dd} current (input frequency 50 MHz; V_{dd} = 3.0 V)
- Divided VCO frequency up to 100 MHz
- Divided VCO (dual modulus output) amplitudes down to 0.5 V peak to peak accepted (AC coupled and biased)
- Reference input frequency up to 20 MHz (over range to 100 MHz)
- On chip reference oscillator
- Fractionalities programmable $^1/_1$ to $^1/_{64}$, providing up to 36 dB in theoretical phase noise improvement for a given frequency resolution
- Counters provide internal divide ratio of up to 255 (overall divide ratio of 255 x P where P is the lower division value of the dual modulus used)
- Dual modulus divide ratios up to a ÷64/65 supported
- F_V (VCO signal divided to reference frequency) and F_R (phase reference at phase comparison frequency) outputs provided for easy debug
- Control of the phase detector and modulus control polarities
- Lock detect output (low = locked, high = not locked)
- Differential voltage and tri-state current source phase detector outputs provided
- Serial data output to enable daisy chaining of serial controlled devices

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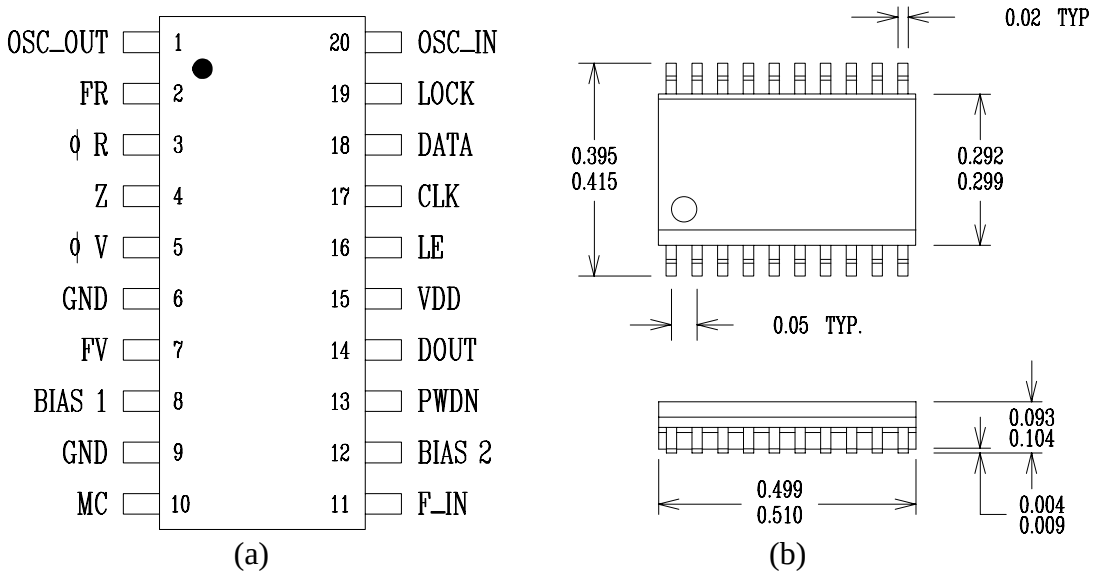

Figure 1. (a) device pin out, (b) package dimensions (in inches)

PIN ASSIGNMENTS

Pin #	Pin name	I/O	Pin Description
1	OSC_OUT	O	Crystal
2	F_R	O	F_R, phase reference output
3	ϕR	O	Phase detector output,
4	Z	O	Phase detector tri-state output, Z
5	ϕV	O	Phase detector output, V
6	GND	PWR	Ground
7	F_V	O	F_V, divided VCO phase output
8	BIAS 1	-	(Must be pulled up to V_{dd} with 10 kΩ)
9	GND	pwr	Ground
10	MC	O	Dual modulus control signal to external dual modulus
11	F_IN	I	VCO divided signal, device clock, from ext. dual modulus
12	BIAS 2	-	(Must be pulled up to V_{dd} with 10 kΩ)
13	PDWN	I	Crystal oscillator power down (active high)
14	DOUT	O	Serial data output for daisy chain
15	V_{dd}	pwr	Power supply
16	LE	I	serial latch enable
17	CLK	I	Serial data clock
18	DATA	I	Serial data input
19	LOCK	O	Lock detect output
20	OSC_IN	I	Crystal oscillator inverting amplifier input

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{dd}	Power supply voltage	0 to +5.5	VDC
T_s	Storage temperature	-65 to +125	°C
T_o	Operating temperature	-40 to +85	°C

SOIC Notes:

1. Devices must be baked @ +125°C for 12 hours to remove any accumulated moisture prior to soldering if the units have been exposed to a relative humidity >20% for more than 24 hours.

2. Maximum reflow solder temperature is +260°C for 10 seconds and no greater than 5°C/second thermal shock should be applied.

3. Handle only at certified static-safe workstation.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Condition
F_{in}	F_IN			100	MHz	V_{dd}=3.0 to 5.0 V
F_{osc}	OSC_IN		10	20	MHz	V_{dd} =3.0 to 5.0V
I_{dd}	Supply current		10	15	mA	V_{dd} =3.0 V, f_{in}=50 MHz
			20	30	mA	V_{dd} =5.0 V, f_{in}=50 MHz
V_{in}	in Sen. F_IN	0.5			V p-p	note 1
V_{osc}	in Sen. OSC_IN	0.5			V p-p	note 1
£(f)	Phase detector floor noise			-155	dBc/Hz	1 MHz at the input of the phase detector

Note 1. AC coupled and biased to +2V ± 0.15V

2. Supply voltage must be equal to or greater than the TTL "HIGH"

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TIMING REQUIREMENTS

Symbol	Parameter	VDD	Spec.	Unit
F_{clk}	Serial Data CLK Frequency, Assuming 25% Duty Cycle	3 V 5 V	dc to 5 dc to 5	MHz
t_{s1}	Minimum Setup Time, Data to CLK	3 V 5 V	10 8	nS nS
t_h	Minimum Hold Time, CLK to Data	3 V 5 V	12 10	nS nS
t_{s2}	Minimum Setup Time, CLK to LE	3 V 5 V	10 8	nS nS
t_{rec}	Minimum Recovery Time, LE to CLK	3 V 5 V	5 5	nS nS
$t_{w(H)}$	Minimum Pulse Width, CLK and LE	3 V 5 V	50 50	nS nS
t_r, t_f	Maximum Input Rise and Fall Time Any Input	3 V 5 V	5 5	uS uS

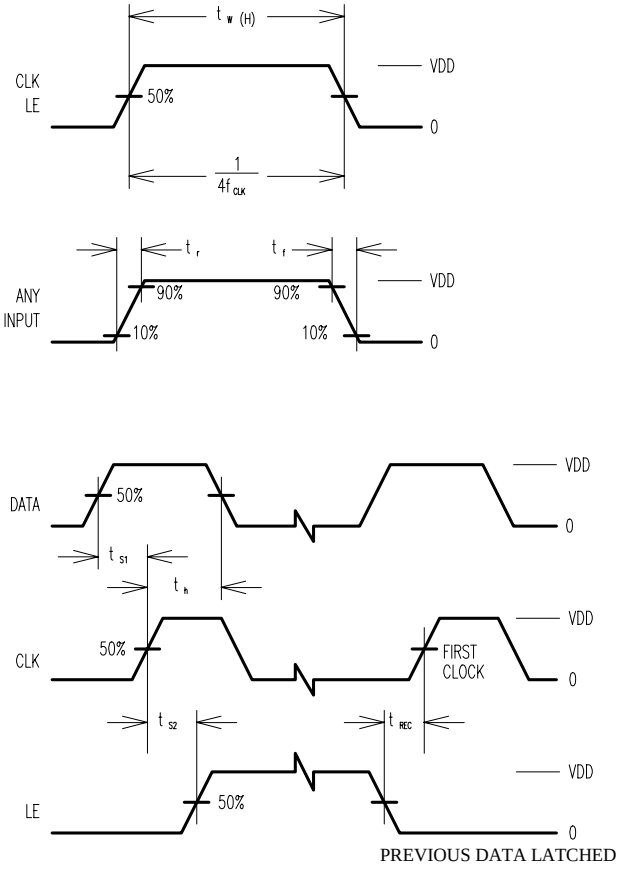

Figure 2. Switching waveforms

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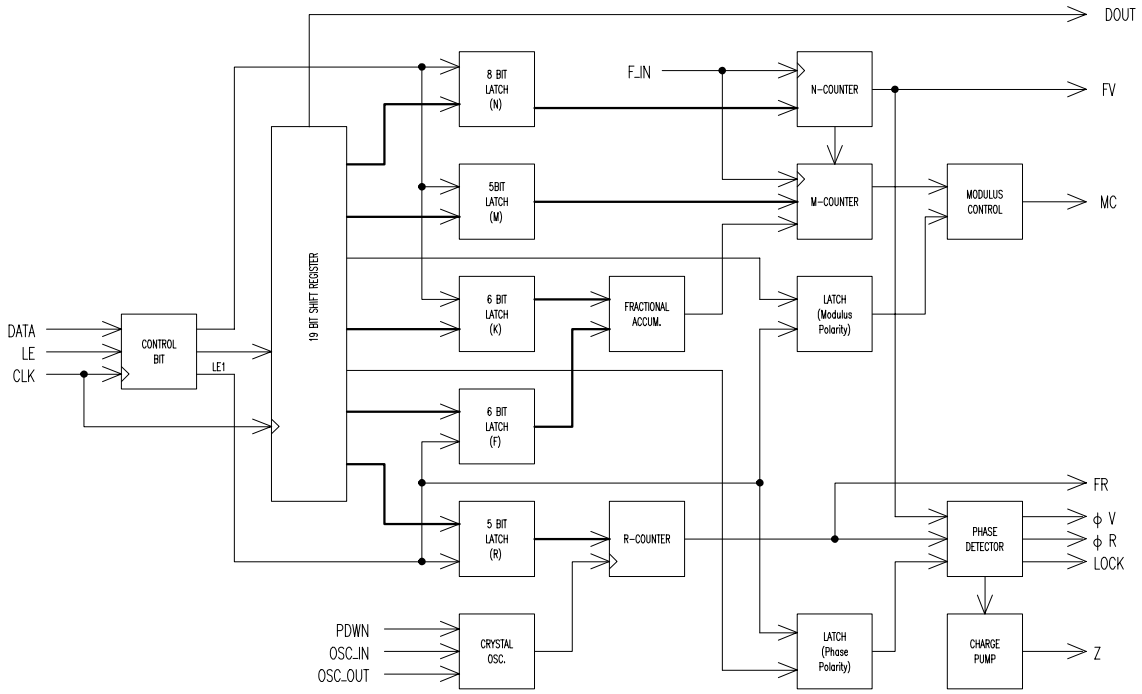

Figure 3. Internal block diagram

DEVICE CONTROL

The variables used to define the vectors sent into the device in order to obtain a given frequency are defined below:

MP	(1 bit)	Modulus control polarity: value of modulus control line for M out of N counts
PP	(1 bit)	Phase detector polarity: determines sign (±) of K_F (0=pos, 1=neg.)
R	(5 bits)	Frequency reference divider control vector (reference division = R+ 1)
F	(6 bits)	Fractionality denominator control vector (fractionality = F + 1)
K	(6 bits)	Fractionality numerator control vector (numerator = K)
N	(8 bits)	VCO dividing counter control vector (division = N)
M	(5 bits)	Dual modulus modulating counter control vector: increments P for M out of N counts
P	#	Dual modulus lower division value (i.e. 16 for a ÷16/17 dual modulus)
F_{ref}	#	Reference frequency supplied to the device

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The phase comparison frequency seen by the phase detector is then:

$$FR = F_{ref} \div (R+1) \quad \text{eq. 1}$$

The fractionality is:

$$f_{frac} = F + 1 \quad \text{eq. 2}$$

The frequency step size at the output is:

$$F_{step} = FR \div f_{frac} \quad \text{eq. 3}$$

The output frequency when the PLL is in lock is:

$$F_{out} = [\, N \times P + M + (K \div f_{frac})] \times FR \quad \text{eq. 4}$$

$$N = INT\,[F_{out} \div P \div FR] \quad \text{eq. 5}$$

$$M = INT\,(F_{out} \div FR) - P \times N \quad \text{eq. 6}$$

$$K = INT\,[(F_{out} \div FR - P \times N - M) \times f_{frac}] \quad \text{eq. 7}$$

For most dual modulus prescalers the lower divide ratio is selected when the modulus control line is high. To interface with these set MP = 0. MP = 1 if the lower division is engaged when the modulus control is low.

The phase polarity setting depends on the polarity of subsequent portions of the system (the sign of K_{VCO}, and which op-amp inputs the differential outputs are connected to). For a detailed diagram of the phase detector response, see Phase Detector Characteristics below. When PP = 0 the phase detector voltage/current outputs are:

$$Z = |K_{\phi Z}| \bullet (\phi R - \phi V) \quad (PP = 0)$$

$$V_{\phi R} = -\phi V = |K_{\phi \Delta}| \bullet (\phi R - \phi V) \quad (PP = 0)$$

$$I_Z = -|K_{\phi Z}| \bullet (\phi R - \phi V) \quad (PP = 1)$$

$$V_{\phi R} = -V_{\phi V} = -|K_{\phi \Delta}| \bullet (\phi R - \phi V) \quad (PP = 1)$$

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The serial interface contains a de-multiplexer allowing one serial stream to contain the programming information for either of two sets of latches. The first set of latches contains the variables that are in general constant for any synthesizer design: the reference division control (R), the fractionality control (F), the modulus control polarity (MP) and the phase detector polarity (PP). The second set of latches contains the variables that will be changed whenever the desired output frequency is changed: the internal division (N), the dual modulus modulating counter (N) and the fractional numerator (K). This scheme allows a decrease in the amount of time needed to load a new frequency, as the redundant constant information need not be continually sent.

The MSB of all vectors is loaded first. The last bit in the stream is the demux control bit 'CB', and the constant vectors F, R, PP, MP, CB = 0 loads the variable vectors N, M, K.

⇓ First bit **CB ⇓**

MP	PP	R4	R3	R2	R1	R0	F5	F4	F3	F2	F1	F0	1

⇓ First bit **CB ⇓**

K5	K4	K3	K2	K1	K0	M4	M3	M2	M1	M0	N7	N6	N5	N4	N3	N2	N1	N0	0

The shift register data is loaded on the rising edge of the serial clock. The internal data latches are loaded on the LE low to high transition.

EXAMPLE

Configuration example:

F_{ref} = 10 MHz Reference frequency at OSC_IN

FR = 1.25 MHz Reference frequency at the input of the phase detector

Step size = 50 kHz Required resolution

K_{VCO} = positive

P = 16 ÷16/17 dual modulus prescaler is used

Therefore

reference division = 8
f_{frac} = 25
R = 7
F = 24
PP = 0 (Z output or FR tied to the op-amp input)
MP = 0 (for most dual modulus prescaler)

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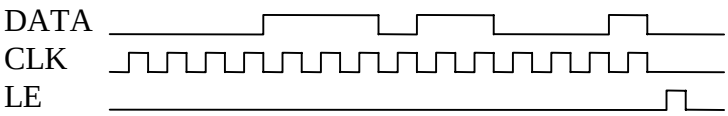
Configuration stream needs to be sent only once after power up. Note that each bit is duplicated in the examples below due to the manner in which the supplied software operates.

	MP	PP	R	F	CB
DATA (pin 18)	00	00	0000111111	001111000000	11 xxxx
CLK (pin 17)	01	01	0101010101	010101010101	01 0000
LE (pin 16)	00	00	0000000000	000000000000	00 0100



Frequency control stream (example):
Assume that:

F_{out} = 843.8 MHz

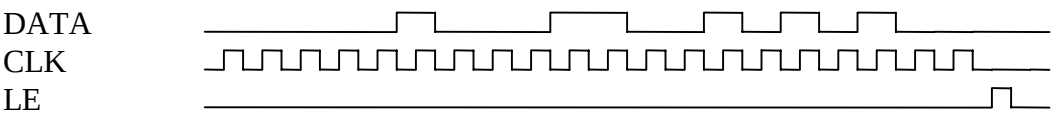
therefore:

N = INT (843.8 MHz ÷ 16 ÷ 1.25 MHz) = 42

M = INT (843.8 MHz ÷ 1.25 MHz - 42 • 16) = 3

K = INT [(843.8 MHz ÷ 1.25 MHz - 42 • 16 - 3) • 25] = 1

	K	M	N	CB
DATA	000000000011	0000001111	0000110011001100	00 xxxx
CLK	010101010101	0101010101	0101010101010101	01 0000
LE	000000000000	0000000000	0000000000000000	00 0100



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PHASE DETECTOR CHARACTERISTICS

The phase detector is a digital phase/frequency detector with standard output waveforms as shown below. The nominal gain of the phase detector depends on the power supply for the differential voltage outputs.

$K_{\phi\Delta}$ = VDD ÷ (2 x π) V/rad

$K_{\phi Z}$ = 1 mA ÷ (2 x π) mA/rad

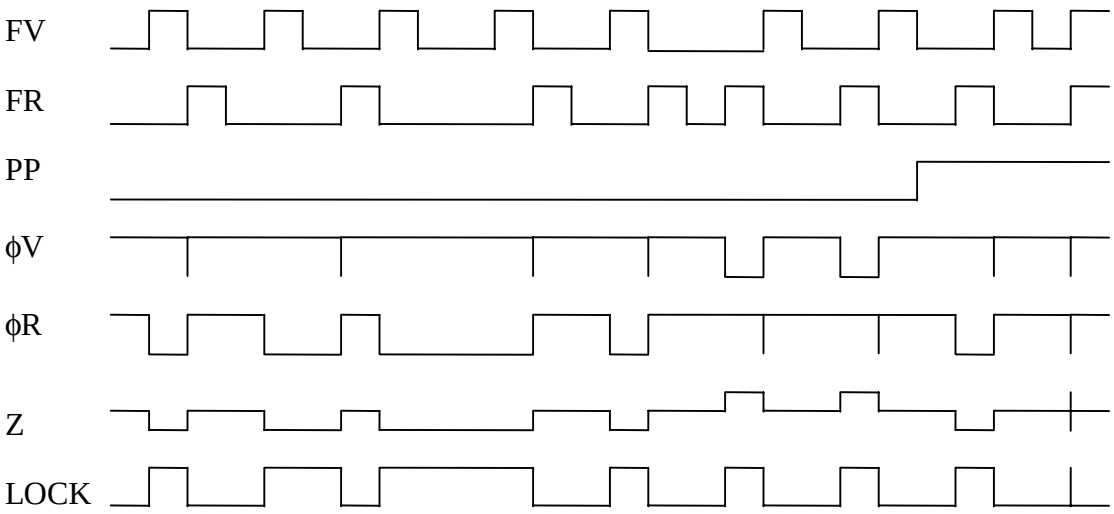

Figure 4. Phase detector waveforms

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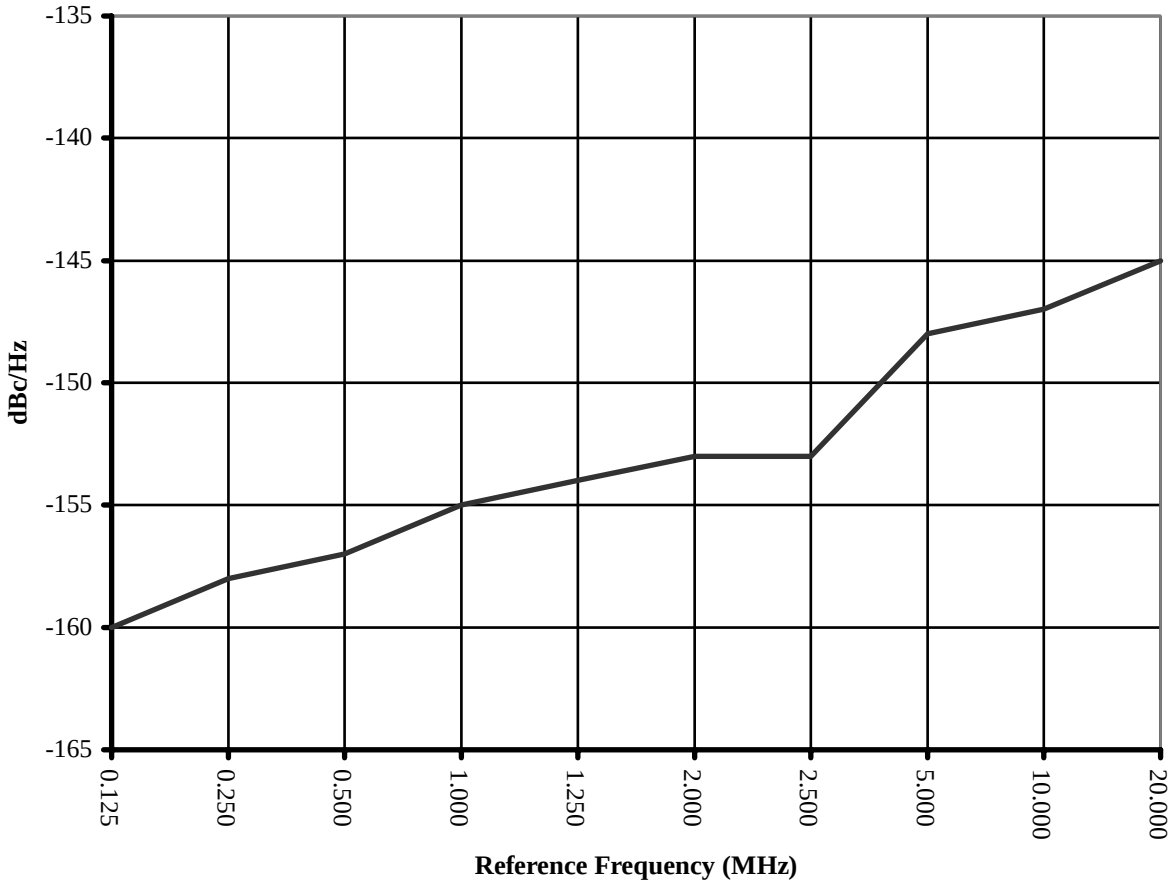
Actual SEI-1618PG Noise Floor
(by reference frequency)



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