Image rejecting front-end for DECT applications

UAA2077AM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 25 dB on-chip image rejection
- IF I/Q combiner at 110 MHz
- On-chip quadrature network
- RX fast **on/off** power-down mode
- Shrink small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DECT hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2077AM contains a high frequency low noise receiver front-end intended to be used in DECT mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077AM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch enables the upper or lower image frequency to be rejected.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers. All RF and IF inputs or outputs are balanced.

Two pins RXON and SXON are used to control the different power-down modes. A special mode of operation called synthesizer-on mode (SX mode), controlled by pin SXON can be used to minimize the LO pulling when the receiver is turned **on**. When SXON is HIGH, all internal buffers on the LO path are turned **on**. Pin SBS allows a selection of whether to reject the upper or lower image frequency. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	T_{amb} = 0 to +70 °C	3.15	4.0	5.3	V
		over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	receive supply current		21.5	26.5	33.5	mA
$I_{CC(PD)}$	supply current in power-down		–	0.2	50	µA
T_{amb}	operating ambient temperature		–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

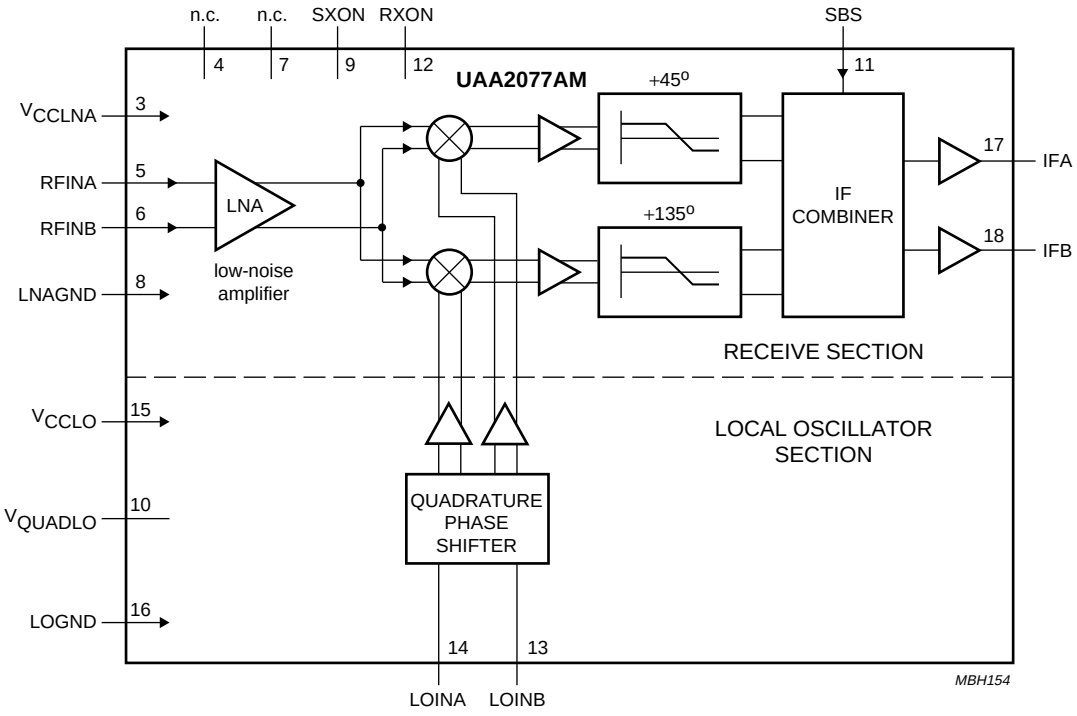


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
V_{CCLNA}	3	supply voltage for LNA and IF parts
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA and IF parts
SXON	9	SX mode enable (see Table 1)
V_{QUADLO}	10	input voltage for LO quadrature trimming
SBS	11	sideband selection
RXON	12	RX mode enable (see Table 1)
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
n.c.	19	not connected
n.c.	20	not connected

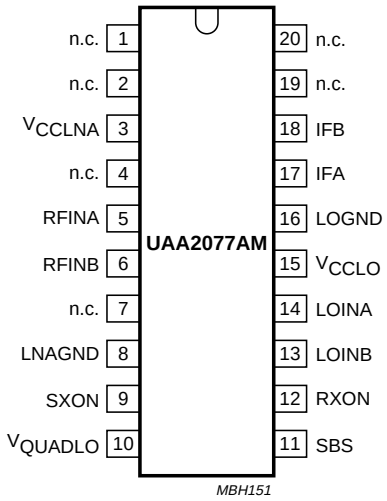


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels.
The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} > f_{RF}$ (SBS = 1)
- $f_{LO} < f_{RF}$ (SBS = 0).

where f_{RF} is the frequency of the wanted signal.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; for example, a 1 kΩ resistor load at each IF output, plus a differential 2 kΩ load consisting of the input impedance of the IF filter or the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 2 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, **on/off**, of the receive section is controlled by the hardware input RXON.

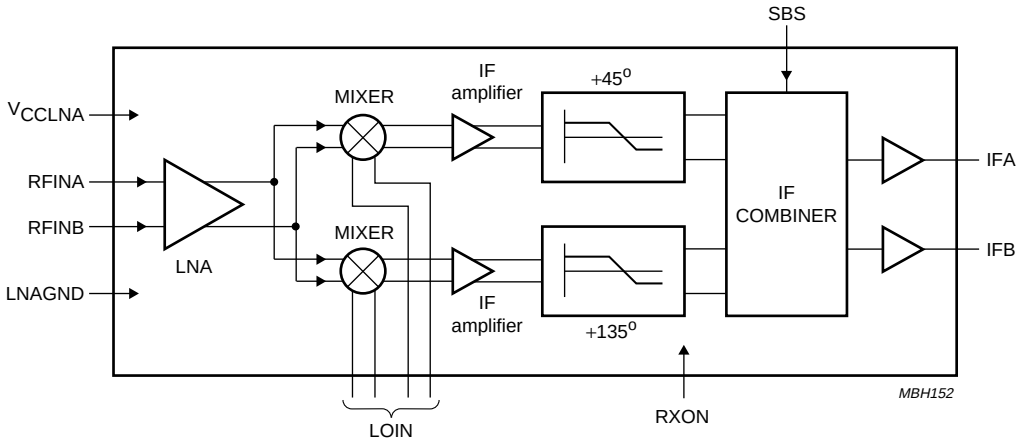


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This should be achieved by connecting a resistor between V_{QUADLO} and V_{CC}. Over 25 dB of image rejection can be obtained by an optimum resistor value.

A synthesizer-on (SX) mode is used to power-up the LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive mode. This mode is active when SXON = 1.

There are no internal biassing components attached to the pins LOINA and LOINB. These pins are connected by capacitors to the internal phase shifting network.

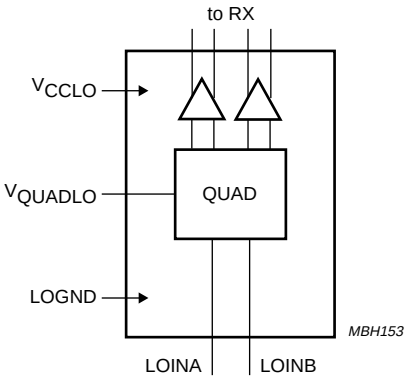


Fig.4 Block diagram, LO section.

Table 1 Control of power status

EXTERNAL PIN LEVEL		CIRCUIT MODE OF OPERATION
RXON	**SXON**	
LOW	LOW	power-down mode
HIGH	X	RX mode (receive and LO sections **on**)
LOW	HIGH	SX mode (only LO section **on**)

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
P_{max}	maximum power dissipation	–	250	mW
T_{stg}	IC storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with *“MIL-STD-883C Class 2 (method 3015.5)”*.

DC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins V_{CCLNA} and V_{CCLO}						
V_{CC}	supply voltage	T_{amb} = 0 to +70 °C	3.15	4.0	5.3	V
		over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	supply current in RX mode		21.5	26.5	33.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	0.2	50	µA
$I_{CC(SX)}$	supply current in SX mode		3	5	7	mA
Pins RXON, SXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFINA and RFINB						
V_I	DC input voltage level	receive section **on**	–	2.0	–	V
Pins IFA and IFB						
I_O	DC output current	receive section **on**	–	2.5	–	mA

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = –30 to +85 °C; unless otherwise specified.

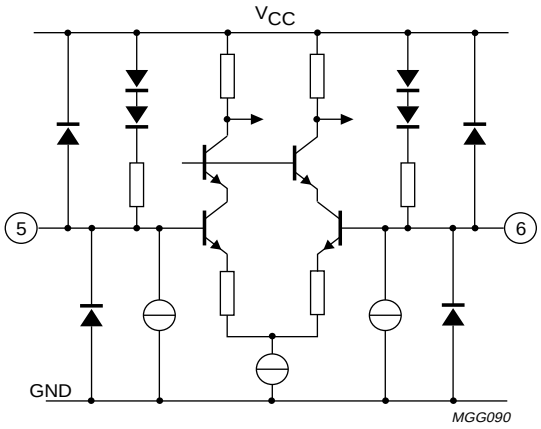
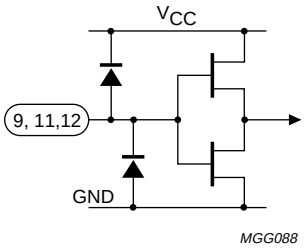
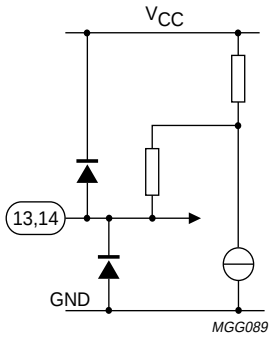
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	60	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1890 MHz	–	1	–	pF
f_{iRX}	RF input frequency		1880	–	1900	MHz
RL_{iRX}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	–	dB
ΔG/T	gain variation with temperature	T_{amb} = –30 to +25 °C; note 2	–20	0	+10	mdB/°C
		T_{amb} = +25 to +85 °C; note 2	–40	–30	–20	mdB/°C
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	–26	–23	–	dBm
DES3	3 dB desensitisation point	interferer frequency offset: 3 MHz; differential RF inputs to differential IF outputs; note 1	–	–30	–	dBm
		interferer frequency offset: 20 MHz; differential RF inputs to differential IF outputs; note 1	–	–28	–	dBm
$IP2D_{RX}$	2nd order intercept point	differential RF inputs to differential IF outputs; note 2	15	30	–	dBm
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	–23	–17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs; notes 2 and 3	–	4.3	5.0	dB

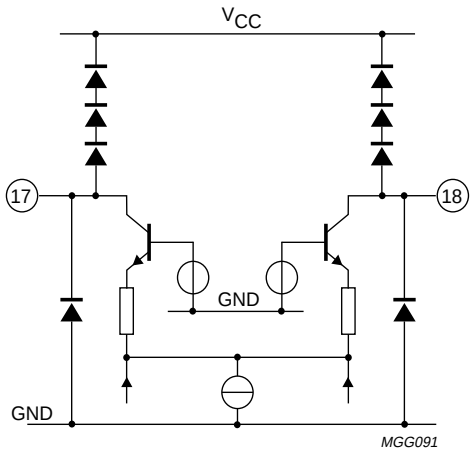
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_{LRX}	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{oRX}	return loss on matched IF output	balanced; note 1	11	15	–	dB
f_{oRX}	IF frequency		–	110	–	MHz
IR	rejection of image frequency	$f_{LO} < f_{RF}$; f_{IF} = 110 MHz; note 4	26	32	–	dB
Local oscillator section (receive section enabled)						
f_{iLO}	LO input frequency		1770	–	2010	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 1780 MHz	–	40	–	Ω
C_{iLO}	LO input capacitance (imaginary part of the parallel input impedance)	balanced; at 1780 MHz	–	2	–	pF
RL_{iLO}	return loss on matched LO input (including power-down mode)	note 1	9	12	–	dB
ΔRL_{iLO}	return loss variation ratio between SX and RX modes	linear S_{11} variation; note 1	–	5	–	mU
P_{iLO}	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = 25 °C.
2. Measured and guaranteed only on UAA2077AM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = 25 °C. V_{QUADLO} open-circuit.

INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
V_{CCLNA}	3	4.0	
RFINA	5	2.0	
RFINB	6	2.0	
LNAGND	8	0	
SXON	9	–	
SBS	11	–	
RXON	12	–	
LOINB	13	–	
LOINA	14	–	
V_{CCLO}	15	4.0	

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
LOGND	16	0	
IFA	17	2.5	
IFB	18	2.5	

APPLICATION INFORMATION

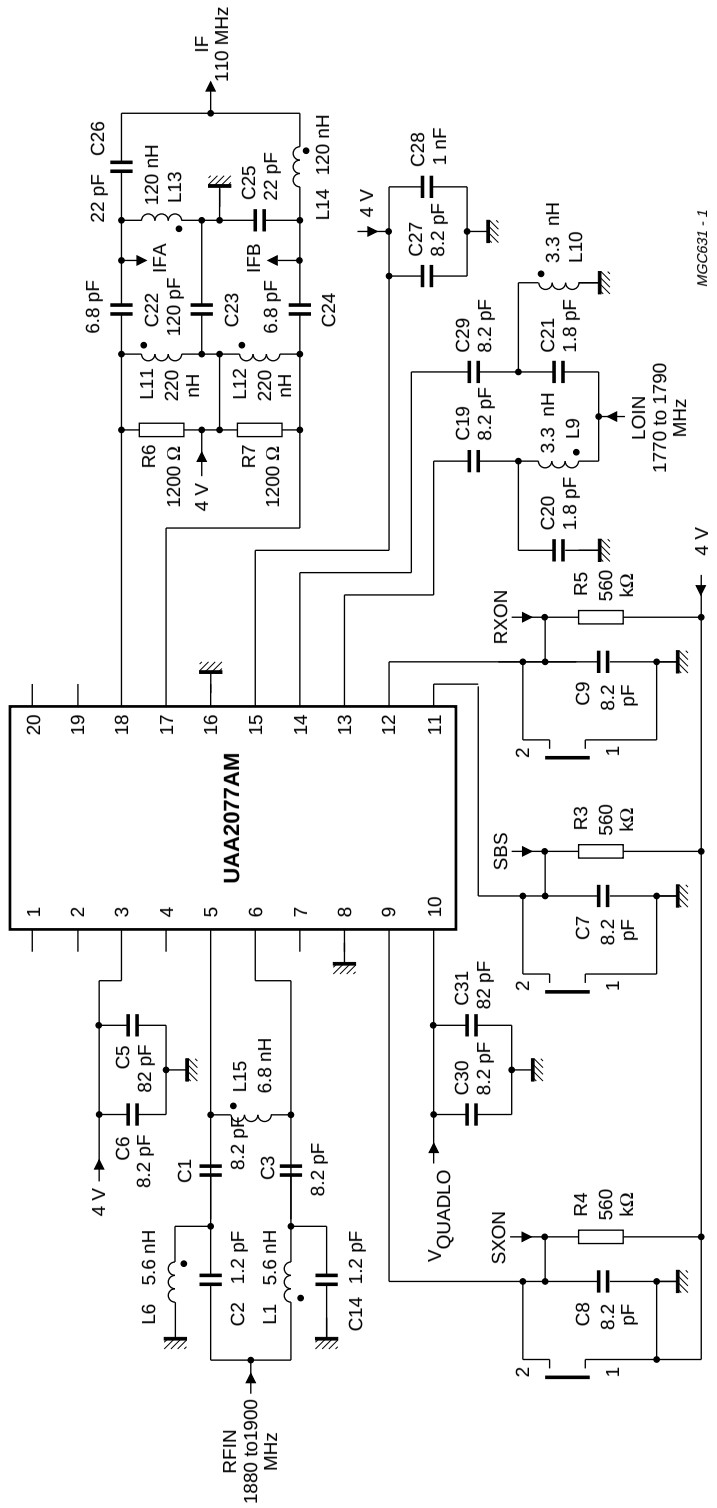


Fig.5 Application diagram.

Figure 5 illustrates the electrical diagram of the UAA2077AM Philips demonstration board for DECT applications. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.