Image rejecting front-end for GSM applications

UAA2072M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for up to 60 dB on-chip image rejection
- Programmable IF I/Q combiner
- On-chip programmable quadrature network
- Very fast 3-wire control bus
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2072M contains both a receiver front-end and a high frequency transmit mixer intended to be used in the GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2072M is its ability to provide at least 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. The precision needed for this signal processing is achieved by compensating for process spreads and trimming for the choosen IF frequency and the LO band centre frequency via a 3-wire serial bus interface.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The overall phase rotation is programmable for maximum image rejection at a given IF. The IF output drivers have differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced, and 200 Ω is used as standard RF impedance.

A 3-pin unidirectional serial interface is used to program the circuits, using 16-bit words. This data bus allows compensation of process spreads, and is used to adjust for maximum image rejection performance at a given IF. It also offers a selection to reject the upper or lower image frequency and control over the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.5	4.8	5.3	V
I_{CCRX}	receive supply current	26	31.5	38	mA
I_{CCTX}	transmit supply current	10	12	14	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2072M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

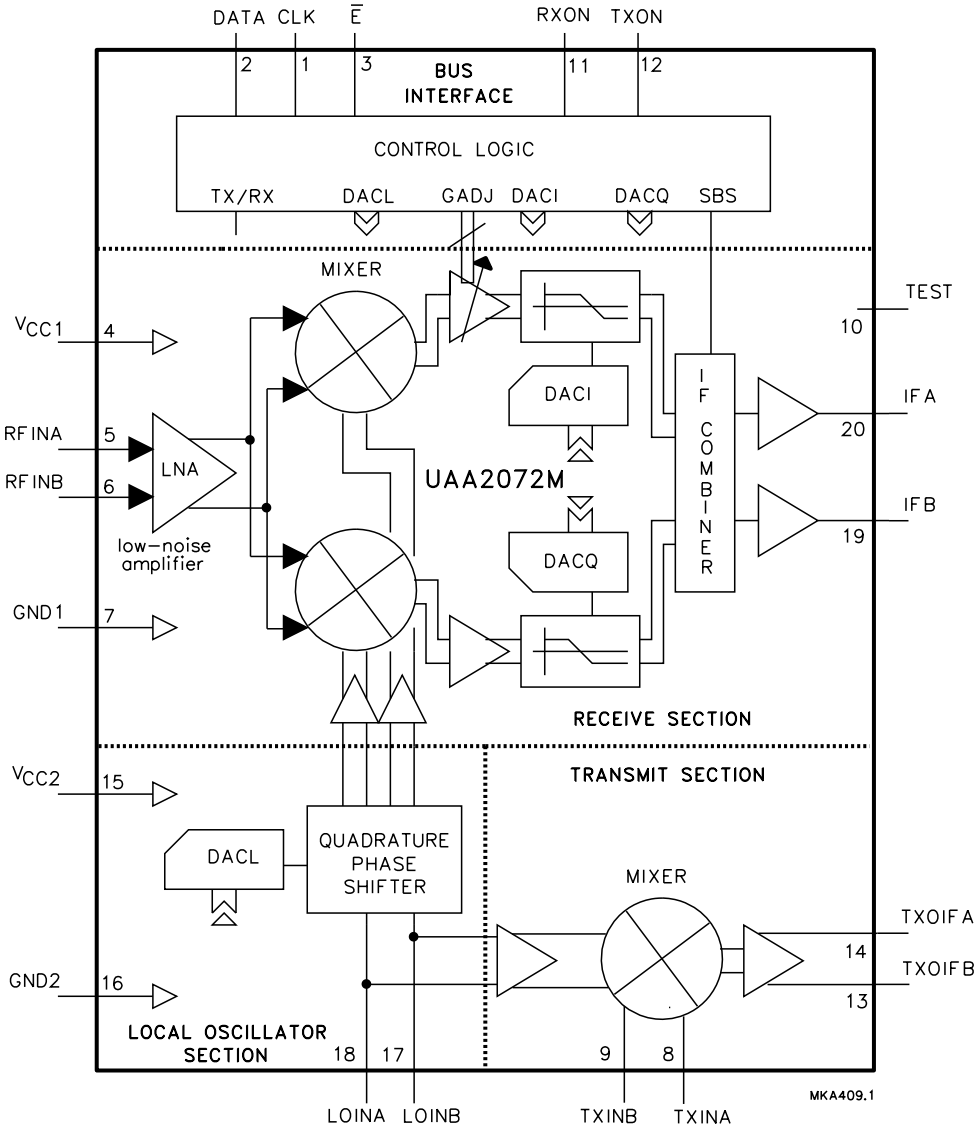

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	serial bus clock
DATA	2	serial bus data
$\overline{E}$	3	serial bus enable (active LOW)
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground for synthesizer buffer and logic
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
TEST	10	reserved for test purposes, should be connected to ground
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for local oscillator parts
GND2	16	ground for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

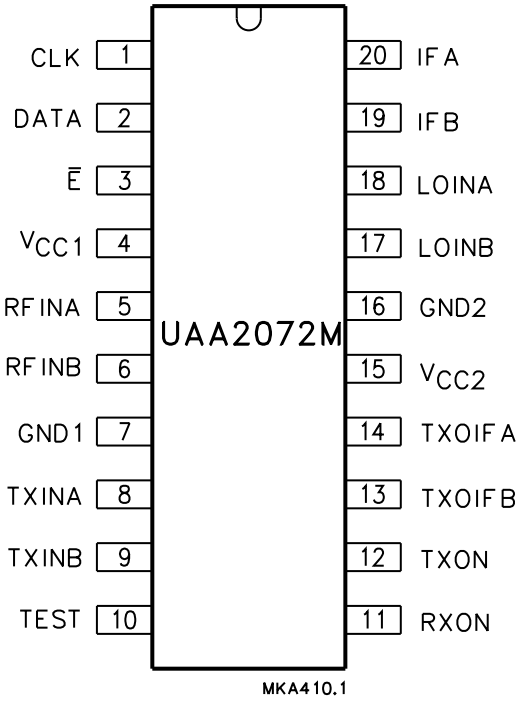

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

The serial bus interface is used for tuning to maximum image rejection at a given IF. The contents of registers ip5 to ip0 and qp5 to qp0 (named IF phase adjustment words) are digital-to-analog converted in the DACI and DACQ blocks. The obtained internal voltages control the phase shift in I and Q; thus allowing them to be trimmed precisely to 45° and 135° at any given IF between 30 and 90 MHz. The gain in the I channel is slightly adjustable using the four bits ga3 to ga0 to allow compensation of small gain mismatches between I and Q.

One bit (sbs) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 200 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to V_{CC} + 3V_{be} or 3 diode forward voltage drops.

In the event of only one output being used, a 1 kΩ resistive load in parallel with a tuning inductor to V_{CC}, provides a matched 1 kΩ output to the external IF filter.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON or via the bus interface by changing the srx-bit in the internal register.

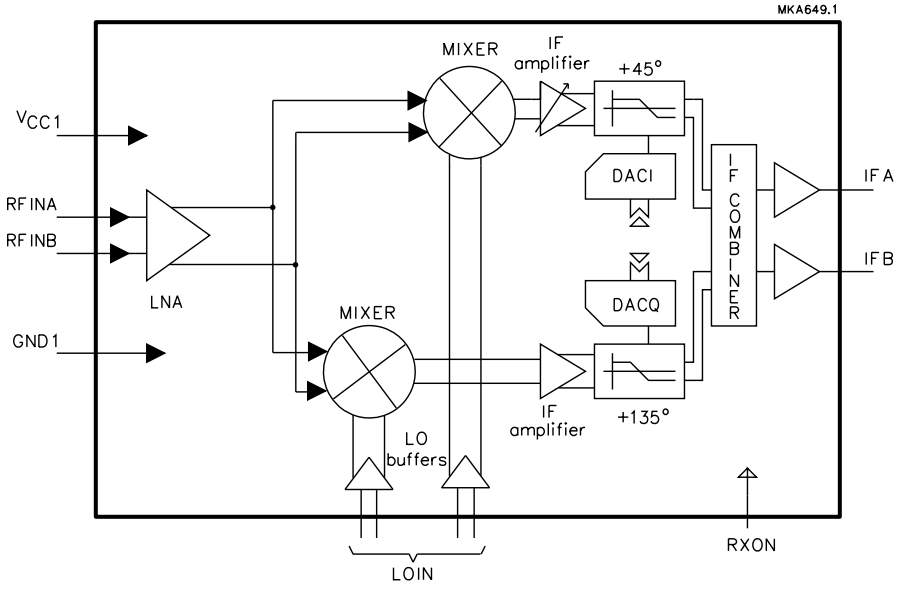

Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by programming via the serial bus. The word ‘lo5 to lo0’ named LO Quad Centre Frequency Adjustment word is converted to an analog voltage in a digital-to-analog converter (DACL, see Fig.6). This voltage trims the all-pass network to the selected LO frequency range. To obtain the 30 dB specified image rejection the precision required on this trimming remains low.

The LO input impedance is 100 Ω differential. Switching from RX to TX or power-down mode has little influence on the LO input impedance.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (common collector type).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON or via the serial bus interface by changing the stx-bit in the internal register.

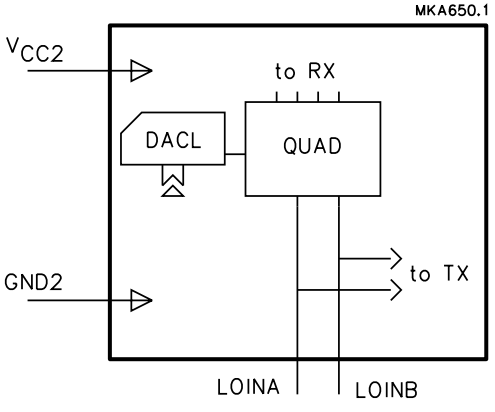

Fig.4 Block diagram, LO section.

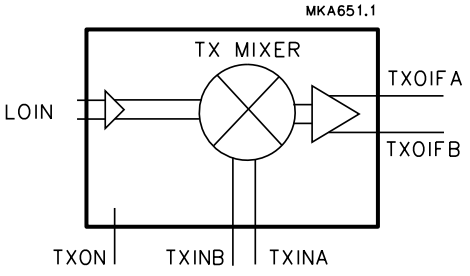

Fig.5 Block diagram, transmit mixer.

Serial bus interface

The 3-wire serial bus interface allows control over the selective power-up of the transmit, receive and LO buffer circuits, the tuning of the LO quadrature and IF quadrature circuits and the selection of sideband rejection. The interface consists of a 16-bit programming register, three working latches and three DACs which provide the tuning voltages for the image rejection of the receive quadrature circuits.

BUS FORMAT

A 3-wire unidirectional bus is used to program the circuit, the 3 wires being: DATA, CLOCK (CLK) AND ENABLE ($\overline{E}$). The timing diagram is illustrated in Fig.6. The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their corresponding data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed working latch when $\overline{E}$ returns HIGH.
Only the last 16 bits clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. If $\overline{E}$ returns HIGH while CLK is still LOW, the extra clock edge produced will cause data shift. The bus interface will not output any address recognition.

Data is entered with the most significant bit first. The leading 12 bits make up the data field, while the trailing 4 bits comprise the address. The first bit entered is p1, the last bit p16. The bits in the programming registers and addresses are arranged as shown in Table 1.

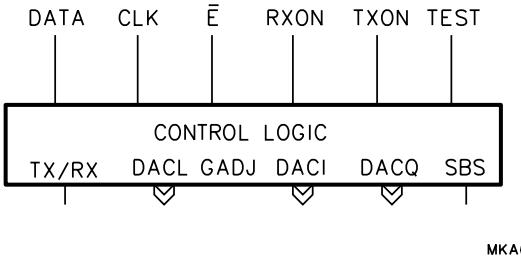

Fig.6 Block diagram, serial bus interface.

Table 1 Register bit allocation

REGISTER BIT ALLOCATION															
FIRST															**LAST**
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16
DATA FIELD												ADDRESS			
dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0
This register is reserved for test purposes and should not be programmed												0	0	0	0
X	X	X	X	sbs	X	X	X	X	hpn	srx	stx	0	0	0	1
ga3	ga2	ga1	ga0	X	X	lo5	lo4	lo3	lo2	lo1	lo0	0	0	1	0
ip5	ip4	ip3	ip2	ip1	ip0	qp5	qp4	qp3	qp2	qp1	qp0	0	0	1	1

Table 2 Bit allocation description

BIT	REMARKS	LOGIC		PRESET
stx	software transmit power-on	1 = power-up	0 = power-down	0
srx	software receive power-on	1 = power-up	0 = power-down	0
hpn	hardware priority not (selects if power status of blocks is controlled via hardware or software)	1 = soft priority	0 = hard priority	0
sbs	sideband select	1 = upper sideband selected	0 = lower sideband selected	0
ga3 to ga0	IF I channel gain adjustment			0111
lo5 to lo0	LO quadrature centre frequency adjustment			011111
ip5 to ip0	IF I channel phase adjustment			011111
qp5 to qp0	IF Q channel phase adjustment			011111
X	not used			

Table 3 details the different power-up modes of the circuit. Attention should be paid to the hpn-bit. This bit enables the RXON and TXON pins to take any logic position when software programming for power-up is used.

Table 3 Control of power status (note 1)

REGISTER BIT STATUS			EXTERNAL PIN LEVEL		CIRCUITS POWER STATUS	
hpn	**stx**	**srx**	**TXON**	**RXON**	**TRANSMIT**	**RECEIVE**
0	X	X	LOW	LOW	off	off
0	X	X	LOW	HIGH	off	on
0	X	X	HIGH	LOW	on	off
0	X	X	HIGH	HIGH	on (2)	on(2)
1	0	0	x	x	off	off
1	0	1	x	x	off	on
1	1	0	x	x	on	off
1	1	1	x	x	on(2)	on(2)

Notes

1. X = don't care; x = HIGH or LOW logic voltage level applied at designated pin.
2. Circuit is operative in this mode but specification is NOT guaranteed.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	v
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	4.5	4.8	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	26	31.5	38	mA
I_{CCTX}	supply current	transmit mode active; DC tested	10	12	14	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	µA
Pins: CLK, DATA, $\overline{E}$, RXON, TXON and TEST						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.7	2.1	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.2	2.5	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	2.5	2.9	3.4	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced	–	200	–	Ω
f_{RFI}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input impedance	note 1	15	20	–	dB
G_{CP}	conversion power gain	RF impedance to 1 IF output matched to 500 Ω	20	23	26	dB
		RF impedance to differential IF outputs matched to 1 kΩ differential	23	26	29	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.1	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	−26	−24.5	–	dBm
$IP2_{RX}$	2nd order intercept point referenced to the RF input	single-ended output; note 2	+15	+22	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	+32	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−18	−15	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	4	5	dB
$Z_{L(IF)}$	typical application IF output load impedance	unbalanced	–	500	–	Ω
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	30	71	90	MHz
		RF > LO	30	45	50	MHz
f_{IR}	image frequency rejection	note 4	30	–	–	dB
f_{IRp}	image rejection at preset	superheterodyne; f_{IF} = 71 MHz; note 1	30	35	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		875	–	1050	MHz
Z_{LO}	LO input impedance	balanced	–	100	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		−7	−4	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	1000	–	Ω
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		880	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	8	10	12	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		–20	–15	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–10	–7	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	–	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2072M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2072M demonstration board.
3. This value includes printed-circuit board and balun losses.
4. This value might be dependent upon control values sent by a microcontroller via the serial bus. This performance is maintained over the RF band for a fixed phase rotation control word.

TIMING CHARACTERISTICS

Typical values measured at V_{CC} = 4.8 V; T_{amb} = 25 °C; maximum value conditions under maximum clock speed; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial bus interface					
f_{clk}	clock frequency	–	–	13	MHz
Serial programming clock (pin CLK)					
t_r	rise time	–	10	40	ns
t_f	fall time	–	10	40	ns
T_{cy}	clock period	75	–	–	ns
Enable programming (pin $\overline{E}$)					
t_{START}	delay to rising edge of clock	30	–	–	ns
t_{END}	delay from last edge of clock	10	–	–	ns
t_W	minimum inactive pulse width	75	–	–	ns
t_{NEW}	delay from $\overline{E}$ inactive to new data	150	–	–	ns
Register serial input data (pin DATA)					
t_{su}	input data to CLK set-up time	20	–	–	ns
t_h	input data to CLK hold time	20	–	–	ns

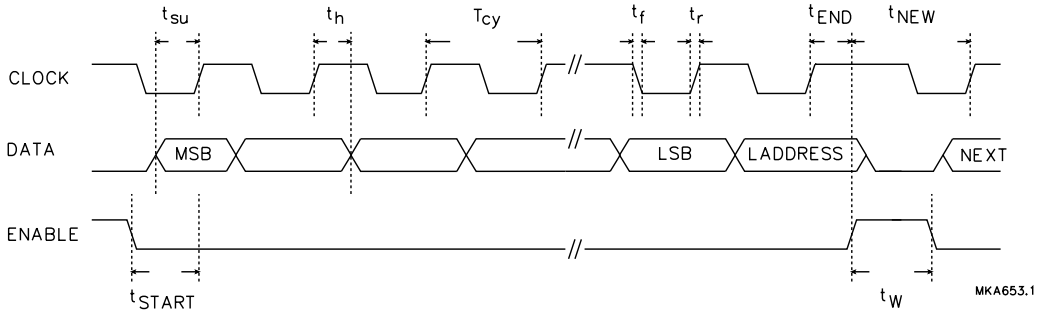

Fig.7 Serial bus timing diagram.

APPLICATION INFORMATION

Figure 8 illustrates the electrical diagram of the UAA2072M Philips demonstration board. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Component manufacturers

All surface mounted resistors and capacitors are manufactured by Philips Components. The small value capacitors are multi-layer ceramic with NPO dielectric.

The inductors are manufactured by Coilcraft UK.

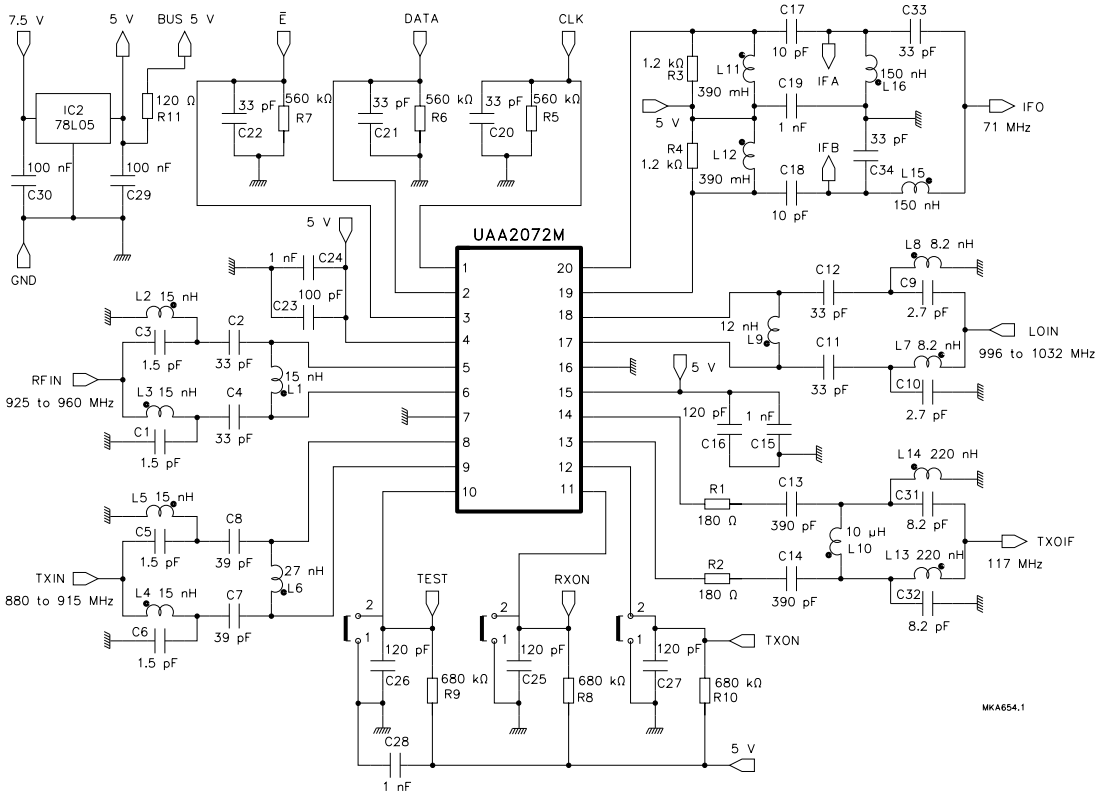

Fig.8 Application diagram.

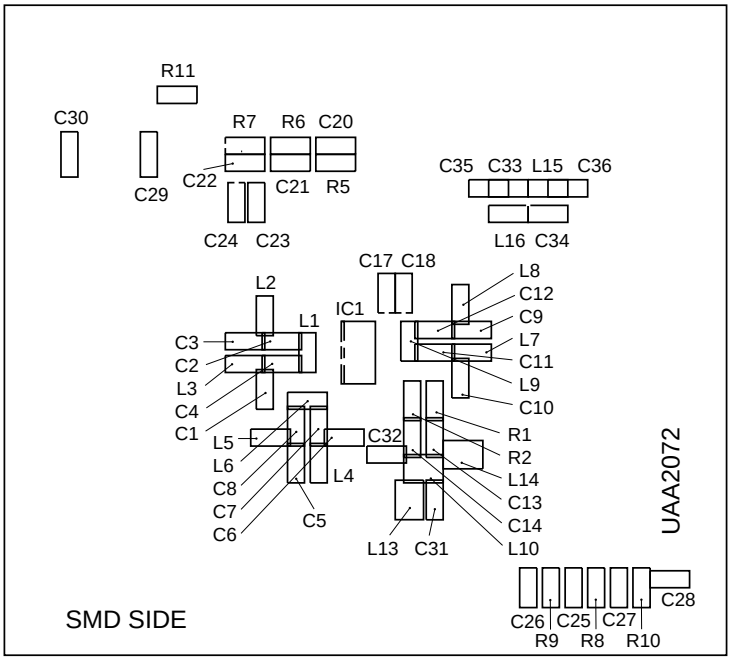

Fig.9 Printed-circuit board, SMD side.

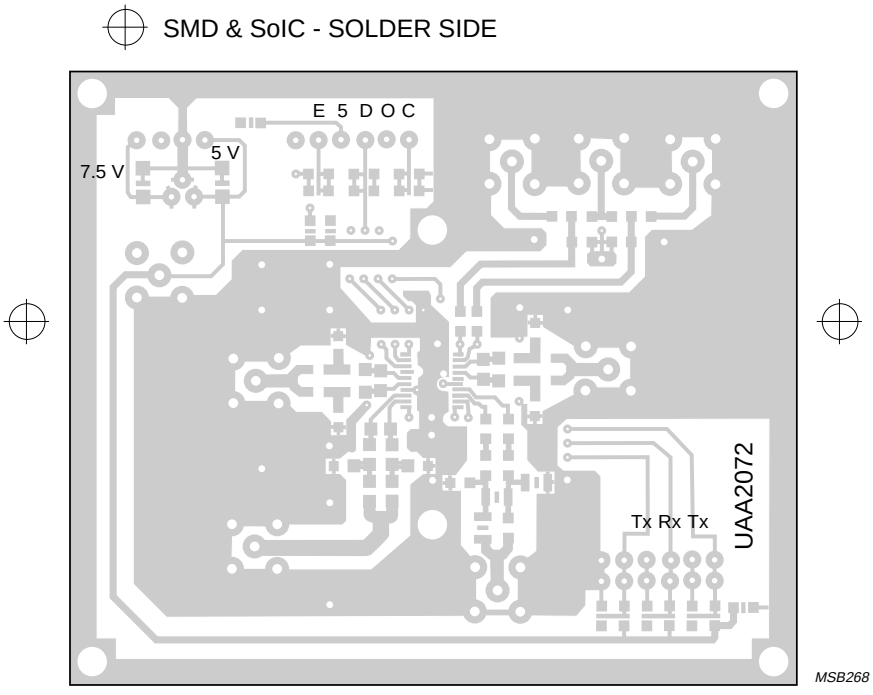

Fig.10 Printed-circuit board, SMD solder side.

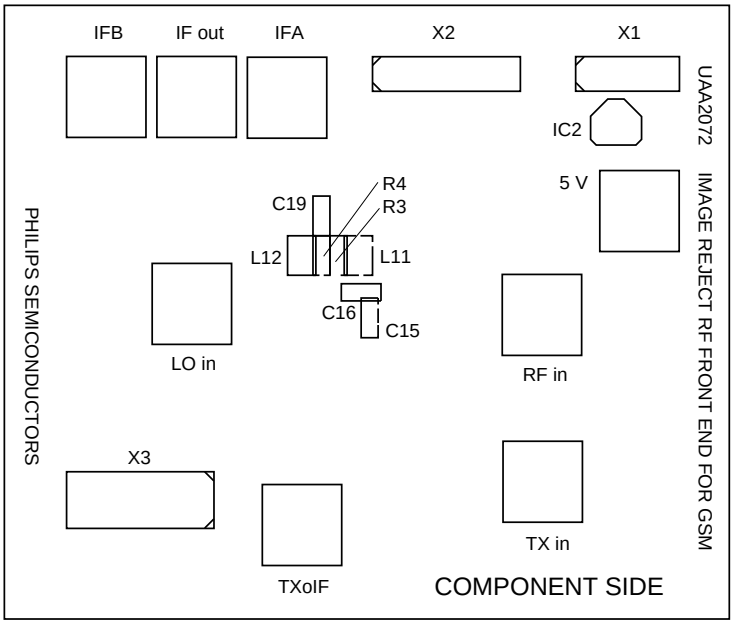

Fig.11 Printed-circuit board, component side for image reject RF front-end for GSM.

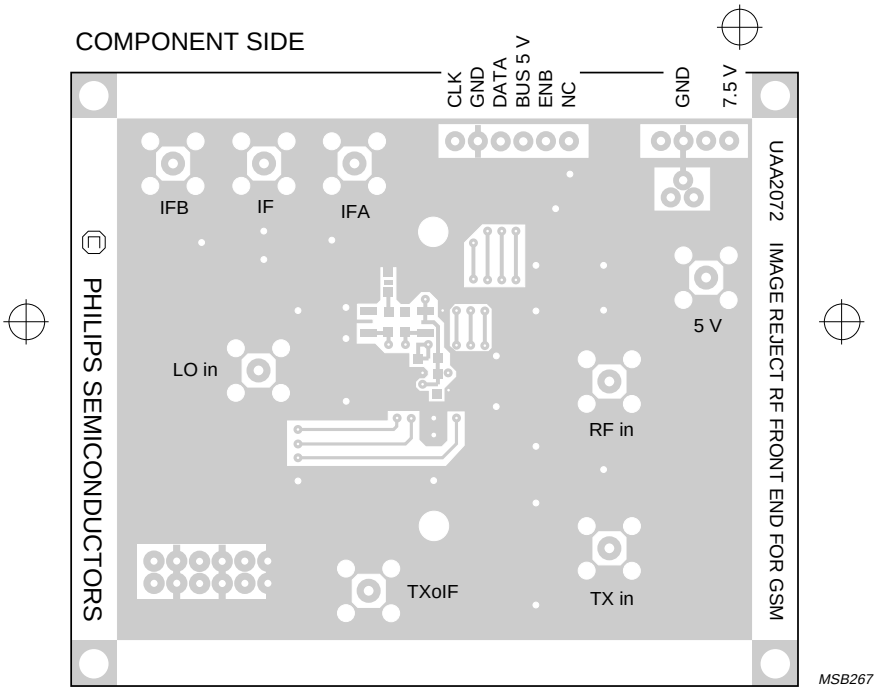

Fig.12 Printed-circuit board, component solder side for image reject RF front-end for GSM.

DEMONSTRATION BOARD - PARTS LIST

COMPONENT	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	1.2 kΩ	0805	IF
R4	1.2 kΩ	0805	IF
R5	560 kΩ	0805	CLK
R6	560 kΩ	0805	DATA
R7	560 kΩ	0805	$\overline{E}$
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	TEST
R10	680 kΩ	0805	TXON
R11	120 Ω	0805	5 V BUS
Capacitors			
C1	1.5 pF	0805	RFIN
C2	33 pF	0805	RFIN
C3	1.5 pF	0805	RFIN
C4	33 pF	0805	RFIN
C5	1.5 pF	0805	TXIN
C6	1.5 pF	0805	TXIN
C7	39 pF	0805	TXIN
C8	39 pF	0805	TXIN
C9	2.7 pF	0805	LOIN
C10	2.7 pF	0805	LOIN
C11	33 pF	0805	LOIN
C12	33 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	1 nF	0805	V_{CC2}
C16	120 pF	0805	V_{CC2}
C17	10 pF	0805	IFO
C18	10 pF	0805	IFO
C19	1 nF	0805	IF / 5 V
C20	33 pF	0805	CLK
C21	33 pF	0805	DATA
C22	33 pF	0805	$\overline{E}$
C23	100 pF	0805	V_{CC1}
C24	1 nF	0805	V_{CC1}
C25	120 pF	0805	RXON
C26	120 pF	0805	TEST

COMPONENT	VALUE	SIZE	LOCATION
Capacitors			
C27	120 pF	0805	TXON
C28	1 nF	0805	5 V
C29	100 nF	1206	5 V regulator
C30	100 nF	1206	5 V regulator
C31	8.2 pF	0805	TXOIF
C32	8.2 pF	0805	TXOIF
C33	33 pF	0805	IFO
C34	33 pF	0805	IFO
C35	link	0805	IF/NOT USED
C36	link	0805	IF/NOT USED
Inductors			
L1	15 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	8.2 nH	0805	LOIN
L8	8.2 nH	0805	LOIN
L9	12 nH	0805	LOIN
L10	10 μH	1008	TXOIF/OPTIONAL
L11	390 nH	1008	IFO
L12	390 nH	1008	IFO
L13	220 nH	1008	TXOIF
L14	220 nH	1008	TXOIF
L15	150 nH	0805	IFO
L16	150 nH	0805	IFO

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2072M
IC2	5 V regulator; type 78L05
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	5 V socket (optional, in place of IC2)
X1, X2 and X3	various 2.54 mm (0.1 inch) connectors