

## Modulator for GaAs power amplifiers

## UBA1710

### FEATURES

- Power MOS modulators for control of GaAs power amplifier drain voltage
- Power control loop amplifier and MOS driver
- Voltage tripler for supply of MOS driver
- Positive-to-negative DC converter for GaAs power amplifier gate biasing.

### APPLICATIONS

- Control of GaAs power amplifiers for GSM and DCS hand-held transceivers.

### GENERAL DESCRIPTION

The UBA1710 integrates the functions required to operate the GaAs Power Amplifiers (PAs) from the CGY20xx family which are intended for GSM and DCS applications.

It includes a negative supply for PA gate biasing and most of the functions required to implement power control so that only a very few external component are required.

The power control section integrates two power MOS devices for control of the PA drain voltages, an MOS driver and a feedback loop amplifier. The MOS driver is supplied from an on-chip voltage tripler.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER <sup>(1)</sup>	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	analog supply voltage	4.2	4.8	6.8	V
$V_{DD}$	digital supply voltage	4.2	4.8	6.8	V
$I_{CC} + I_{DD}$	peak supply current in power-up mode	–	10	–	mA
$T_{amb}$	operating ambient temperature	–20	–	+85	°C

### Note

1. For conditions, see Chapter “Characteristics”.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1710M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

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## BLOCK DIAGRAM

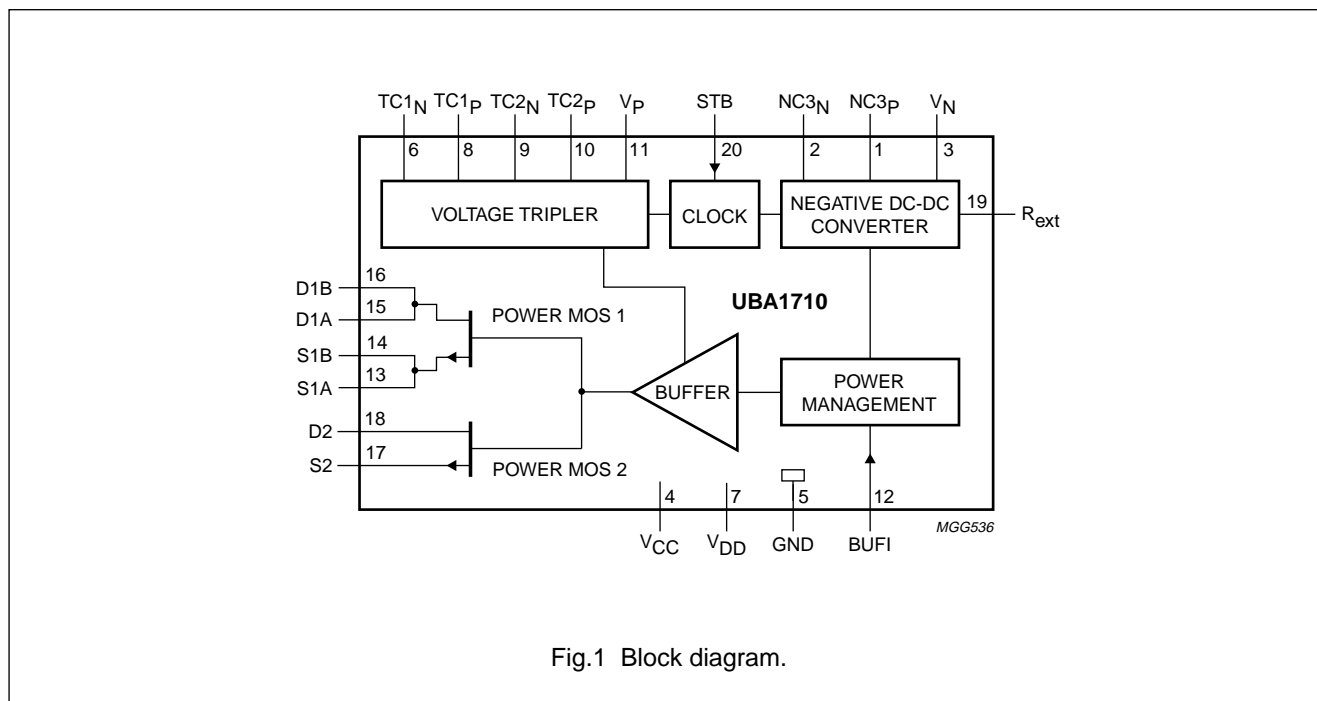


Fig.1 Block diagram.

## PINNING

SYMBOL	PIN	DESCRIPTION
NC3P	1	charge pump tank capacitor
NC3N	2	charge pump tank capacitor
V <sub>N</sub>	3	negative bias voltage
V <sub>CC</sub>	4	analog supply voltage
GND	5	ground
TC1N	6	charge pump tank capacitor
V <sub>DD</sub>	7	digital supply voltage
TC1P	8	charge pump tank capacitor
TC2N	9	charge pump tank capacitor
TC2P	10	charge pump tank capacitor
V <sub>P</sub>	11	positive tripler voltage
BUFI	12	buffer input
S1A	13	power MOS 1 source A
S1B	14	power MOS 1 source B
D1A	15	power MOS 1 drain A
D1B	16	power MOS 1 drain B
S2	17	power MOS 2 source
D2	18	power MOS 2 drain
R <sub>ext</sub>	19	external resistance for V <sub>N</sub>
STB	20	standby input (active HIGH)

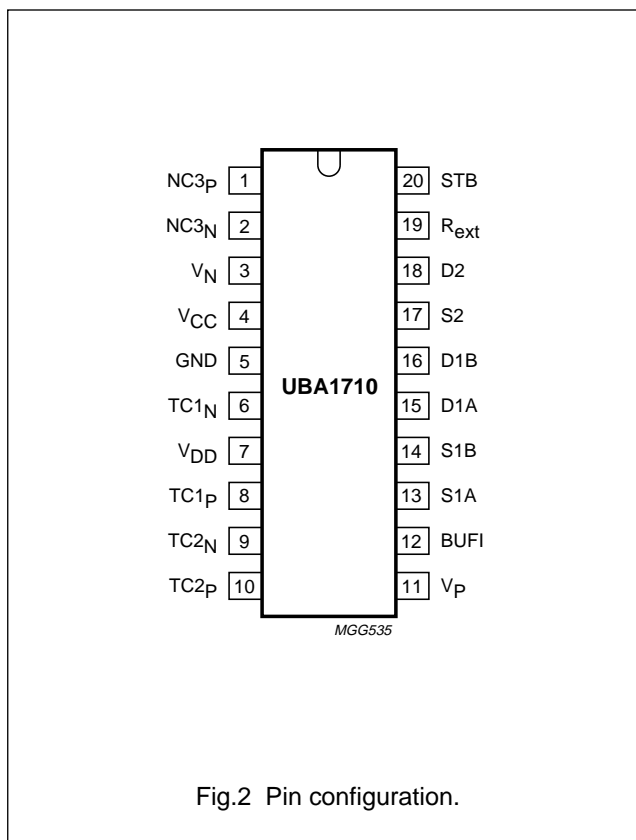


Fig.2 Pin configuration.

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**FUNCTIONAL DESCRIPTION****Power control section**

Power control for GaAs PAs from the CGY20xx family is achieved by varying the drain voltage. This is achieved with the UBA1710 by means of the two power MOS devices integrated on-chip. They enable separate control of the PA output stage from the pre-amplifier stages. They have a very low 'on' resistance for low drop voltage at high RF output power.

The MOS devices are driven by a buffer. The buffer amplifier, in association with power MOS, is included in a feedback loop to exhibit a high cut-off frequency (3 MHz) over the whole control dynamic range. This buffer allows fast switching of the MOS in accordance with GSM power ramping requirements.

**DC-DC converters**

One DC-DC converter is required to provide negative gate biasing to the GaAs PA.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>CC</sub>	analog supply voltage	-0.5	+9.0	V
V <sub>DD</sub>	digital supply voltage	-0.5	+9.0	V
V <sub>I</sub>	DC input voltage on all pins (except BUFI)	-0.5	+9.0	V
I <sub>I</sub>	DC current into any signal pin	-10	+10	mA
P <sub>tot</sub>	total power dissipation	-	0.65	W
T <sub>stg</sub>	storage temperature	-65	+150	°C
T <sub>amb</sub>	operating ambient temperature	-20	+85	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	100	K/W

The standard value is typically -2 V, without any external resistor connected. The other one is a voltage tripler and is required to supply the MOS driver. The driver is required to raise the MOS gate voltage well above the battery voltage in order to open the MOS switches ('high side' driver).

These DC-DC converters are operated at a typical frequency of 600 kHz supplied by an internal oscillator. Five external capacitors with a typical value of 0.1 μF (0603 SMD) are required to operate these converters.

**Power management**

The power management disables the PA drain voltage and prevents the PA from burnout if drain voltage is supplied before the negative gate voltage is available.

**Standby mode**

An additional feature includes a standby mode, reducing the current consumption to typically 2 μA.

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**CHARACTERISTICS** $V_{CC} = V_{DD} = 4.8 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{CC}$	analog supply voltage		4.2	4.8	6.8	V
$V_{DD}$	digital supply voltage		4.2	4.8	6.8	V
$I_{CC} + I_{DD}$	peak supply current	power-up mode; PA on	–	10	tbf	mA
		power-down mode; PA off	–	6	tbf	mA
$I_{stb}$	standby current	standby mode	–	2	tbf	$\mu\text{A}$
<b>Power MOS 1</b>						
$R_{DSon1}$	on resistance	$I_{DS} = 1.5 \text{ A}$	–	0.2	tbf	$\Omega$
<b>Power MOS 2</b>						
$R_{DSon2}$	on resistance	$I_{DS} = 0.5 \text{ A}$	–	0.6	tbf	$\Omega$
<b>Clock circuit</b>						
$f_{clk}$	clock frequency		–	600	–	kHz
<b>Voltage tripler</b>						
$V_{Po}$	output voltage	with $I_{Po} = 2 \text{ mA}$	11.5	11.8	12.1	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{Po} = 2 \text{ mA}$ ; $C1 = C2 = 100 \text{ nF}$ ; $C_P = 100 \text{ nF}$	–	2	–	mV
$t_{on}$	turn-on time		–	100	tbf	$\mu\text{s}$
<b>Negative DC/DC converter</b>						
$V_{No}$	output voltage	with $I_{No} = 250 \text{ } \mu\text{A}$ ; $R_{ext} = 470 \text{ k}\Omega$	–1.6	–1.8	–2.0	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{No} = 250 \text{ } \mu\text{A}$ ; $C3 = 100 \text{ nF}$ ; $C_N = 100 \text{ nF}$	–	2	tbf	mV
$t_{on}$	turn-on time		–	280	tbf	$\mu\text{s}$
<b>MOS buffer amplifier</b>						
$V_i$	input voltage		1.2	–	3.2	V
$t_{sw}$	switching time from 0 to 4.5 V	2 $\Omega$ load at MOS outputs	–	1	–	$\mu\text{s}$

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APPLICATION INFORMATION

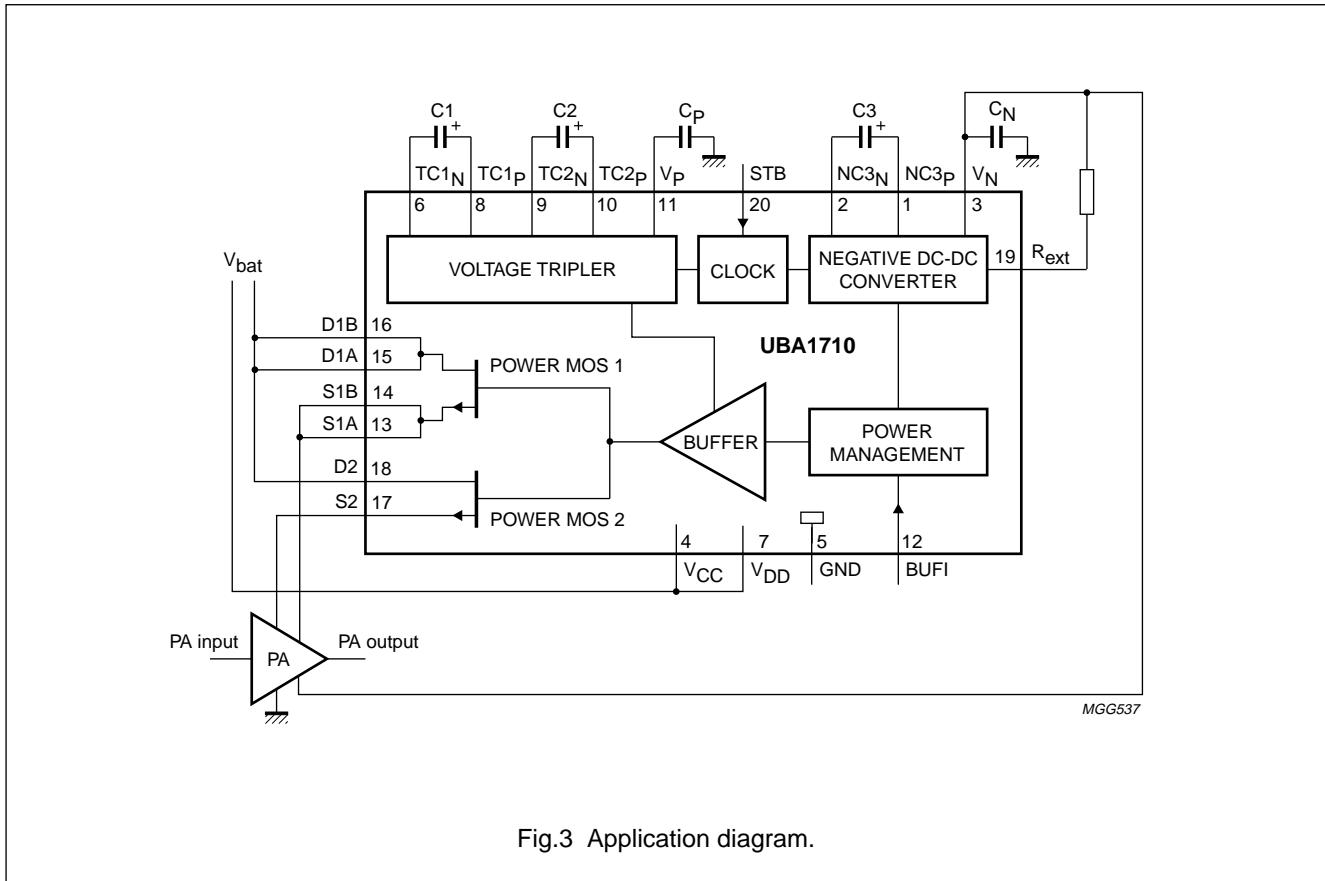


Fig.3 Application diagram.