# Data processor for cellular radio (DPROC2)

# UMA1002

## BLOCK DIAGRAM

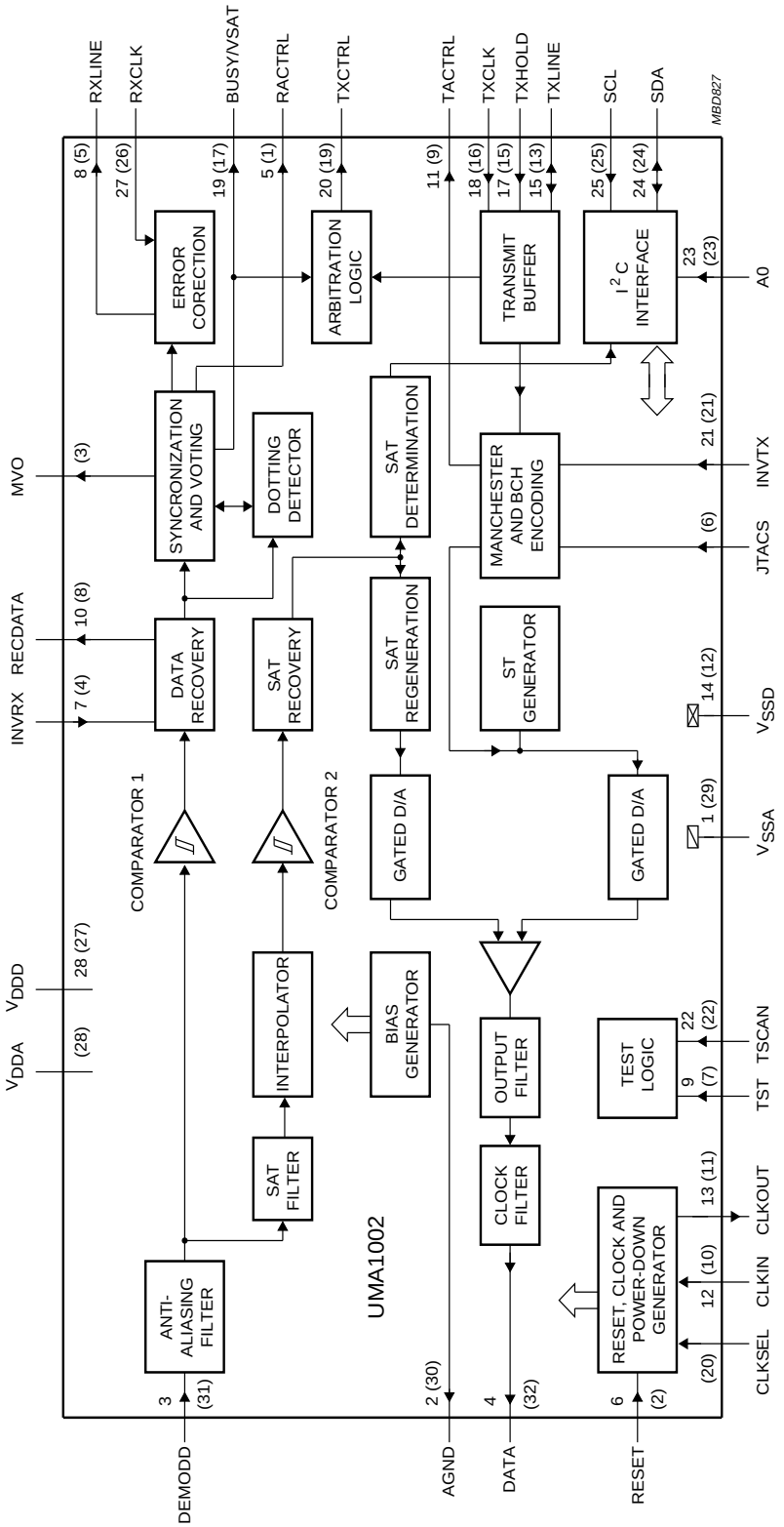



Fig.1 Block diagram.

Pins in parenthesis apply to UMA1002H in LQFP32.

PINNING

| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | SO28 | LQFP32 | |
| $V_{SSA}$ | 1 | 29 | Negative analog supply (0 V). To be connected low-ohmic to $V_{SSD}$. |
| AGND | 2 | 30 | Internally generated analog signal ground. Voltage level = $\frac{1}{2}V_{DDA}$. This pin should be connected to a blocking capacitor, no DC load allowed. |
| DEMODD | 3 | 31 | DEMODD inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC-coupled. See chapter ÒAC characteristicsÓ. |
| DATA | 4 | 32 | Data is an analog output which provides the Manchester encoded and filtered data signal, SAT and signalling tone. This signal should normally be AC-coupled into the Audio/Data summer. See chapter ÒAC characteristicsÓ. |
| RACTRL | 5 | 1 | Received audio control output. Open-drain output used to blank the audio path to the earpiece when a sequence of dotting followed by a synchronization word or 2 synchronization words separated by 77 bits is detected. RACTRL and TACTRL functions can be combined using one line. Output level LOW means audio muted. |
| RESET | 6 | 2 | Master reset input resetting all internal ßip-ßops to the speciÞed state. This input has no inßuence on analog parts, but must be controlled by an active HIGH microcontroller port. |
| INVRX | 7 | 4 | This input inverts the sense of received data stream, which allows RF demodulators with high or low local oscillators to be used. The AMPS and TACS speciÞcations deÞne NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC2 depends on the receiver local oscillator. Input LOW means data normal. |
| RXLINE | 8 | 5 | Received data signal output to the system controller. Maximum data rate is 100 kbits/s. |
| TST | 9 | 7 | Test input pin (note 1). |
| RECDATA | 10 | 8 | Output of the recovered digital data signal (note 1). |
| TACTRL | 11 | 9 | Transmitter audio control output. This open-drain output is used to blank the audio path and enable the data path to the modulator during data bursts on the RVC. Output level LOW means audio muted. |
| CLKIN | 12 | 10 | 1.2 MHz or 9.6 MHz external master clock input. This input signal should be accurate to $100 \times 10^{-6}$ and have a worst case 60 : 40 mark-space ratio. |
| CLKOUT | 13 | 11 | Output of 1.2 MHz clock signal (for APROC) derived from CLKIN. |
| $V_{SSD}$ | 14 | 12 | Negative digital supply (0 V), internally connected to substrate. To be connected low-ohmic to $V_{SSA}$. |
| TXLINE | 15 | 13 | Open-drain bi-directional data line to the system controller (internal 100 kW pull-up). Maximum data rate is 100 kbits/s. |
| n.c. | 16 | 14 | Not connected. |
| TXHOLD | 17 | 15 | This input holds off transmission of data when set to HIGH. |
| TXCLK | 18 | 16 | Transmitted data clock input from the system controller. |
| BUSY/VSAT | 19 | 17 | Output indicating the status of the RECC by providing output information based on a majority decision on the last 3 consecutive Busy/Idle bits (FVC = logic 0). Output level LOW means channel idle.<br>Indicating the result of the comparison of the measured SAT and the expected SAT colour-code bits ($I^2C$-bus register) in the voice channel mode (FVC = logic 1 and ENSM = logic 1). Output level LOW means incoming SAT not equal to expected SAT. |

| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | SO28 | LQFP32 | |
| TXCTRL | 20 | 19 | Transmitter control open-drain output used to disable the transmitter during an RECC access failure. Output level LOW means RF disabled. |
| INVTX | 21 | 21 | This input inverts the sense of transmitted data stream, which allows RF modulators with high or low local oscillators to be used. The AMPS and TACS speciÞcations deÞne NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator. Input LOW means data inverted. |
| TSCAN | 22 | 22 | Test switch input, only enabled if TST = logic 1, but should have a deÞned state. |
| A0 | 23 | 23 | Input to select the least signiÞcant bit of the I²C-bus address. |
| SDA | 24 | 24 | Serial data input/output ($I^2C$-bus). |
| SCL | 25 | 25 | Serial clock input ($I^2C$-bus). |
| n.c. | 26 | 18 | Not connected. |
| RXCLK | 27 | 26 | Received data clock input from the system controller. |
| $V_{DDD}$ | 28 | 27 | Digital supply voltage (+3 V). |
| $V_{DDA}$ | - | 28 | Analog supply voltage (+3 V). |
| MVO | - | 3 | Majority voting output indicating that on FOCC the Þrst 3 received words do not differ from each other and thus the majority decision over 5 words can already be carried out. Because of the required speed, indication is at this pin (and not via the $I^2C$-bus) which can be monitored by the system controller. Output LOW means the receiver can be switched off. |
| JTACS | - | 6 | Digital input signal for JTACS, input HIGH means that data is routed from TXLINE directly without processing to gated DAC (if enabled by STEN bit). |
| CLKSEL | - | 20 | Input switch for internal divide-by-8 or divide-by-1 divider between CLKIN and CLKOUT (internal pull-down ®  divide-by-1 is default if not bonded out in SO28 package). |

Note

1. Must not be connected in existing applications.

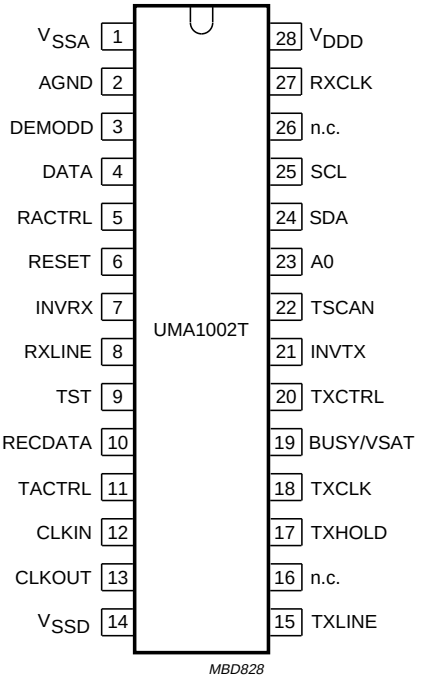



Fig.2 Pin configuration for SO28, SOT136-1.

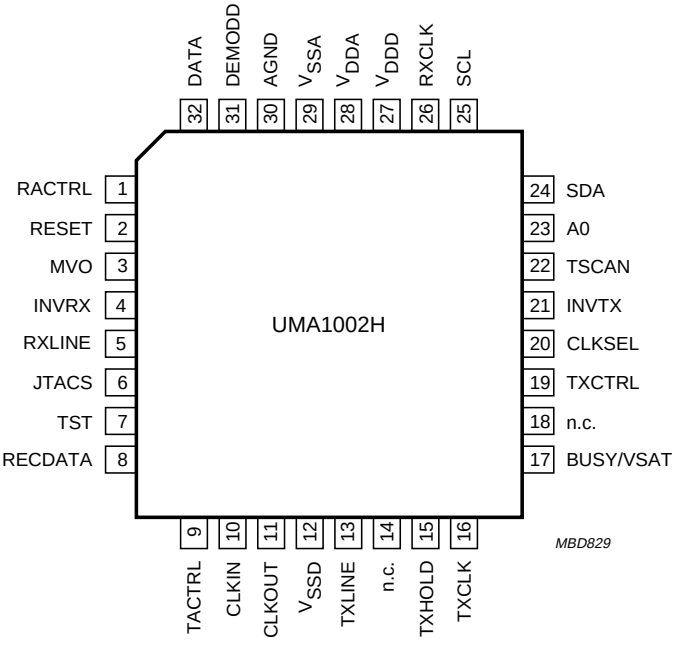



Fig.3 Pin configuration for LQFP32, SOT358-1.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | - 0.5 | 6.5 | V |
| $I_{DD}$ | supply current | | - | 50 | mA |
| $I_I$ | DC input current (any input) | | - | ± 10 | mA |
| $I_O$ | DC output current (any output) | | - | ± 10 | mA |
| $V_I$ | input voltages (all inputs) | $V_{DD(max)}$ = 6.0 V | - 0.5 | $V_{DD}$ + 0.5 | V |
| $P_{tot}$ | total power dissipation | | - | 300 | mW |
| $P_o$ | power dissipation per output | | - | 10 | mW |
| $T_{amb}$ | operating ambient temperature | | - 30 | +70 | °C |
| $T_{stg}$ | storage temperature | | - 65 | +150 | °C |

DC CHARACTERISTICS

$V_{DD}$ = 3 V ($V_{DDA}$ and $V_{DDD}$ externally connected); $T_{amb}$ = - 30 to +70 °C; $f_{CLKIN}$ = 1.2 MHz (if CLKSEL = logic 0); unless otherwise speciÞed.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Supply | | | | | | |
| $V_{DD}$ | supply voltage | | 2.7 | 3.0 | 5.5 | V |
| $I_{DD}$ | operating supply current at pins $V_{DDD}$ and $V_{DDA}$ | in FVC | - | 1.3 | 1.8 | mA |
| | | in FOCC | - | 0.4 | - | mA |
| Digital inputs: INVRX, INVTX, CLKSEL, TXHOLD, TXCLK, A0, RESET, RXCLK, TST, TSCAN, CLKIN and JTACS | | | | | | |
| $V_{IL}$ | LOW level input voltage | | - 0.3 | - | $0.2V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | $0.8V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| $I_{LI}$ | LOW/HIGH level input leakage current | pins without pull-down | - | - | 1 | mA |
| $R_{pdCLKSEL}$ | CLKSEL internal pull-down resistance | | - | 200 | - | kW |
| $R_{pdJTACS}$ | JTACS internal pull-down resistance | | - | 200 | - | kW |
| $R_{pdTST}$ | TST internal pull-down resistance | | - | 200 | - | kW |
| Digital push-pull outputs: RXLINE, BUSY/VSAT, RECDATA, MVO and CLKOUT | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{sink}$ = 1 mA | - | - | 0.4 | V |
| $V_{OH}$ | HIGH level output voltage | $I_{source}$ = - 1 mA | $V_{DD}$ - 0.4 | - | - | V |
| Open-drain n-channel outputs: TXCTRL, TACTRL and RACTRL | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{sink}$ = 2 mA | - | - | 0.4 | V |
| Open-drain n-channel input/output: TXLINE | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_{sink}$ = 2 mA | - | - | 0.4 | V |
| $V_{IL}$ | LOW level input voltage | | - 0.3 | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | $0.7V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| $R_{puTXLINE}$ | internal pull-up resistance | | - | 100 | - | kW |
| $I^2C$-bus pins: SCL and SDA | | | | | | |
| $t_{data}$ | data conversion rate | | - | - | 100 | kbits/s |
| Analog reference pin: AGND | | | | | | |
| $V_{AGND}$ | DC voltage level | for $V_{DD}$ = 2.7 to 5.5 V | - | $0.5V_{DD}$ | - | V |

AC CHARACTERISTICS

$V_{DD}$ = 3 V ($V_{DDA}$ and $V_{DDD}$ externally connected); $T_{amb}$ = - 30 to +70 °C; $f_{CLKIN}$ = 1.2 MHz (if CLKSEL = logic 0); unless otherwise speciÞed.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Data rate of data transfer link: RXCLK, RXLINE, TXCLK, TXLINE | | | | | | |
| $t_{data}$ | data conversion rate | | - | - | 500 | kbit/s |
| Clock input: CLKIN (CLKSEL = logic 0) | | | | | | |
| $C_i$ | input capacitance | | - | 5 | - | pF |
| $T_{CLKIN}$ | clock input period time | | 833.25 | 833.33 | 833.42 | ns |
| $t_{CLKINH}$ | clock input HIGH time | | 40 | 50 | 60 | $\%T_{CLKIN}$ |
| $t_r$ | clock input rise time | | - | 50 | - | ns |
| $t_f$ | clock input fall time | | - | 50 | - | ns |
| Clock input: CLKIN (CLKSEL = logic 1) | | | | | | |
| $T_{CLKIN}$ | clock input period time | | - | 104.17 | - | ns |
| $t_{CLKINH}$ | clock input HIGH time | | 40 | 50 | 60 | $\%T_{CLKIN}$ |
| $t_r$ | clock input rise time | | - | 5 | - | ns |
| $t_f$ | clock input fall time | | - | 5 | - | ns |
| Analog output: DATA | | | | | | |
| $V_{DATA}$ | DC output voltage level | | - | $V_{AGND}$ | - | V |
| $V_{o(p-p)}$ | output voltage level for signalling tone (peak-to-peak value) | $V_{DD}$ = 3 V; note 1 | 1.14 | 1.2 | 1.26 | V |
| | | $V_{DD}$ = 5 V; note 1 | 1.9 | 2.0 | 2.1 | V |
| THD | total harmonic distortion for Supervisory Audio Tone (SAT) | | - | - | 10 | % |
| $R_L$ | allowed load resistance to AC ground | | 10 | - | - | kW |
| $C_L$ | allowed load capacitance to AC ground | | - | - | 100 | pF |
| Analog input: DEMODD | | | | | | |
| $V_{DEMODD}$ | DC input voltage level | 100 kWresistor external to AGND | - | $V_{AGND}$ | - | V |
| $V_{i(p-p)}$ | data input voltage level (peak-to-peak value) | input via a 10 nF capacitor | 200 | 250 | 600 | mV |
| $V_{i(p-p)}$ | SAT input voltage level (peak-to-peak value) | | 50 | - | - | mV |
| $Z_i$ | input impedance | | 1 | - | - | MW |

Note

1. Plus supply voltage variation ($DV_{DD}$), $R_L$ = 10 kW.

## FUNCTIONAL DESCRIPTION

### General

The UMA1002 (DPROC2) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation.

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.4.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz) is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the ÔloopÕ. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand-held portable cellular set are:

- Small physical size
- Minimum number of interconnections (serial bus)
- Low power consumption
- Low cost.

The DPROC2 is a member of our Cellular Radio chip set, based on the $I^2C$-bus, which meets these requirements.

A cellular radio system schematic using the chip set is shown in Fig.11.

### DPROC2 power-saving features

To support current saving in the application DPROC2 has three different modes of circuit operation implemented. They are decoded by the $I^2C$-bus register bit FVC and by activity on the data transfer link (TXCLK and TXLINE). In power-down mode the relevant digital circuits have the clock disabled, the analog circuits have the bias currents and the switched capacitor clock switched off.

- Normal mode: all circuit parts are operating (e.g. on Voice channels)
- Power-down mode 1: the SAT path is in power-down (e.g. during access of the RECC)
- Power-down mode 2: the SAT path and the total data transmit path are in power-down (e.g. for Idle state, DPROC2 operating only on FOCC).

### System power-saving features

Besides the above mentioned power-down modes DPROC2 also includes features to reduce system current (e.g. switching off parts of the receiver, and put the system controller into Idle mode for longer periods of time).
All these features are controlled by the $I^2C$-bus. For further explanation of the following features refer to the Section $I^2C$-bus registers.

#### MAJORITY VOTING (ONLY IN LQFP32)

Majority voting includes more intelligence. This feature is enabled in FOCC with $I^2C$-bus bit MAJ = logic 1.
If 3 consecutive identical words have been received it is signalled via pin MVO. Therefore during the last 2 frame words the receiver could be switched off to save system current consumption.

#### CONTROL FILLER WORDS FILTER

System current can be further reduced by an on-chip control filler words filter in FOCC, which enables the detection of consecutive identical control filler words.
If consecutive control filler words are identical (i.e. DCC, CMAC and WFOM) they will not be passed on to the microcontroller. Consequently the system controller can remain in power-saving mode.

### Programming of ESCC bits

There is a possibility to program the expected ESCC bits, so that DPROC2 can compare expected and received SAT and signal any inconsistency to the system controller via BUSY/VSAT pin. Consequently there is no need to read the measured SAT periodically via the $I^2C$-bus.

### BCH error filter

If this feature is enabled, DPROC2 will not pass on to the microcontroller words with BCH errors. Consequently the microcontroller can remain in power-saving mode. This feature in combination with the control filler feature is defined in Table 8.

### Selectable clock divider (only in LQFP32)

An on-chip selectable divide-by-8 clock divider reduces external peripheral component count.

### Power-up state and master reset (RESET)

RESET should be HIGH as soon as power supply is available.

DPROC2 will not respond reliably to any inputs (including RESET) until 100 ms after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No on-chip power-on reset is provided, therefore before the device can enter normal operation RESET must be held HIGH.

RESET is an active HIGH master reset input, with a minimum active pulse width of 4 ms which may be used to reset the total logic within DPROC2 to a predefined state as illustrated in Tables 1 and 2. It is preferably only used during power-up, during normal operation it is recommended to use the fully synchronous reset signals derived from the $I^2C$-bus bits FVC, STS and TXRST (see Table 4). To ensure correct operation TXCLK must be held HIGH during RESET operation.

Table 1 Predefined state of the digital output pins

| OUTPUT | STATE |
|---|---|
| RXLINE | HIGH |
| TXCTRL | high-impedance (HIGH) |
| TACTRL | high-impedance (HIGH) |
| RACTRL | high-impedance (HIGH) |
| BUSY/VSAT | HIGH |
| TXLINE | HIGH (by 100 kΩ internal pull-up resistor) |
| RECDATA | LOW |
| MVO | HIGH |
| SDA | high-impedance (HIGH) |

Table 2 Predefined state of the $I^2C$-bus registers

| REGISTER | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Status (read) | LOW | LOW | LOW | HIGH | LOW | LOW | HIGH | HIGH |
| Control 1 (write) | LOW | LOW | LOW | LOW | LOW | LOW | LOW | LOW |
| Control 2 (write) | LOW | LOW | LOW | LOW | LOW | LOW | LOW | LOW |

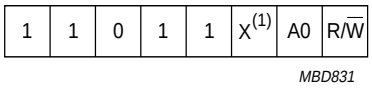
I²C-bus serial data link (SDA; SCL)

SDA is the bi-directional data line, SCL is the clock input from an I²C-bus master. These constitute a typical I²C link and conform to standard I²C-bus characteristics.
A detailed description of the I²C-bus specification, with applications, is given in the brochure *ÒThe I²C-bus and how to use itÓ*. This brochure may be ordered using the code 9398 393 40011.

· Data rate up to 100 kbits/s.

SLAVE ADDRESS SELECT (A0)

Selection of the device slave address is achieved by connecting A0 to either $V_{SS}$ or $V_{DDD}$. The slave address is defined in accordance with the I²C-bus specifications as shown in Fig.4




MBD831

(1) X = donÕt care.

Fig.4 Device slave address.

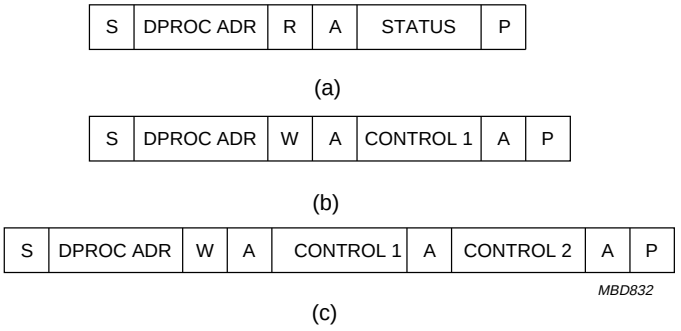
## I²C-BUS REGISTERS

The I²C-bus register block resides internally within the I²C-bus interface block and contains various items of status and control information which are transferred to and from DPROC2 via the I²C-bus. The block is organized into three 8-bit registers:

- Status register which contains read only items
- Control registers 1 and 2 which contain write only items

Table 3 I²C-bus register map

| REGISTER | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Status (read) | - | - | WSYNC | BUSY | TXABRT | TXIP | MSCC1 | MSCC0 |
| Control 1 (write) | BUFEN | SERV | STS | TXRST | ABREN | FVC | STEN | SATEN |
| Control 2 (write) | MAJ | MR1 | MR0 | DBCH | DCFM | ENSM | ESCC1 | ESCC0 |




(a) Read from DPROC2 status register.

(b) Write to DPROC2 control register 1.

(c) Write to all DPROC2 control registers.

Where:
S = START condition
W = read/write bit (logic 0 = write)
R = read/write bit (logic 1 = read)
A = acknowledge bit
P = STOP condition
DPROC ADR = slave address of DPROC2.

Fig.5 I²C-bus data format.

Table 4 Description of $I^2C$-bus register map

| REGISTER BITS | LOGIC LEVEL | DESCRIPTION |
|---|---|---|
| Control Register 1 | | |
| BUFEN | 0 | 1.2 MHz signal not available at pin CLKOUT |
| | 1 | 1.2 MHz signal is available at pin CLKOUT |
| SERV | 0 | serving system data stream B selected |
| | 1 | serving system data stream A selected |
| STS(1) | 0 | TACS selected |
| | 1 | AMPS selected |
| TXRST | 1 | terminates a message being transmitted on the reverse channel; monostable signal causing a reset of the message transmission circuitry and resets the $I^2C$-bus bits TXABRT, TXIP and clears the transmit buffer |
| ABREN | 1 | DPROC2 has permission to abort data transmission and disable RF on the RECC following the detection of a channel access attempt collision |
| | 0 | no permission for above operations |
| FVC(2) | 0 | control channel format selected |
| | 1 | voice channel format selected |
| STEN | 0 | disables output of signalling tone to pin DATA |
| | 1 | enables output of signalling tone to pin DATA if FVC = logic 1 |
| SATEN | 0 | disables output of SAT transponded signal to pin DATA |
| | 1 | enables output of SAT transponded signal to pin DATA if FVC = logic 1 |
| Control Register 2 | | |
| MAJ | 0 | majority voting procedure on FOCC using all 5 frame words, MVO output is always HIGH |
| | 1 | majority voting procedure on FOCC using the Þrst 3 frame words, if they are all identical the MVO pin goes LOW (see Fig.6) |
| MR0, MR1 | see Table 5 | determines set-up time of MVO signal with respect to beginning of the next dotting (see Fig.6) |
| DBCH | see Table 8 | BCH error Þlter |
| DCFM | see Table 8 | control Þller message Þlter |
| ENSM | 0 | enable SAT monitoring; ESCC bits are not used |
| | 1 | enable SAT monitoring; ESCC bits are used for following function |
| ESCC0, ESCC1 | see Table 6 | expected SAT colour code bits; the incoming SAT is compared to these bits, the result (expected or not expected SAT frequency) is given out by the BUSY/VSAT pin (when FVC = logic 1), which prevents periodical reading from the $I^2C$-bus status register |

| REGISTER BITS | LOGIC LEVEL | DESCRIPTION |
|---|---|---|
| Status Register | | |
| WSYNC | 0 | DPROC2 has not acquired frame synchronization in accordance with FOCC format |
| | 1 | DPROC2 has acquired frame synchronization in accordance with FOCC format |
| BUSY | | indicates the status of RECC, determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits of the FOCC and is also routed to pin BUSY/VSAT |
| | 0 | channel idle |
| | 1 | channel busy |
| | | indicates the result of the comparison of the incoming SAT and the stored SAT Colour Code bits in the Voice Channel mode and is also routed to pin BUSY/VSAT |
| | 0 | incoming SAT not equal to expected SAT |
| | 1 | incoming SAT equal to expected SAT |
| TXABRT | | indicates that a RECC access attempt has been aborted without successful message transmission |
| | 0 | no access collision detected |
| | 1 | transmission attempt aborted |
| TXIP | 0 | no transmission on RECC or RVC in progress |
| | 1 | data transmission by DPROC2 on RECC or RVC in progress |
| MSCC1, MSCC0 | see Table 7 | provides information about the current measured SAT colour code |

Notes

1. Changing this register bit resets internally the receive and transmit logic circuitry.
2. Changing this register bit resets internally the receive logic circuitry.

Table 5 Set-up time of MVO signal

| MR0 | MR1 | $t_{MVO}$ (ms) |
|---|---|---|
| 0 | 0 | 3 |
| 0 | 1 | 6 |
| 1 | 0 | 9 |
| 1 | 1 | 12 |

Table 6 Expected SAT colour code

| ESCC1 | ESCC0 | SAT FREQUENCY (Hz) |
|---|---|---|
| 0 | 0 | 5970 |
| 0 | 1 | 6000 |
| 1 | 0 | 6030 |
| 1 | 1 | no valid SAT |

Table 7 Measured SAT colour code

| MSCC1 | MSCC0 | SAT FREQUENCY (Hz) |
|---|---|---|
| 0 | 0 | 5970 |
| 0 | 1 | 6000 |
| 1 | 0 | 6030 |
| 1 | 1 | no valid SAT |

**Table 8** Conditions for transmission of received words to system controller

| DBCH | DCFM | BCH ERROR BIT | CHANGE IN CONTROL FILLER WORD DETECTED | TRANSMISSION OF CONTROL FILLER WORD TO SYSTEM CONTROLLER |
|---|---|---|---|---|
| 0 | 0 | x | x | yes |
| 0 | 1 | 0 | 0 | no |
| 0 | 1 | 0 | 1 | yes |
| 0 | 1 | 1 | x | yes |
| 1 | 0 | 0 | x | yes |
| 1 | 0 | 1 | x | no |
| 1 | 1 | 0 | 0 | no |
| 1 | 1 | 0 | 1 | yes |
| 1 | 1 | 1 | x | no |

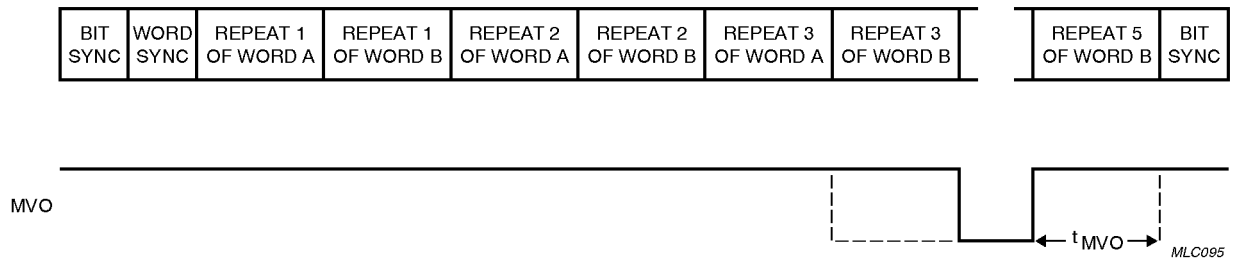



Fig.6 Timing of MVO output.

## Digital circuit blocks

### GENERAL

The majority of the digital circuitry within the DPROC2 device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig.1.

### DATA RECOVERY

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Comparator Block, on which it performs the following functions:

- Clock recovery
- Manchester decoding
- Data regeneration.

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a logic 1 otherwise it is latched as a logic 0.

### SAT RECOVERY

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.

The recovery is performed using a digital phase-locked loop.

### SAT DETERMINATION

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the $I^2C$ status registers MSCC0 and MSCC1.

### SAT REGENERATION

The SAT Regeneration Block generates a digital SAT stream for transponding back to the base station. The transponded SAT is phase-locked to the recovered SAT by means of a second digital phase-locked-loop. To minimize the total harmonic distortion of the output signal the transponded SAT is then processed by a delta modulator before being passed on to the Gated Digital-to-Analog converter.

### DOTTING DETECTOR

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

### WORD SYNCHRONIZATION DETECTOR

The Word Synchronization Block performs the following functions:

- Frame Synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination.

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC2 has achieved frame synchronization.

In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode.

Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

FVC: After detection of 2 consecutive sync words the circuit leaves its Search Mode and enters the Lock Mode. The data word in between is considered as valid and already stored for Majority Voting. Whenever a sync word was found the incoming data stream is examined 88 bits later for sync again. Whenever a valid sync word is detected the following data word is given to the Majority Voting block. After missing two consecutive sync words the circuit goes back to the search mode (scanning for sync every bit). If a sync word is then detected again, the following data word is immediately accepted (and not only after two correctly timed sync words). The detection process of sync words is independent of the detection of dotting. The audio mute via pin RACTRL is activated either by receiving a sync word after detection of a dotting sequence or by entering Lock Mode.

### MAJORITY VOTING BLOCK

The Majority Voting Block performs the following functions:

- Identifying position and validity of frames in the received data stream
- Extracting five repeats of each word from a valid frame
- Performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC2 is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC2. On the Forward Voice Channel the extraction of a data word for majority voting is described in the Section “Word Synchronization Detector”.

DPROC2 enables two mechanisms for Majority Voting. The first is based on 5 words and is described above. The other mechanism is based on 3 consecutive identical words and thus enabling switch-off of parts of the receiver during reception of the remaining two words (see Table 5 and Fig.6).

### ERROR CORRECTION BLOCK

The Error Correction Block performs the following functions:

- Extraction of a valid message from the Majority-Voted Word
- Computation of the S1 and S3 syndromes
- Correction of up to one error in the word
- Communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$1 + X + X^6$ and $1 + X + X^2 + X^4 + X^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC2 only corrects up to one error although the code used has a Hamming distance of five. The occurrence of

two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

### RECEIVED DATA SERIAL LINK

The Received Data Serial Link transfers data and control information from DPROC2 to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC2 output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC2 will reset the receive buffer for the next word after the period RWIN (see Fig.8).

#### *Data format*

Each Received Data word consists of 4 bytes. The word format is shown in Fig.7(a). The sense and function of the fields is shown in Table 9.

#### *Link protocol*

The Received Data protocol is described by the timing diagram Fig.8(a) and has the following parameters:

- Maximum receive window (RWIN)
  - Control Channel (TACS) = 47 ms MAJ = 0
  - Control Channel (TACS) = 30.5 ms MAJ = 1 (in FOCC only)
  - Control Channel (AMPS) = 37 ms MAJ = 0
  - Control Channel (AMPS) = 23.8 ms MAJ = 1 (in FOCC only)
- Minimum clock period ($t_{CLKmin}$) = 2 μs
- Minimum clock hold-off ($t_{WAIT}$) = 2 μs.

### TRANSMIT DATA SERIAL INTERFACE

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC2 over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

#### *Data format*

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.7(b). The sense and function of the fields is shown in Table 10.

#### *Link protocol*

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC2 will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC2 to control the transfer of data words. DPROC2 has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC2, within the time period Buffer clear to end of TWIN, DPROC2 will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the $I^2C$-bus signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 4). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.8(b) and has the following parameters:

- Maximum transmit window (TWIN)
  - voice channel (TACS) = 60 ms
  - voice channel (AMPS) = 48 ms
  - control channel (TACS) = 29 ms
  - control channel (AMPS) = 23 ms
- Minimum clock period ($t_{CLKmin}$) = 2 μs
- Minimum wait period ($t_{WAIT}$) = 2 μs.

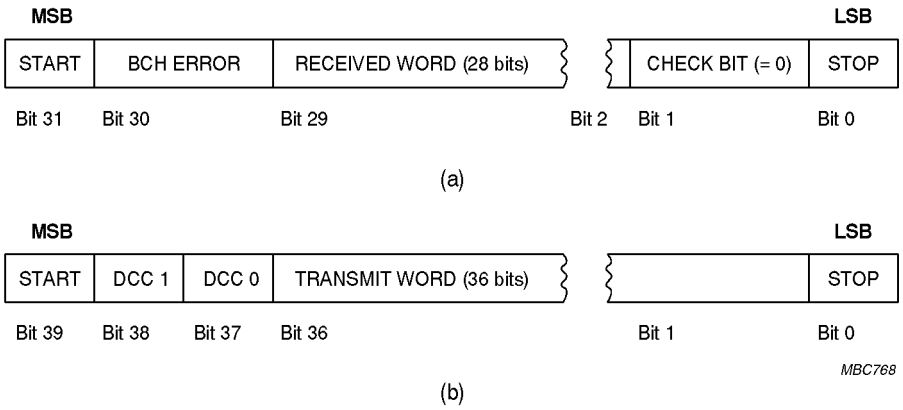
Note that TXRST will clear the transmit buffer.

**Table 9** Received data word

| BIT | TITLE | SENSE | FUNCTION |
|---|---|---|---|
| 31 | start | LOW | identifies start of word |
| 30 | BCH error | active HIGH | indicates that an uncorrected BCH error is associated with the word |
| 29 to 2 | received data | binary data | received data word |
| 1 | RXLINE error | LOW | if detected as HIGH indicates that a transmission error has occurred on the microprocessor to DPROC2 serial link |
| 0 | stop | HIGH | identifies end of the word |

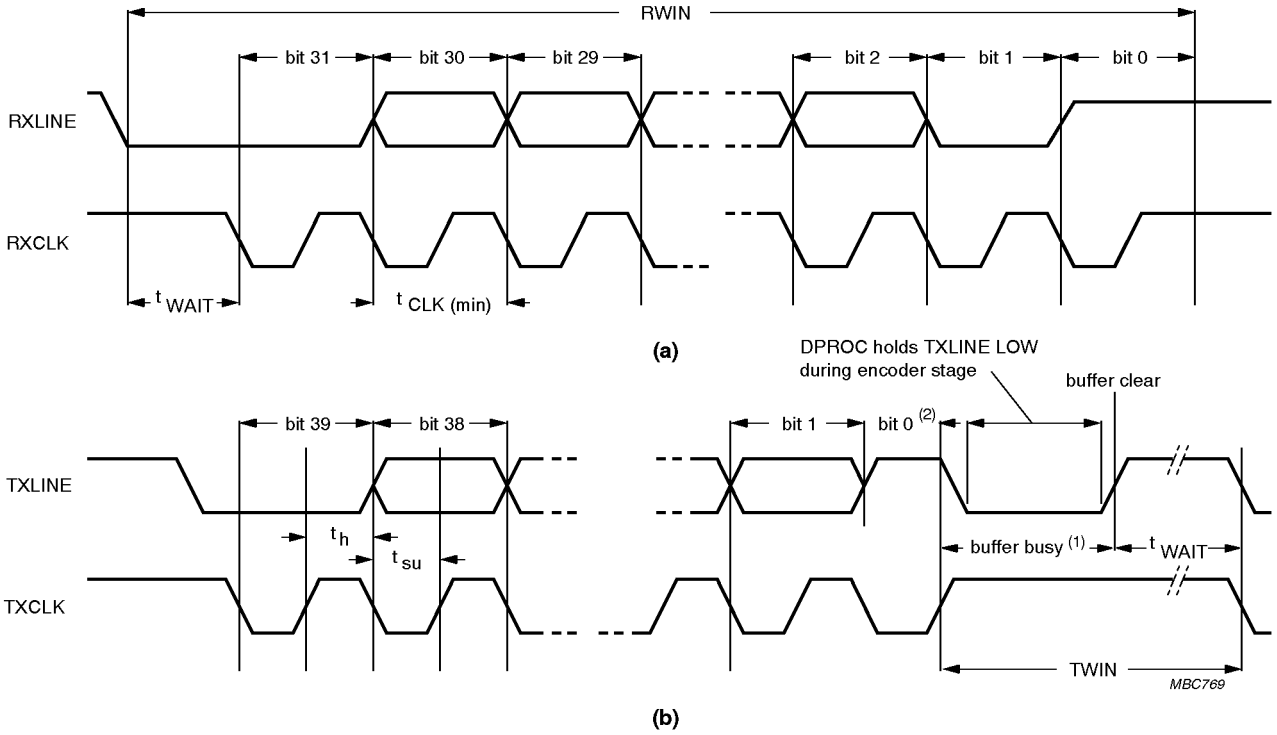
**Table 10** Transmit data word

| BIT | TITLE | SENSE | FUNCTION |
|---|---|---|---|
| 39 | start | LOW | identifies start of word |
| 38 and 37 | DCC | binary data | digital colour code (see Table 11) |
| 36 to 1 | transmit data | binary data | transmit data word |
| 0 | stop | HIGH | identifies end of the word |




(a) Received data word.
(b) Transmit data word.

Fig.7 Data word formats.




(1) The buffer time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH-to-LOW on the rising edge of TXCLK, then a framing error has occurred. This can be caused by glitches on the clock line or if an arbitration error occurred while the DPROC2 transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in Section “Reverse Control Channel Access Arbitration” - “Abort procedure (see Fig.10)”.

(a) DPROC2 to microcontroller link; receive data timing.

(b) Microcontroller to DPROC2 link; transmit data timing.

Where:
$t_h$ >100 ns
$t_{su}$ >500 ns.

Fig.8 Data timing diagrams.

### BCH AND MANCHESTER ENCODING BLOCK

The functions performed by this circuit block include:

- Reception of data from the System Controller
- Parity generation
- Message construction
- Manchester encoding.

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.

The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code (see Table 11)
- 48-bit code word.

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 11.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

### REVERSE CONTROL CHANNEL ACCESS ARBITRATION

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC2 monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC2 the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ORed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing $I^2C$-bus register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

*Initial state*

- Transmitter disabled
- DPROC2 transmit circuitry in power-up state
- TXCTRL line HIGH.

**Table 11** Digital colour code; 7-bit word

| DCC1 | DCC0 | CODED DCC | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

*Access attempt procedure*

1. System Controller decides to send message(1).
2. System Controller drives TXCTRL LOW directly.
3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I²C-bus to DPROC2.
5. System Controller sets ABREN via I²C (if required) allowing DPROC2 to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC2 via serial link(1).
9. DPROC2 sets I²C-bus signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC2 when the buffer becomes clear as shown in Fig.8(b).
13. On completion of entire message DPROC2 clears TXIP and 25 ms later the System Controller disables transmitter via I²C-bus.
14. System Controller finally sends TXRST to prepare DPROC2 for next transmission.

*Abort procedure (see Fig.10)*

1. DPROC2 immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC2 sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC2 for next transmission.

### SIGNAL TONE GENERATION (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

(1) At stage 1 the system controller may choose to preload DPROC2 with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC2. Figure 9 illustrates the DPROC2 data transmission timing.

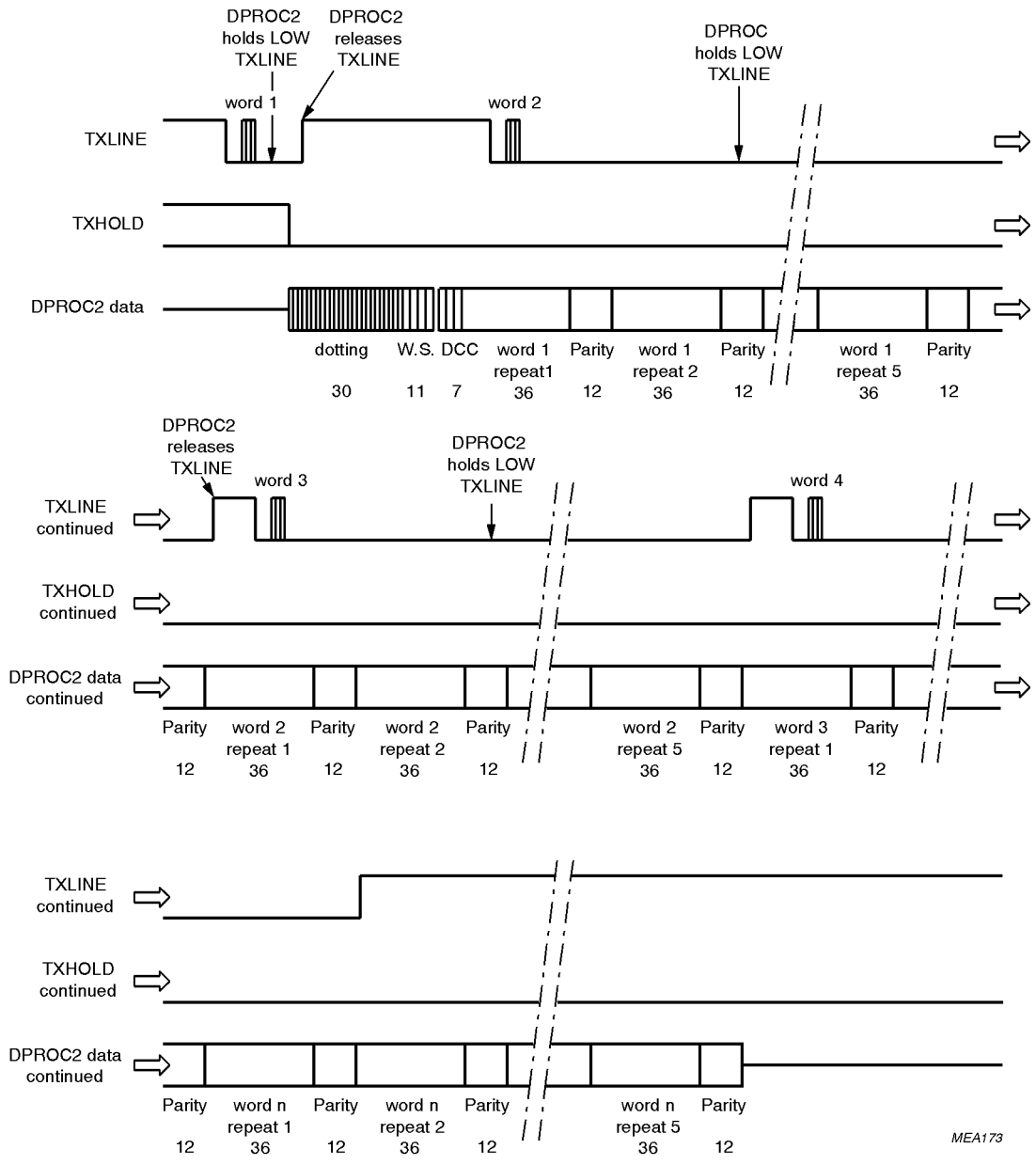



Fig.9 DPROC2 data transmission timing/microcontroller interface.

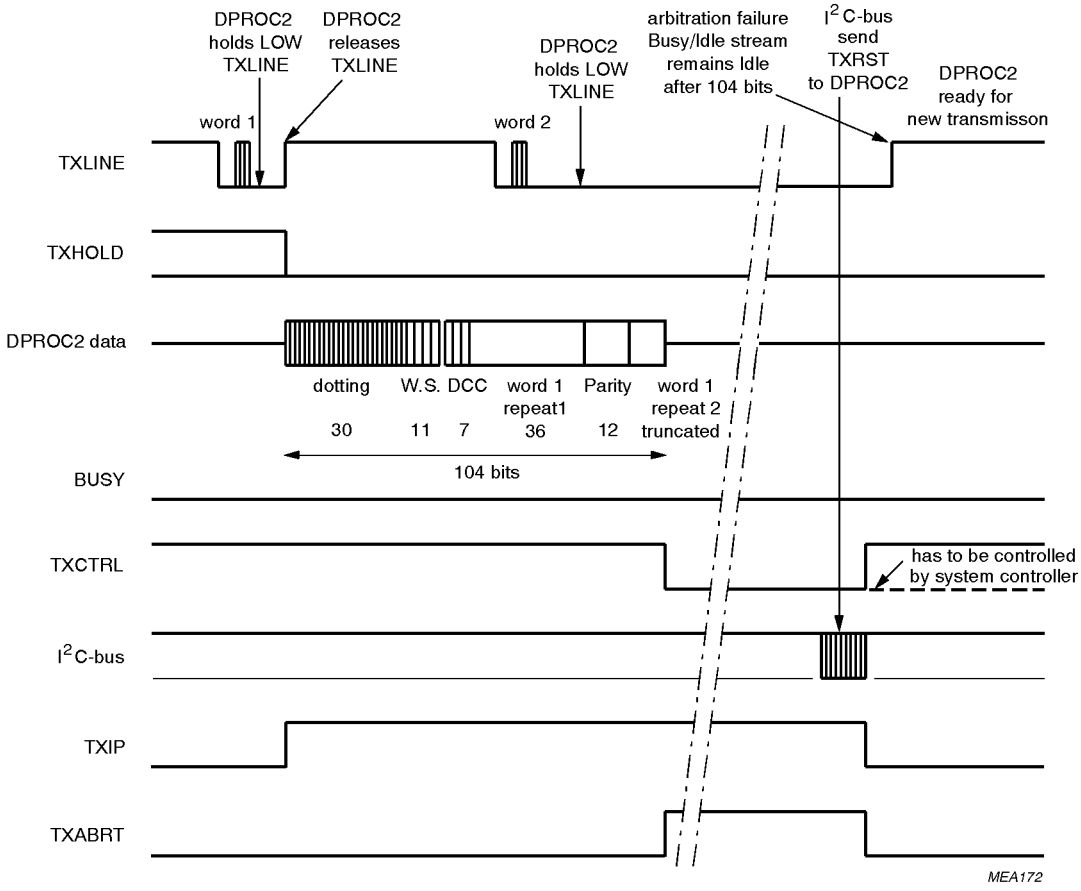



Fig.10 DPROC data transmission timing/microcontroller interface during arbitration failure.

## Analog circuit blocks

### General

The analog signal processing functions on DPROC2 are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by RC active filters, passive interpolators and comparators.

The RC sections, the Anti-Alias Filter and the Clock Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolator increases the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolator is converted to a sampled 2-state digital signal by a Comparator. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC2 output signals, and conversion to the sampled analog domain.

These analog sections of the device are shown in Fig.1.

### Bias Generator

The Bias Generator generates the analog ground reference voltage (AGND) used internally within the DPROC2 device. To minimize noise AGND must be externally decoupled to $V_{SSA}$ as shown in Fig.12. It also contains a current reference to generate all bias currents for the analog circuits.

### Anti-Aliasing Filter

The Anti-Aliasing Filter is placed before the SAT filter block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Aliasing Filter is a time-continuous RC-active low-pass filter.

### SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

### Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the SAT filter. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

### Comparators

The Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal. To prevent unwanted signals being processed by the digital circuitry both comparators have a hysteresis implemented

### Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC2. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.

The data streams are enabled by the $I^2C$ signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The typical relative signal weights applied in the summer (with respect to the data path) are shown in Table 12.

**Table 12** Typical relative signal weight

| SIGNAL | RELATIVE OUTPUT LEVEL AMPS AND TACS |
|---|---|
| ST or DATA | 1.0 |
| SAT | 0.25 |

### Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC2 output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC-coupling from the DATA pin.

### Clock Filter

The Clock Noise Filter is a non-critical continuous time RC-active low-pass filter used to remove any switching transient residues from the output signal. It contains an output driver stage to provide a low output impedance and sufficient driving capability for the pin DATA

## APPLICATION INFORMATION

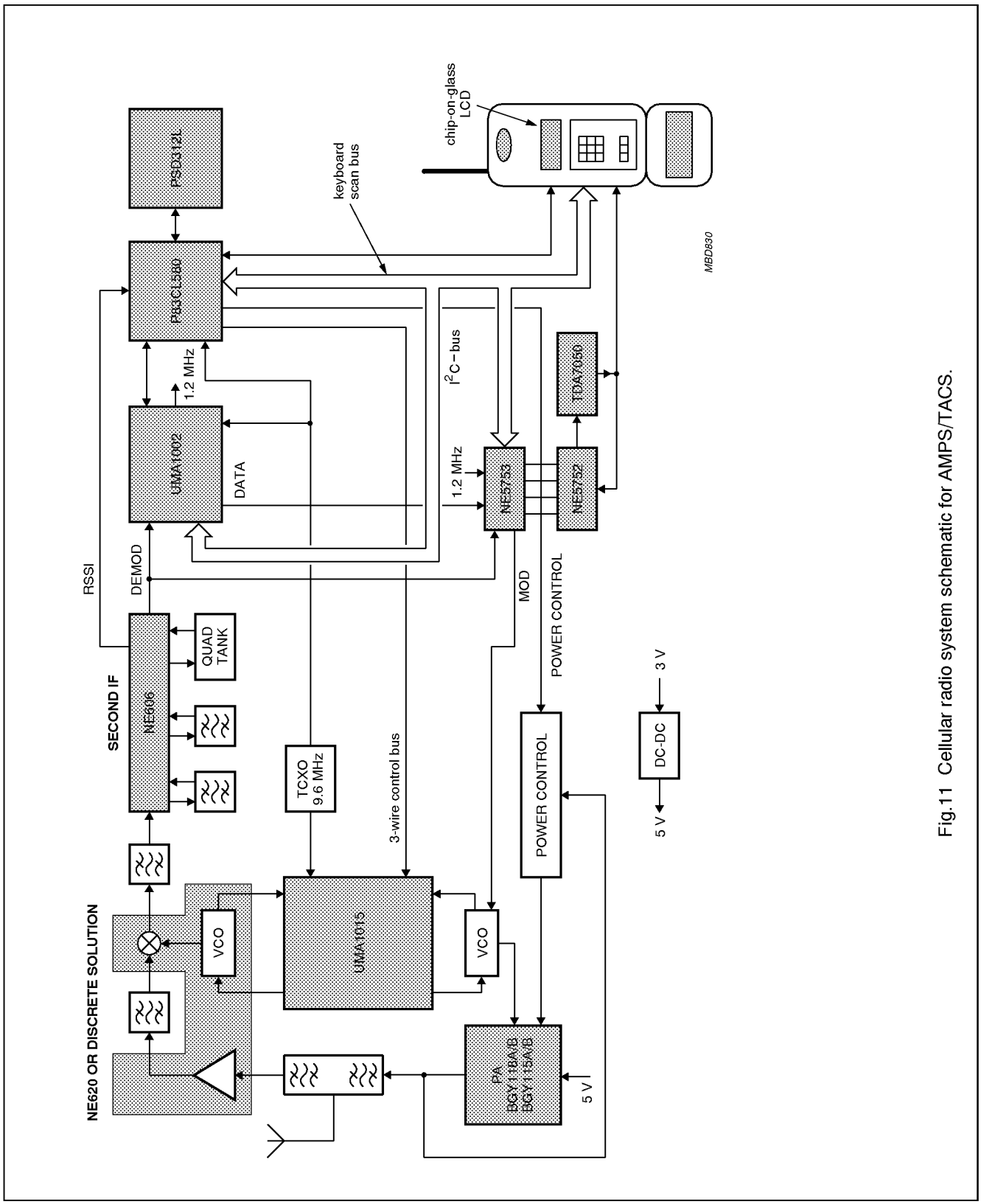



Fig.11 Cellular radio system schematic for AMPS/TACS.

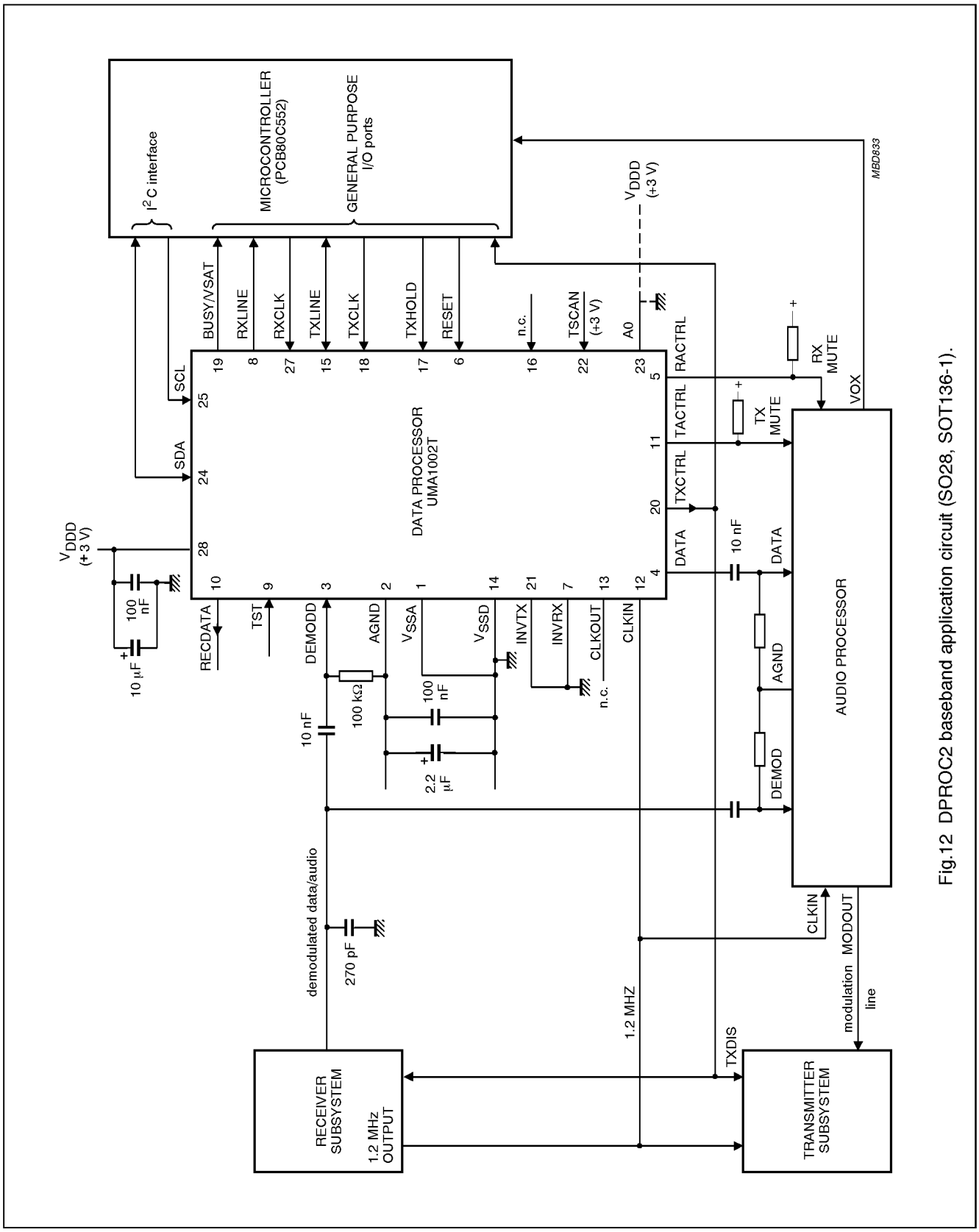



Fig.12 DPROC2 baseband application circuit (SO28, SOT136-1).

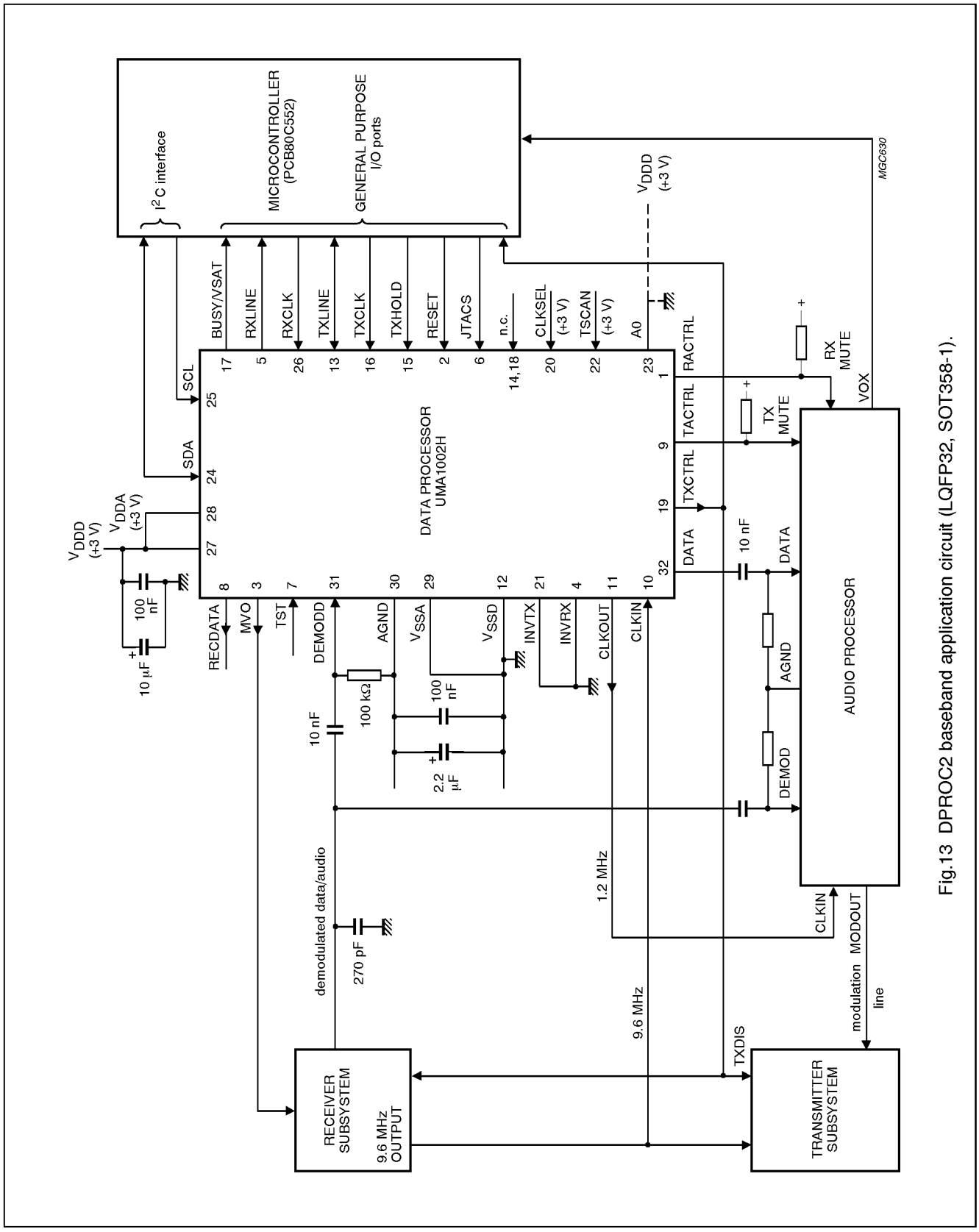



Fig.13 DPROC2 baseband application circuit (LQFP32, SOT358-1).

## SIGNALLING FORMATS

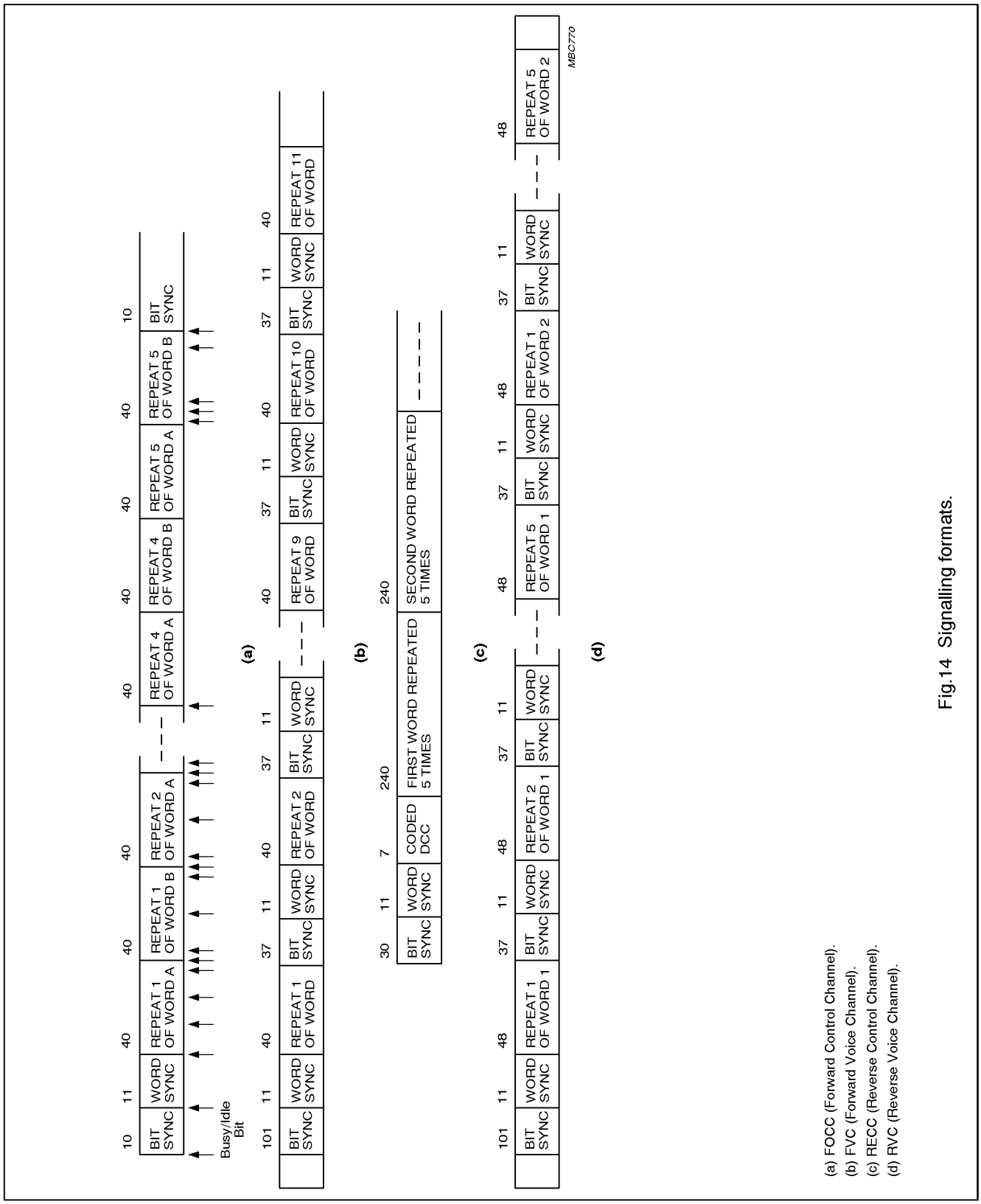



Fig.14 Signalling formats.

(a) FOCC (Forward Control Channel).
(b) FVC (Forward Voice Channel).
(c) RECC (Reverse Control Channel).
(d) RVC (Reverse Voice Channel).